CS 105 Spring 2023
Check-in 6 March 8, 2023

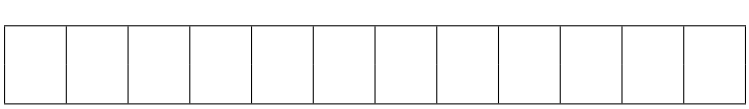
The following table depicts a 2-way set associate cache, with a 4 byte block size and 8 total lines:

2-way Set Associative Cache												
Index	Tag	Valid	Data				Tag	Valid	Data			
0	29	0	34	29	8E	00	87	0	39	AE	AB	07
1	F3	1	0D	8F	AA	E9	3D	1	0C	3C	EA	01
2	A7	1	88	4B	E2	04	AB	1	D2	13	B0	05
3	3B	1	AC	99	FF	1F	E0	0	B5	47	0D	00

You should assume:

- Memory is byte addressable. All memory accesses read/write 1-byte.
- Memory addresses are 12 bits.
- The cache uses a least-recently used (LRU) eviction policy.
- The cache is write-back, write-allocate.

1. The box below depicts a 12-bit memory address. Indicate (by labeling the diagram) the fields that would be used to determine (1) the tag, (2) the index, and (3) the offset.



2. Consider the following sequence of accesses (yes, they occur sequentially). For each access, indicate whether that access would correspond to a cache hit (yes/no), what byte is read (for reads), and whether or not a memory write will occur. Use the notation `MEM[addr]` for reads that read an unknown value from memory.

Operation	Tag	Index	Offset	Hit?	Byte read	Mem write?
i. `Write $0x00, 0xAB8`					n/a	
ii. `Read 0xA78`						
iii. `Write $0x01, 0x472`					n/a	
iv. `Read 0x472`						
v. `Read 0xEBA`						