INSTRUCCIONES DE CARGA Y ALMACENAMIENTO									
Instr.	Ejemplo	Significado	Código de operación						Microinstrucciones
LI	LI Rd, #Slit16	Rd = Slit16	01	Rd	Slit16				WR
LWI	LWI Rd, lit16	Rd = Mem[lit16]	02	Rd	lit16				SDMD SWD WR
LW	LW Rd,lit12(Rt)	Rd = Mem[Rt+lit12]	23	Rd	Rt	lit12			SWD SEXT SOP2 ALUOP=0011 WR LF
SWI	SWI Rd, lit16	Mem[lit16] = Rd	03	Rd	lit16				SR2 SDMD WD
SW	SW Rd, lit12(Rt)	Mem[Rt+lit12] = Rd	04	Rd	Rt	lit12			SR2 SEXT SOP2 ALUOP=0011 WD LF
INSTRUCCIONES ARITMÉTICAS									
ADD	ADD Rd,Rt,Rs	Rd = Rt+Rs	00	Rd	Rt	Rs	S/U	00	SWD WR LF SR ALUOP=0011
SUB	SUB Rd,Rt,Rs	Rd = Rt-Rs	00	Rd	Rt	Rs	S/U	01	SWD WR LF SR ALUOP=0111
ADDI	ADDI Rd,Rt,#Slit12	Rd = Rt+Slit12	05	Rd	Rt	Slit12			SWD WR LF SR ALUOP=0011 SOP2
SUBI	SUBI Rd,Rt,#Slit12	Rd = Rt-Slit12	06	Rd	Rt	Slit12			SWD WR LF SR ALUOP=0111 SOP2
INSTRUCCIONES LÓGICAS									
AND	AND Rd,Rt,R	Rd=Rt&Rs	00	Rd	Rt	Rs	S/U	02	SWD WR SR ALUOP=0000 LF
OR	OR Rd,Rt,Rs	Rd=Rt | Rs	00	Rd	Rt	Rs	S/U	03	SWD WR SR ALUOP=0001 LF
XOR	XOR Rd,Rt,Rs	Rd=Rt ^ Rs	00	Rd	Rt	Rs	S/U	04	SWD WR SR ALUOP=0010 LF
NAND	NAND Rd,Rt,Rs	Rd=~(Rt & Rs)	00	Rd	Rt	Rs	S/U	05	SWD WR SR ALUOP=1101 LF
NOR	NOR Rd,Rt,Rs	Rd=~(Rt | Rs)	00	Rd	Rt	Rs	S/U	06	SWD WR SR ALUOP=1100 LF
XNOR	NOR Rd,Rt,Rs	Rd=~(Rt ^ Rs)	00	Rd	Rt	Rs	S/U	07	SWD WR SR ALUOP=0110 LF
NOT	NOT Rd, Rs	Rd = ~Rs	00	Rd	Rs	Rs	S/U	08	SWD WR SR ALUOP=1101 LF
ANDI	ANDI Rd,Rt,#lit12	Rd=Rt & lit12	07	Rd	Rt	lit12			SEXT SOP2 ALUOP=0000 LF SR SWD WR
ORI	ORI Rd,Rt,#lit12	Rd=Rt | lit12	08	Rd	Rt	lit12			SEXT SOP2 ALUOP=0001 LF SR SWD WR

XORI	XORI Rd,Rt,#lit12	Rd=Rt ^ lit12	09	Rd	Rt	lit12			SEXT SOP2 ALUOP=0010 LF SR SWD WR
NANDI	NANDI Rd,Rt,#lit12	Rd=~(Rt & lit12)	10	Rd	Rt	lit12			SEXT SOP2 ALUOP=1101 LF SR SWD WR
NORI	NORI Rd,Rt,#lit12	Rd=~(Rt | lit12)	11	Rd	Rt	lit12			SEXT SOP2 ALUOP=1100 LF SR SWD WR
XNORI	XNORI Rd,Rt,#lit12	Rd=~(Rt ^ lit12)	12	Rd	Rt	lit12			SEXT SOP2 ALUOP=0110 LF SR SWD WR
INSTRUCCIONES DE CORRIMIENTO									
SLL	SLL Rd,Rt,#lit4	Rd=Rt<<lit4	00	Rd	Rt	S/U	lit4	09	SHE DIR WR
SRL	SRL Rd,Rt,#lit4	Rd=Rt>>lit4	00	Rd	Rt	S/U	lit4	10	SHE WR
INSTRUCCIONES DE SALTOS CONDICIONALES E INCONDICIONALES									
BEQI	BEQI Rd,Rt,Slit12	If(Rd==Rt) goto Slit12 PC = PC + Slit12	13	Rd	Rt	Slit12			SR2 LF ALUOP=0111 SOP1 SOP2 ALUOP=0011 LF SR SDMP WPC
BNEI	BNEI Rd,Rt,Slit12	If(Rd!=Rt) goto Slit12 PC = PC + Slit12	14	Rd	Rt	Slit12			SR2 LF ALUOP=0111 SOP1 SOP2 ALUOP=0011 LF SR SDMP WPC
BLTI	BLTI Rd,Rt,Slit12	If(Rd<Rt) goto Slit12 PC = PC + Slit12	15	Rd	Rt	Slit12			SR2 LF ALUOP=0111 SOP1 SOP2 ALUOP=0011 LF SR SDMP WPC
BLETI	BLETI Rd,Rt,Slit12	If(Rd<=Rt) goto Slit12 PC = PC + Slit12	16	Rd	Rt	Slit12			SR2 LF ALUOP=0111 SOP1 SOP2 ALUOP=0011 LF SR SDMP WPC
BGTI	BGTI Rd,Rt,Slit12	If(Rd>Rt) goto Slit12 PC = PC + Slit12	17	Rd	Rt	Slit12			SR2 LF ALUOP=0111 SOP1 SOP2 ALUOP=0011 LF SR SDMP WPC
BGETI	BGETI Rd,Rt,Slit12	If(Rd>=Rt) goto Slit12 PC = PC + Slit12	18	Rd	Rt	Slit12			SR2 LF ALUOP=0111 SOP1 SOP2 ALUOP=0011 LF SR SDMP WPC
B	B lit16	PC = lit16	19	S/U	lit16				WPC
INSTRUCCIONES DE MANEJO DE SUBRUTINAS									
CALL	CALL #lit16	PC(n+1) = lit16	20	S/U	lit16				UP WPC

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RET	RET	PC = PC(n-1)	21	S/U	S/U	S/U	S/U	S/U	DW
OTRAS INSTRUCCIONES									
NOP	NOP		22	S/U	S/U	S/U	S/U	S/U	------

MEMORIA DE MICROCÓDIGO DE OPERACIÓN																		
OP	UP	DW	WPC	SDMP	SR2	SWD	SHE	DIR	WR	LF	SEXT	SOP1	SOP2	ALUOP	SDMD	WD	SR	ITR
	1	2	3	4	5	6	7	8	9	10	11	12	13	14-17	18	19	20	
0	0	0	0	0	1	0	0	0	0	1	0	0	0	0111	0	0	0	BCON
1	0	0	0	0	0	0	0	0	1	0	0	0	0	0000	0	0	0	LI
2	0	0	0	0	0	1	0	0	1	0	0	0	0	0000	1	0	0	LWI
3	0	0	0	0	1	0	0	0	0	0	0	0	0	0000	1	1	0	SWI
4	0	0	0	0	1	0	0	0	0	1	1	0	1	0011	0	1	0	SW
5	0	0	0	0	0	1	0	0	1	1	0	0	1	0011	0	0	1	ADDI
6	0	0	0	0	0	1	0	0	1	1	0	0	1	0111	0	0	1	SUBI
7	0	0	0	0	0	1	0	0	1	1	1	0	1	0000	0	0	1	ANDI
8	0	0	0	0	0	1	0	0	1	1	1	0	1	0001	0	0	1	ORI
9	0	0	0	0	0	1	0	0	1	1	1	0	1	0010	0	0	1	XORI
10	0	0	0	0	0	1	0	0	1	1	1	0	1	1101	0	0	1	NANDI
11	0	0	0	0	0	1	0	0	1	1	1	0	1	1100	0	0	1	NORI
12	0	0	0	0	0	1	0	0	1	1	1	0	1	0110	0	0	1	XNORI
13	0	0	1	1	0	0	0	0	0	1	0	1	1	0011	0	0	1	BEQI
14	0	0	1	1	0	0	0	0	0	1	0	1	1	0011	0	0	1	BNEI
15	0	0	1	1	0	0	0	0	0	1	0	1	1	0011	0	0	1	BLTI
16	0	0	1	1	0	0	0	0	0	1	0	1	1	0011	0	0	1	BLETI
17	0	0	1	1	0	0	0	0	0	1	0	1	1	0011	0	0	1	BGTI
18	0	0	1	1	0	0	0	0	0	1	0	1	1	0011	0	0	1	BGETI
19	0	0	1	0	0	0	0	0	0	0	0	0	0	0000	0	0	0	B
20	1	0	1	0	0	0	0	0	0	0	0	0	0	0000	0	0	0	CALL
21	0	1	0	0	0	0	0	0	0	0	0	0	0	0000	0	0	0	RET
22	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	0	0	0	NOP
23	0	0	0	0	0	1	0	0	1	1	1	0	1	0011	0	0	0	LW

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MEMORIA DE MICROCÓDIGO DE FUNCIÓN																	
FN	UP	DW	WPC	SDMP	SR2	SWD	SHE	DIR	WR	LF	SEXT	SOP1	SOP2	ALUOP	SDMD	WD	SR	ITR
	1	2	3	4	5	6	7	8	9	10	11	12	13	14-17	18	19	20	
0	0	0	0	0	0	1	0	0	1	1	0	0	0	0011	0	0	1	ADD
1	0	0	0	0	0	1	0	0	1	1	0	0	0	0111	0	0	1	SUB
2	0	0	0	0	0	1	0	0	1	1	0	0	0	0000	0	0	1	AND
3	0	0	0	0	0	1	0	0	1	1	0	0	0	0001	0	0	1	OR
4	0	0	0	0	0	1	0	0	1	1	0	0	0	0010	0	0	1	XOR
5	0	0	0	0	0	1	0	0	1	1	0	0	0	1101	0	0	1	NAND
6	0	0	0	0	0	1	0	0	1	1	0	0	0	1100	0	0	1	NOR
7	0	0	0	0	0	1	0	0	1	1	0	0	0	0110	0	0	1	XNOR
8	0	0	0	0	0	1	0	0	1	1	0	0	0	1101	0	0	1	NOT
9	0	0	0	0	0	0	1	1	1	0	0	0	0	0000	0	0	0	SLL
10	0	0	0	0	0	0	1	0	1	0	0	0	0	0000	0	0	0	SRL

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