**Digital Design and Computer Organisation Laboratory**

**3rd Semester, Academic Year 2024**

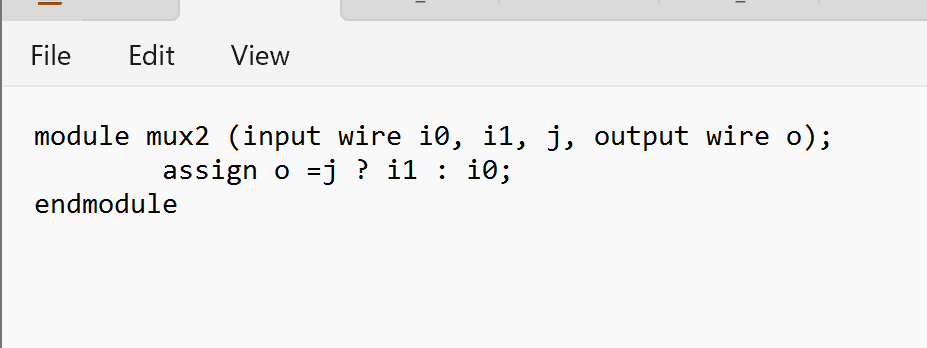
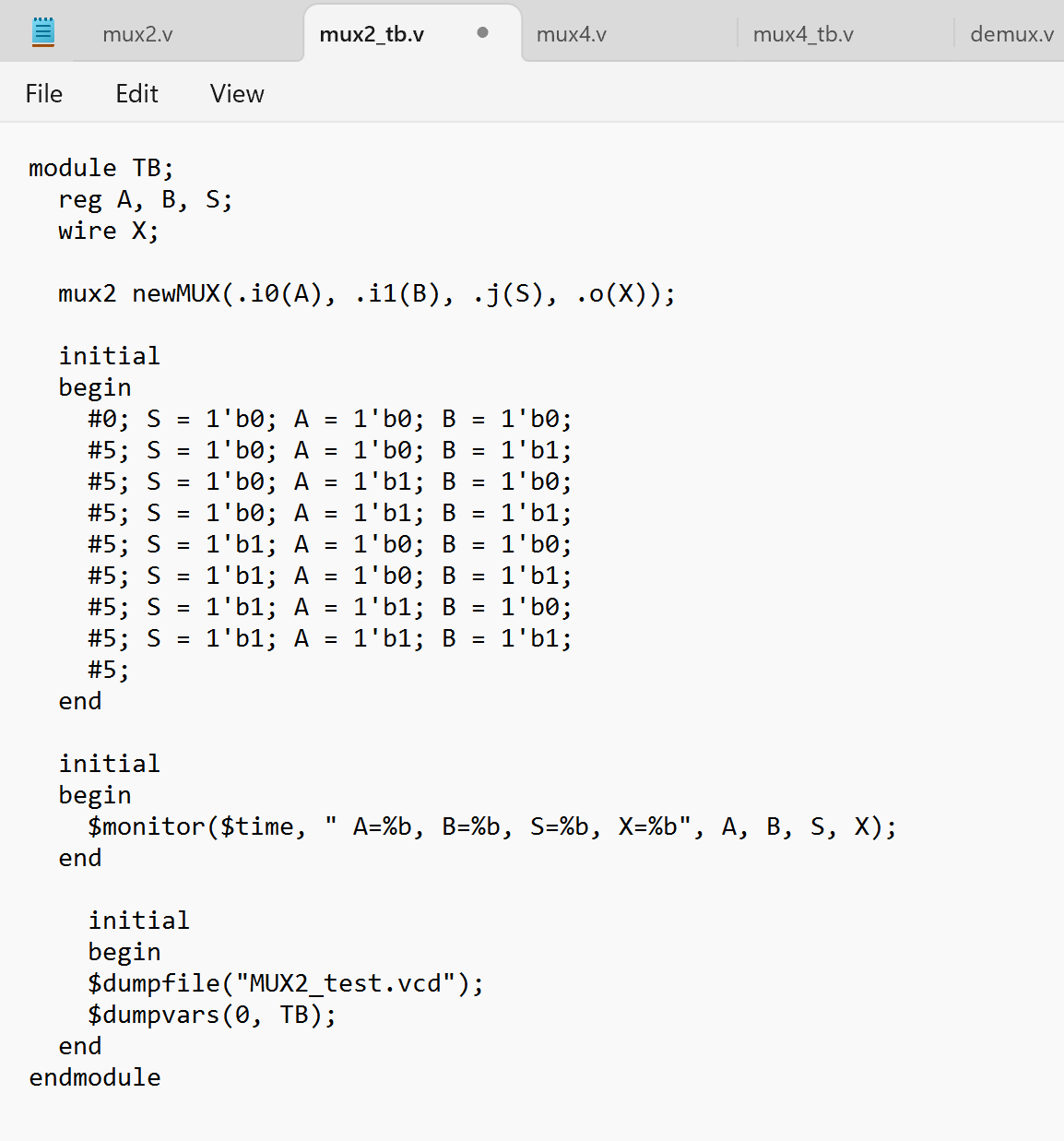
Date:06/09/2024

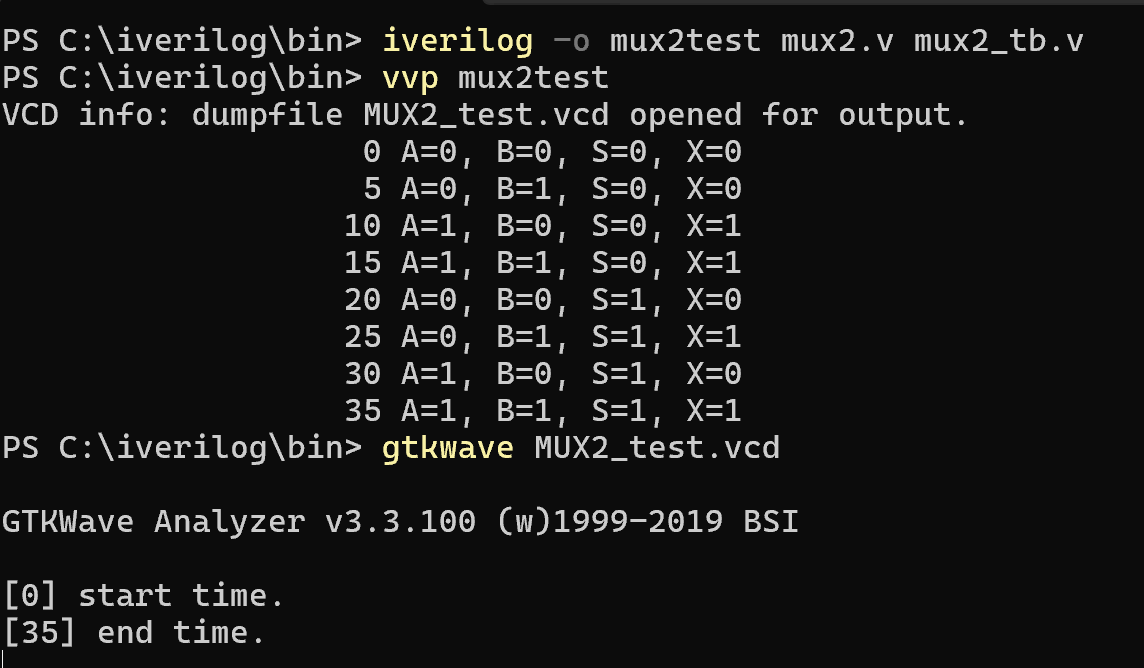
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| --- | --- | --- |
| Name: Rohan Cyriac Suraj | SRN:PES2UG23CS490 | Section  H |

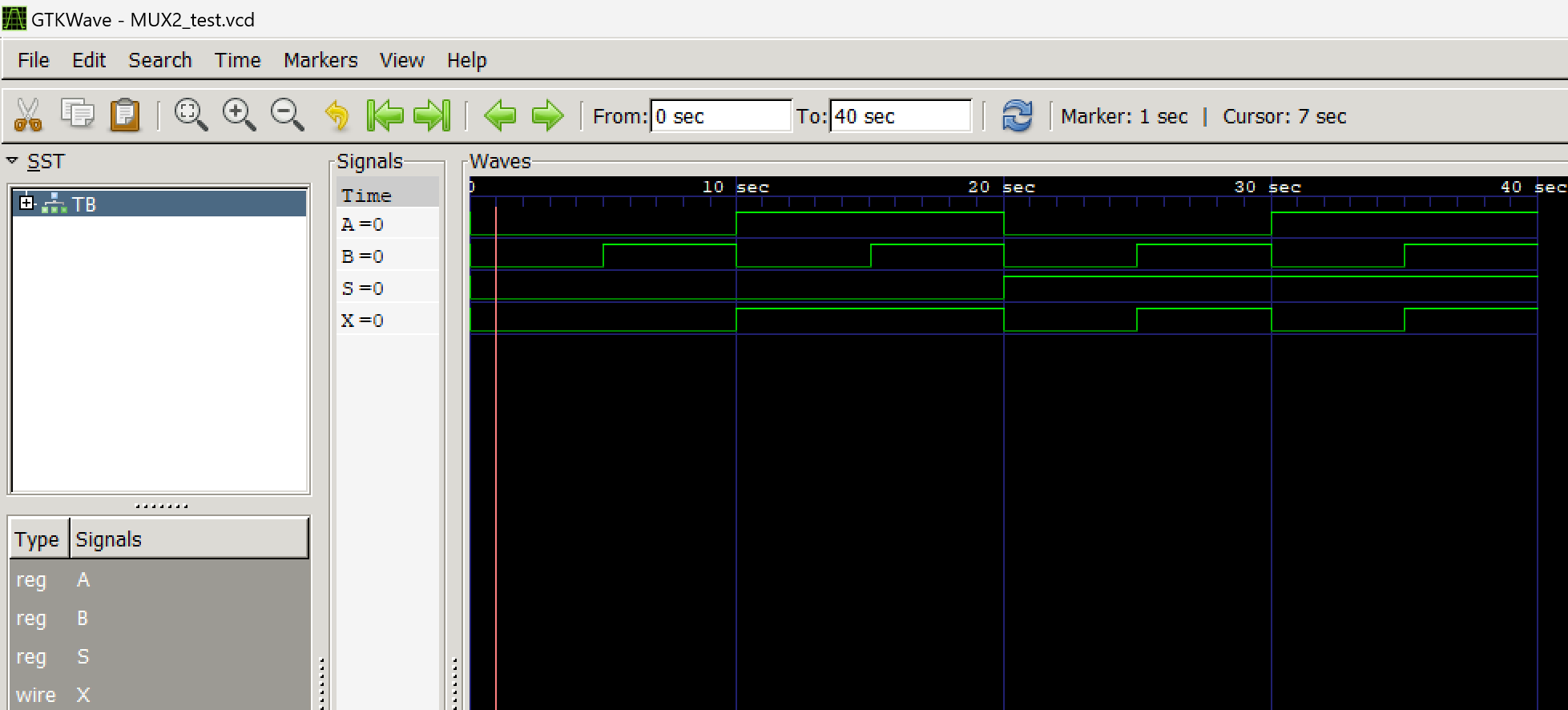
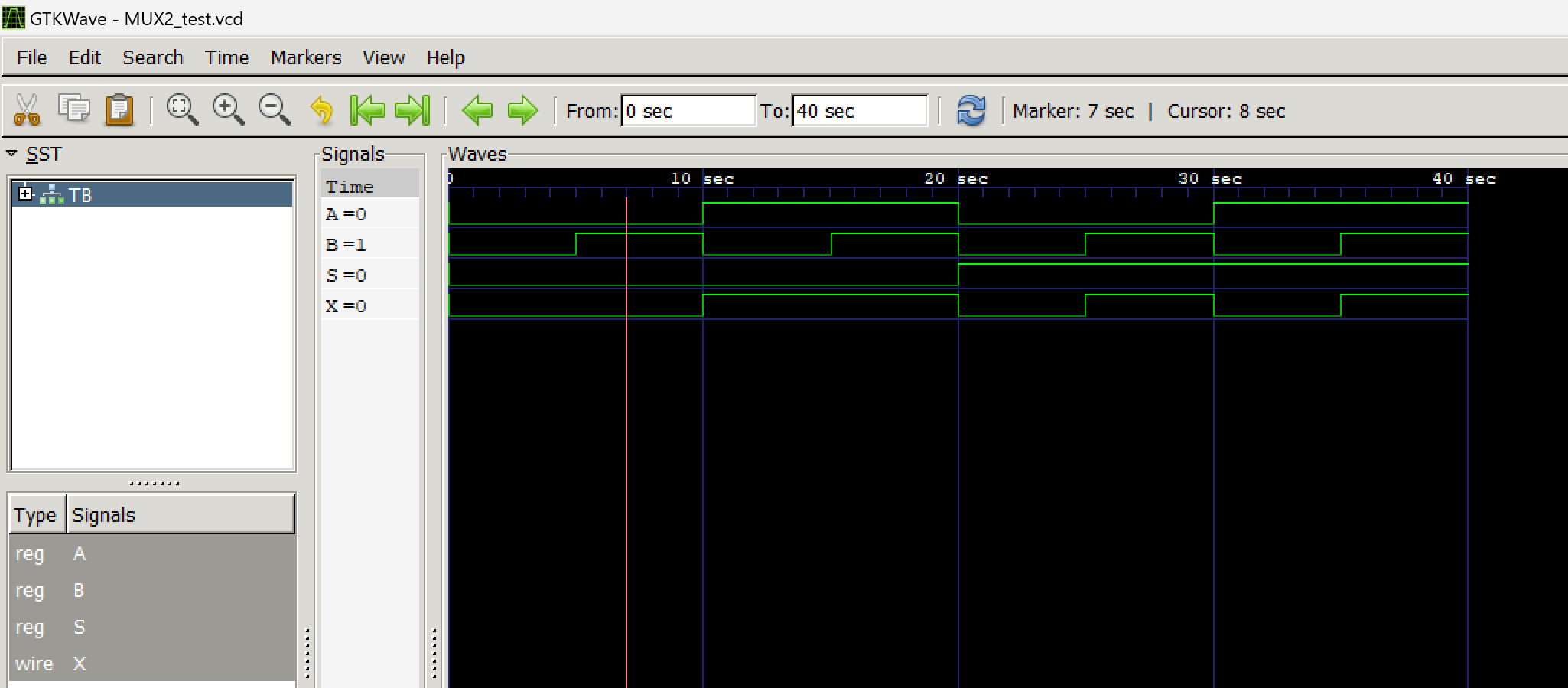
Week#\_\_\_\_4\_\_\_\_\_\_\_ Program Number: \_\_\_\_4\_\_\_

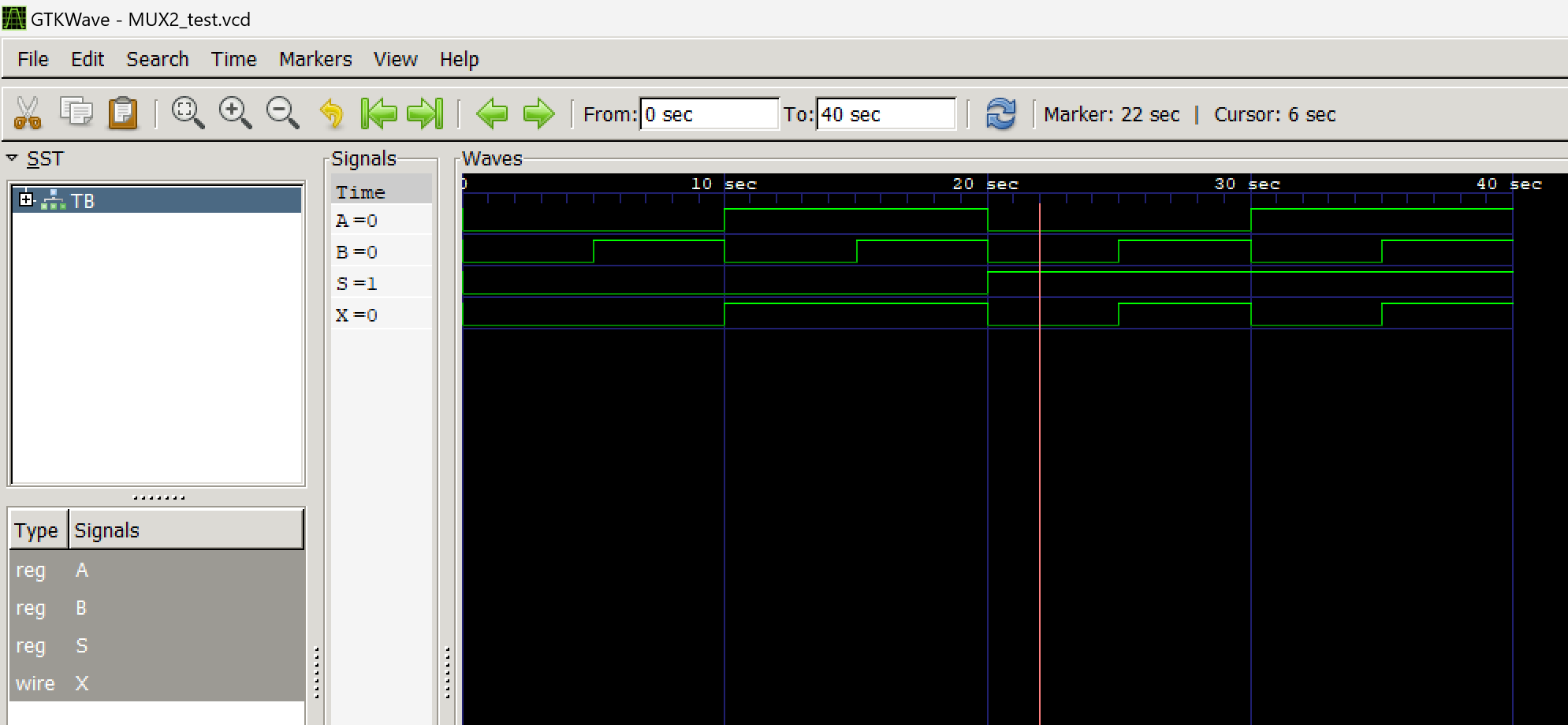
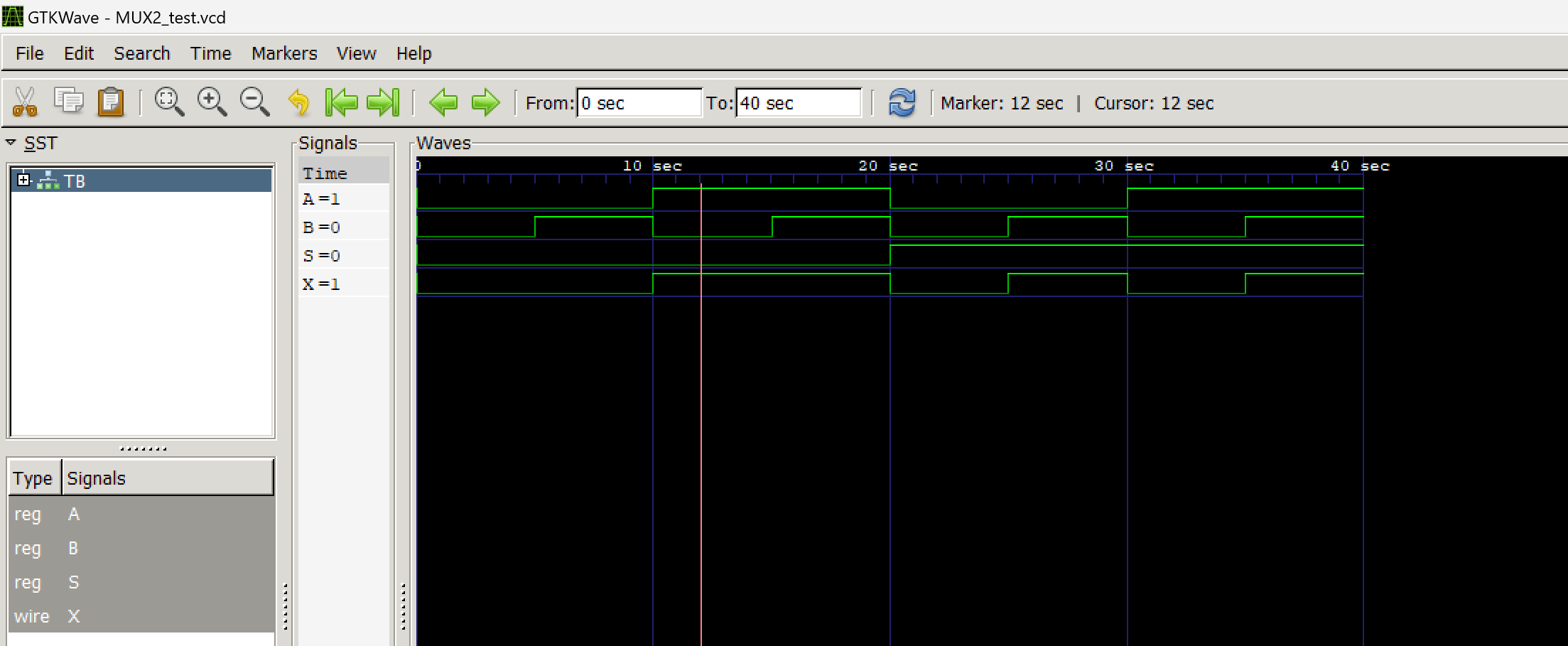
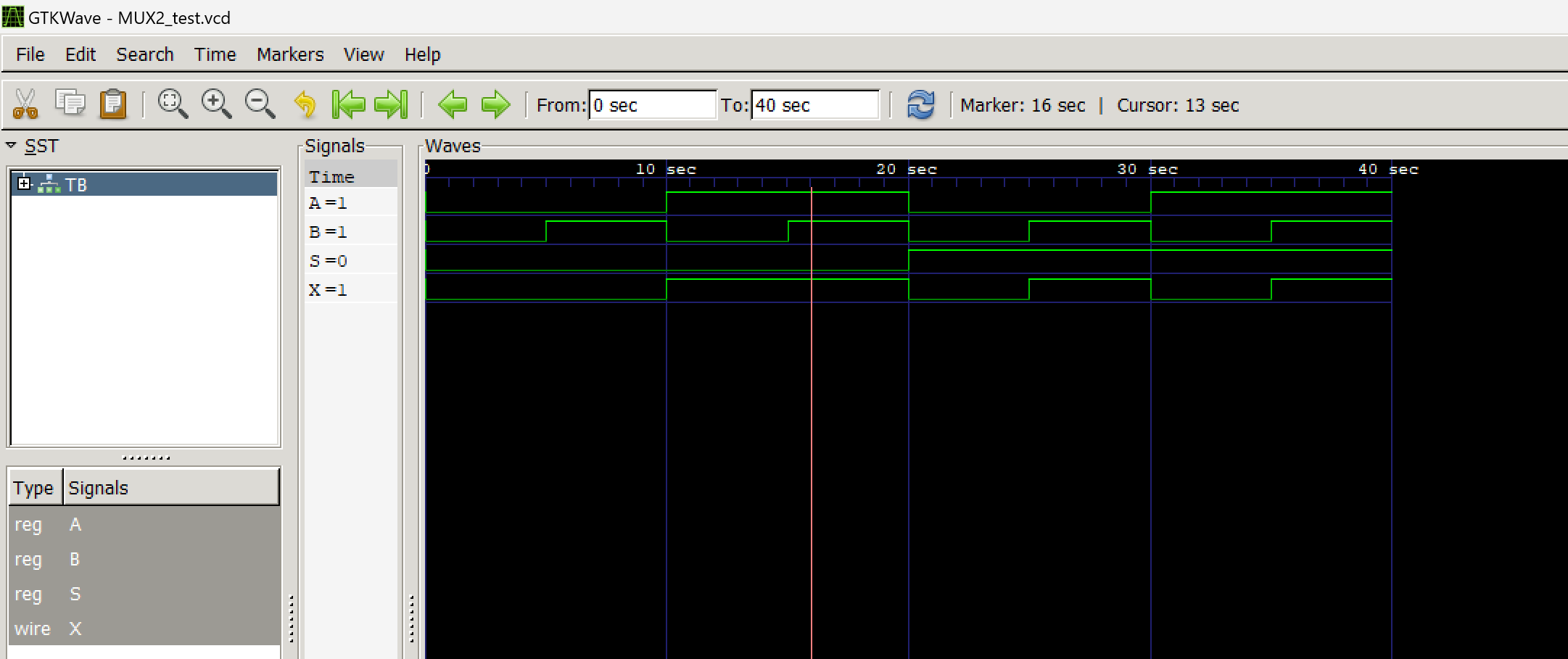
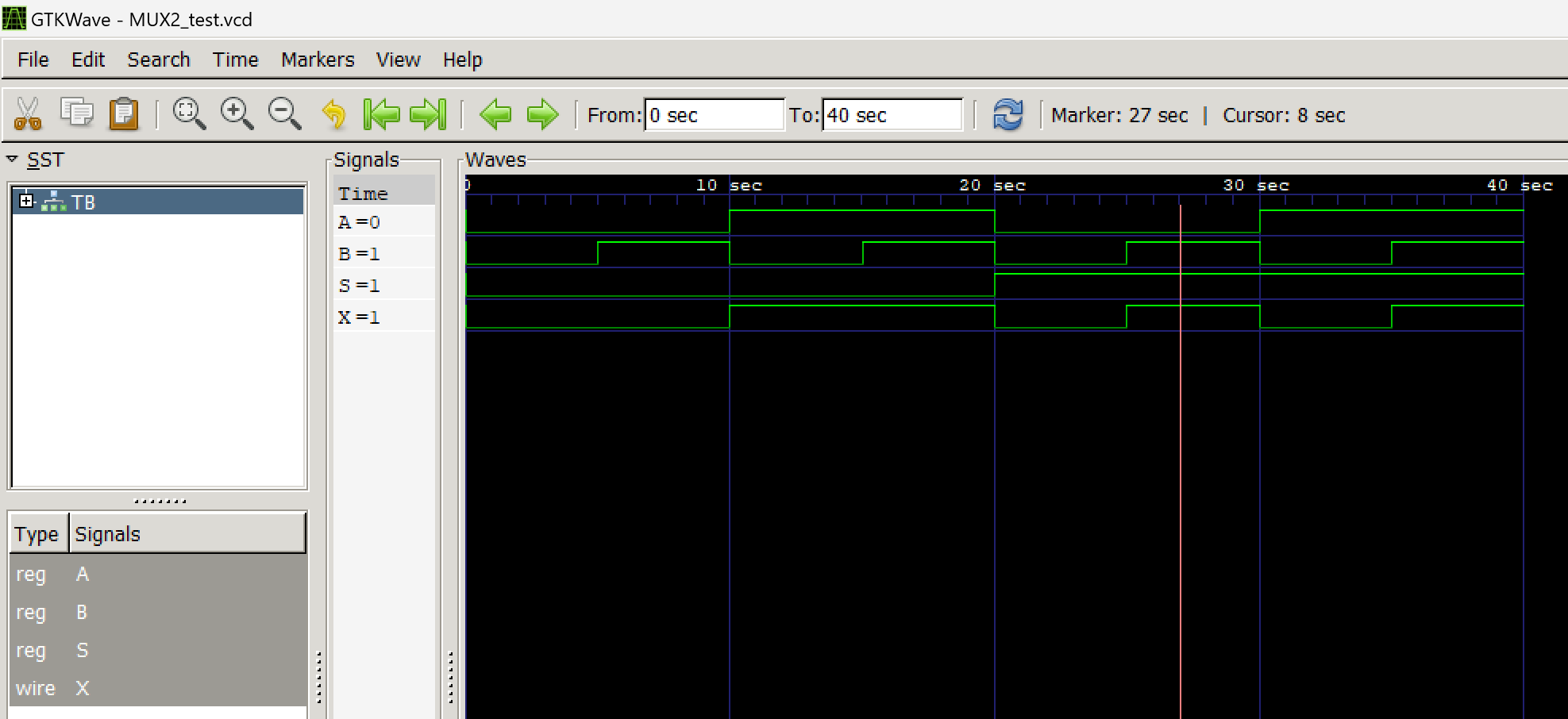
**WRITE A VERILOG PROGRAM TO MODEL A 2:1 MUX . GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE**

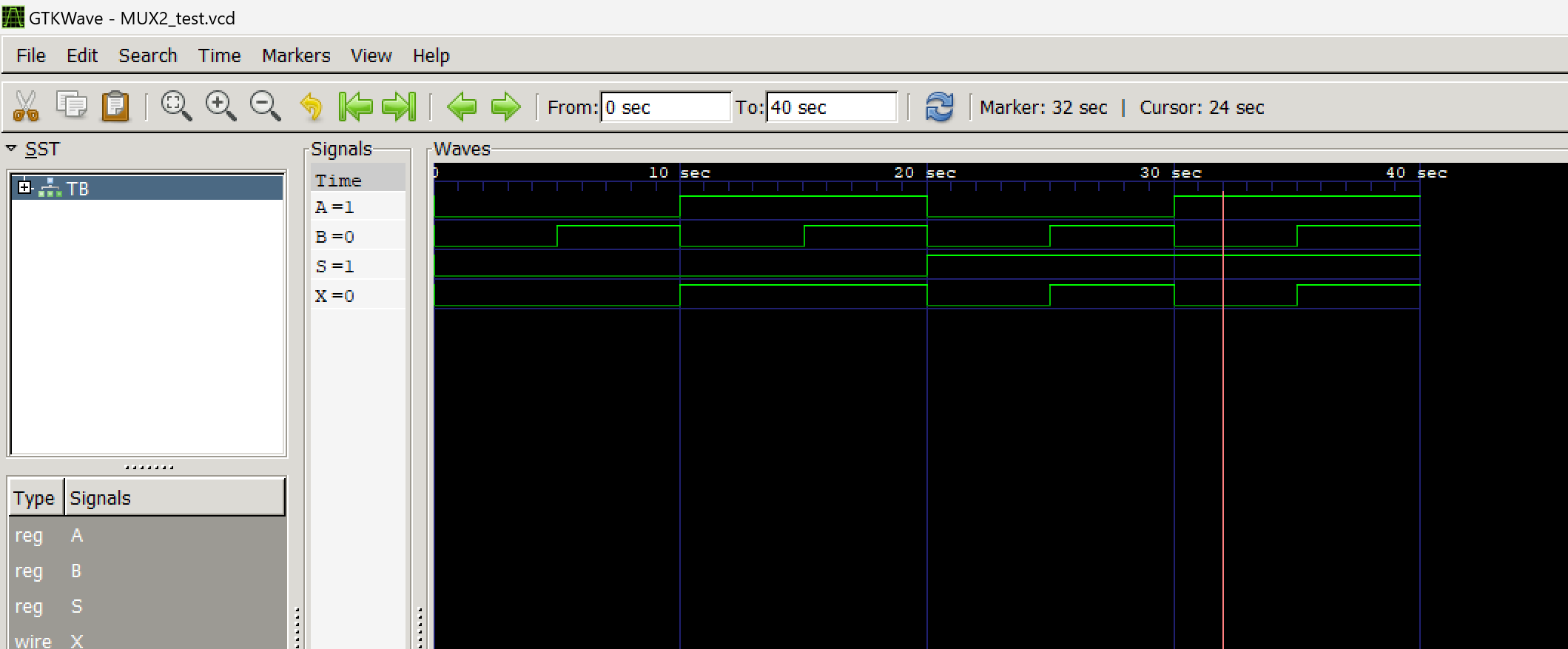
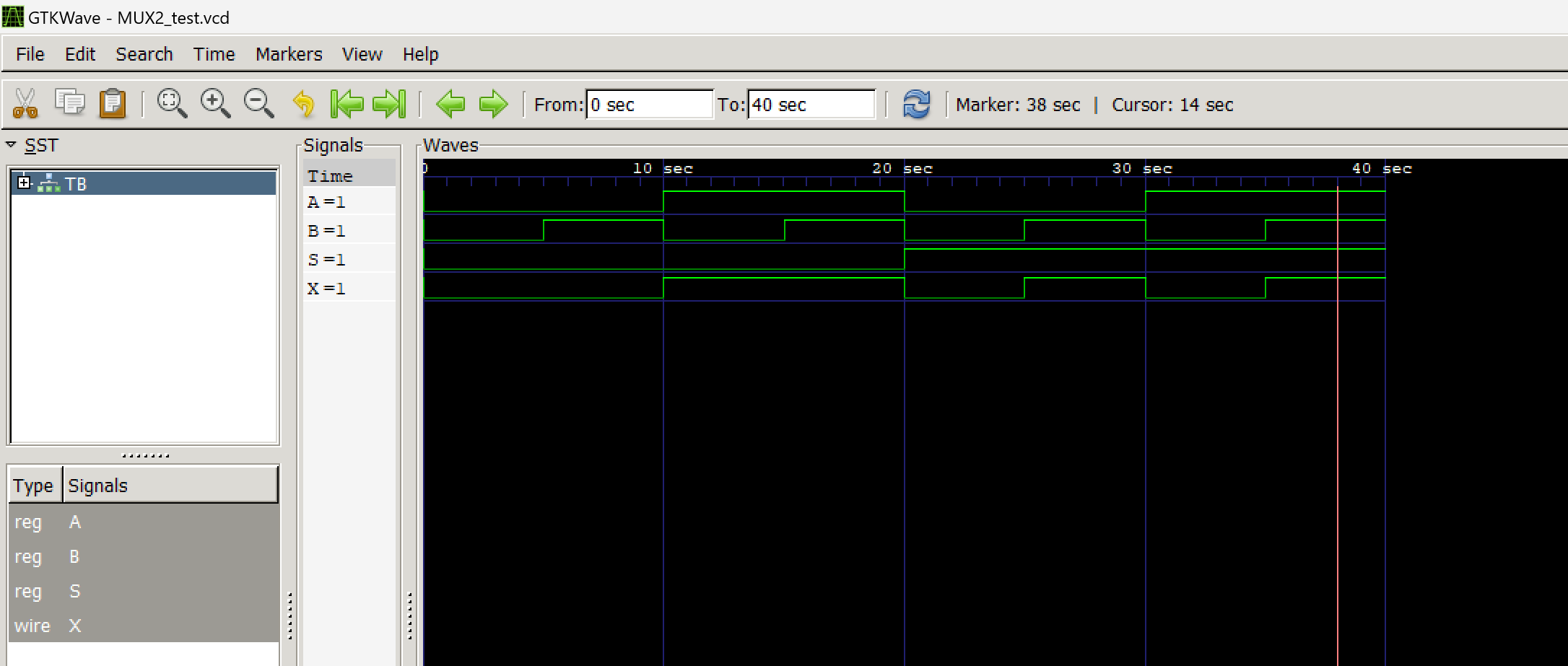
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

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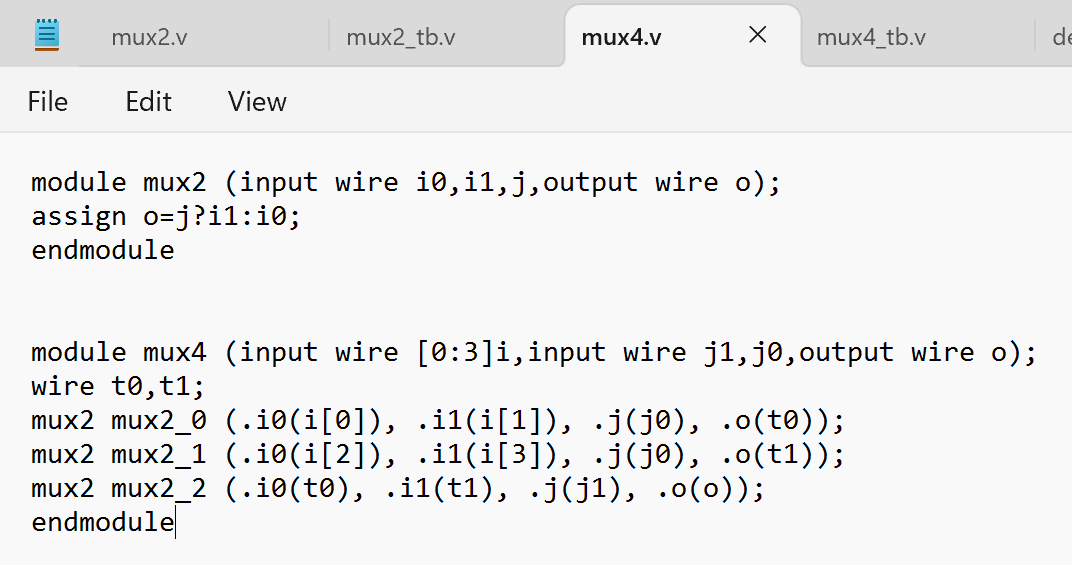
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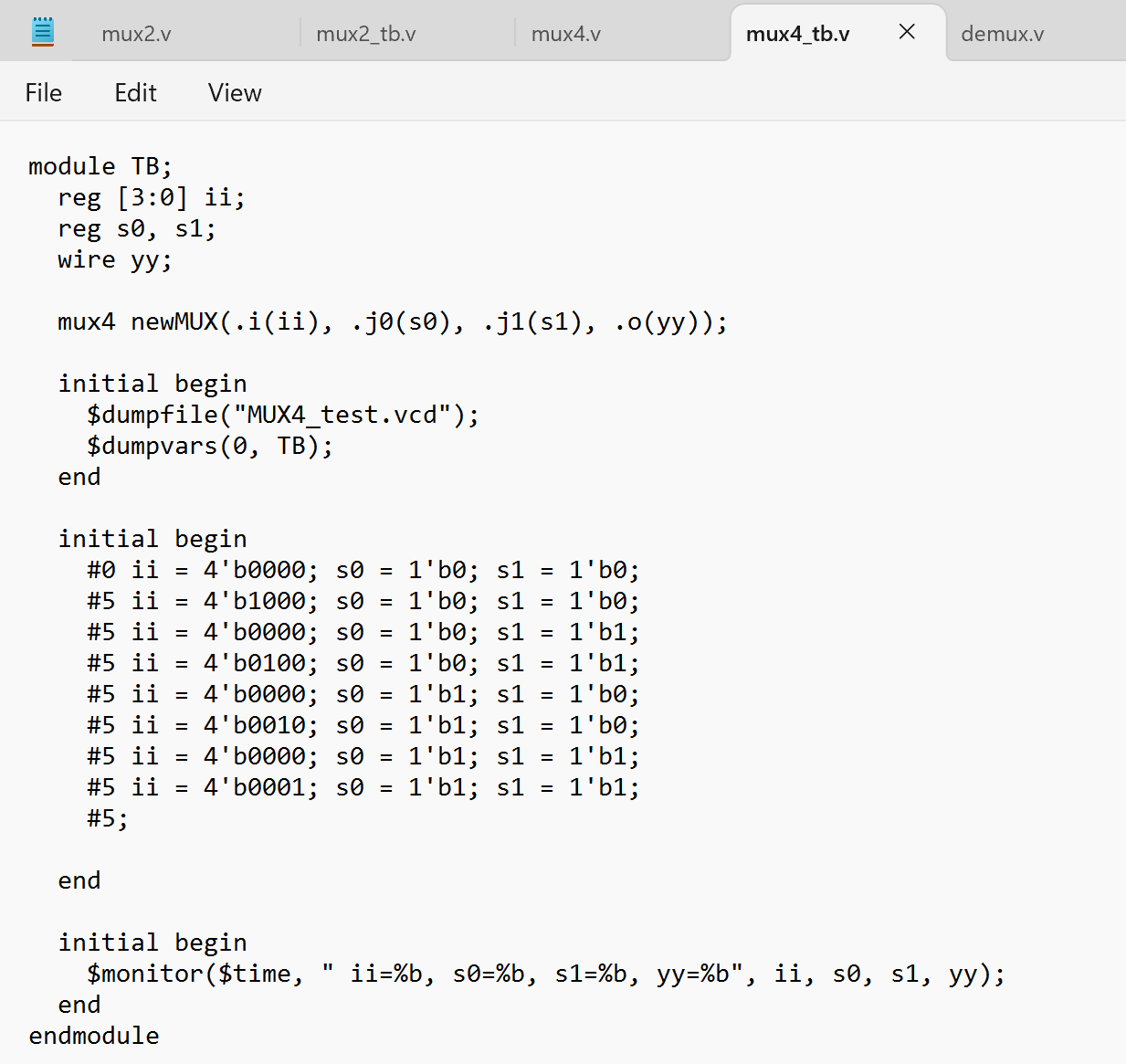
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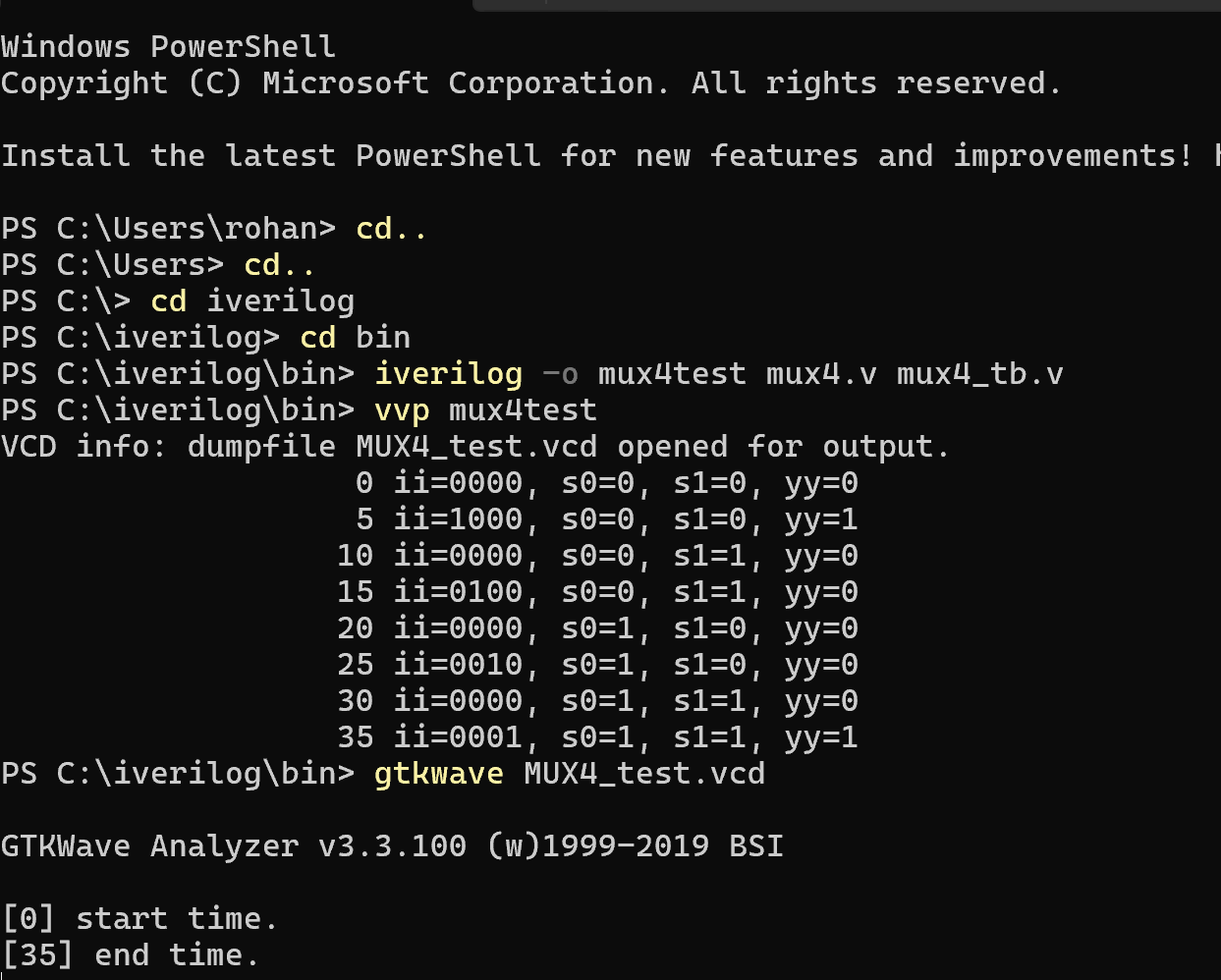
|  |  |  |  |
| --- | --- | --- | --- |
| A | B | S | X |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 |

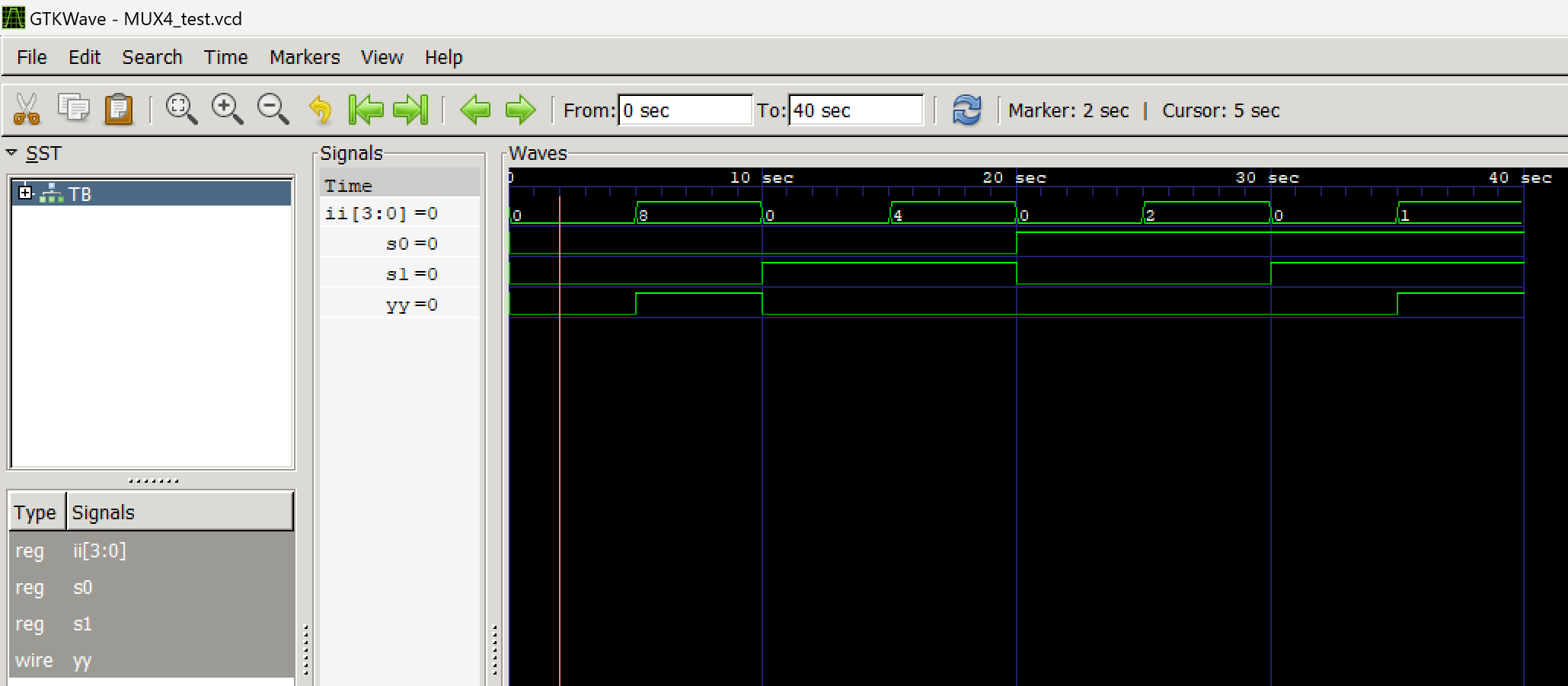
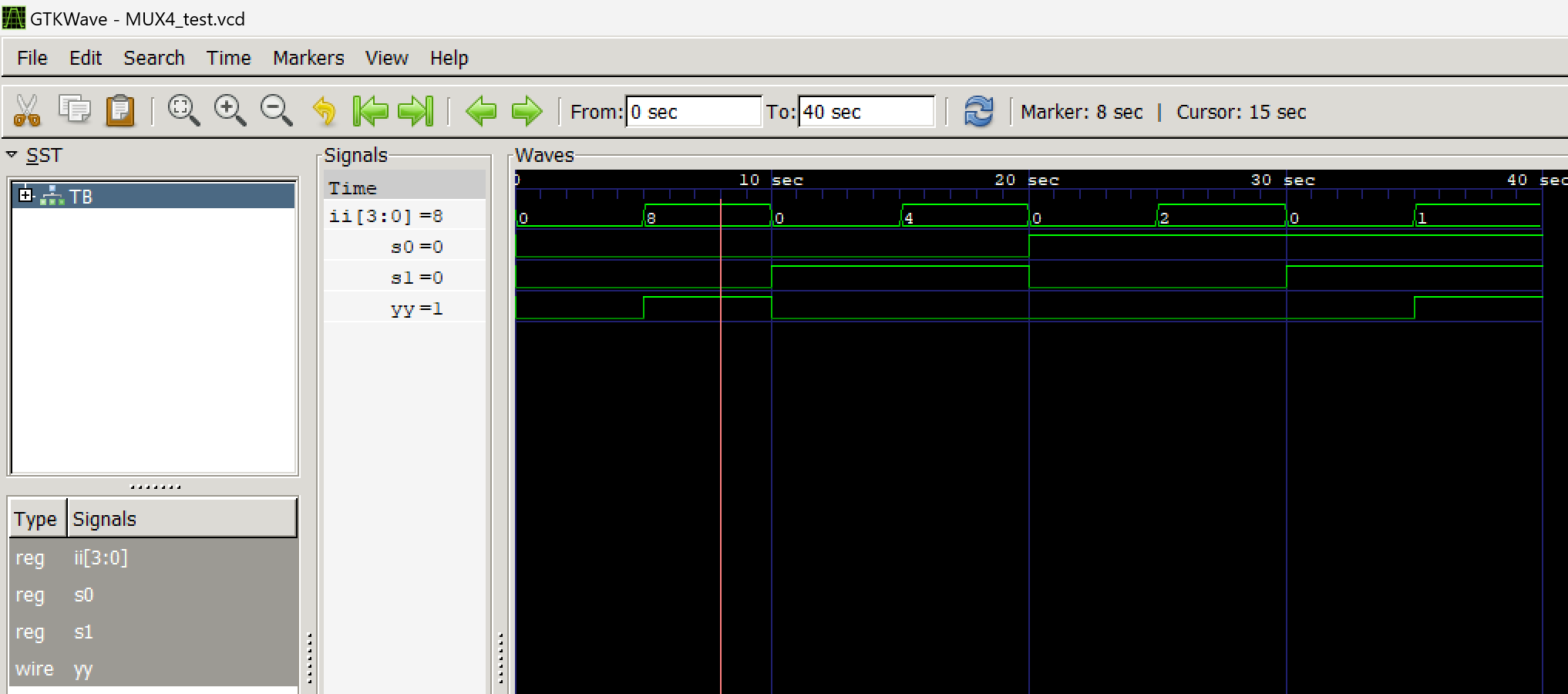
**WRITE A VERILOG PROGRAM TO MODEL A 4:1 MUX . GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE**

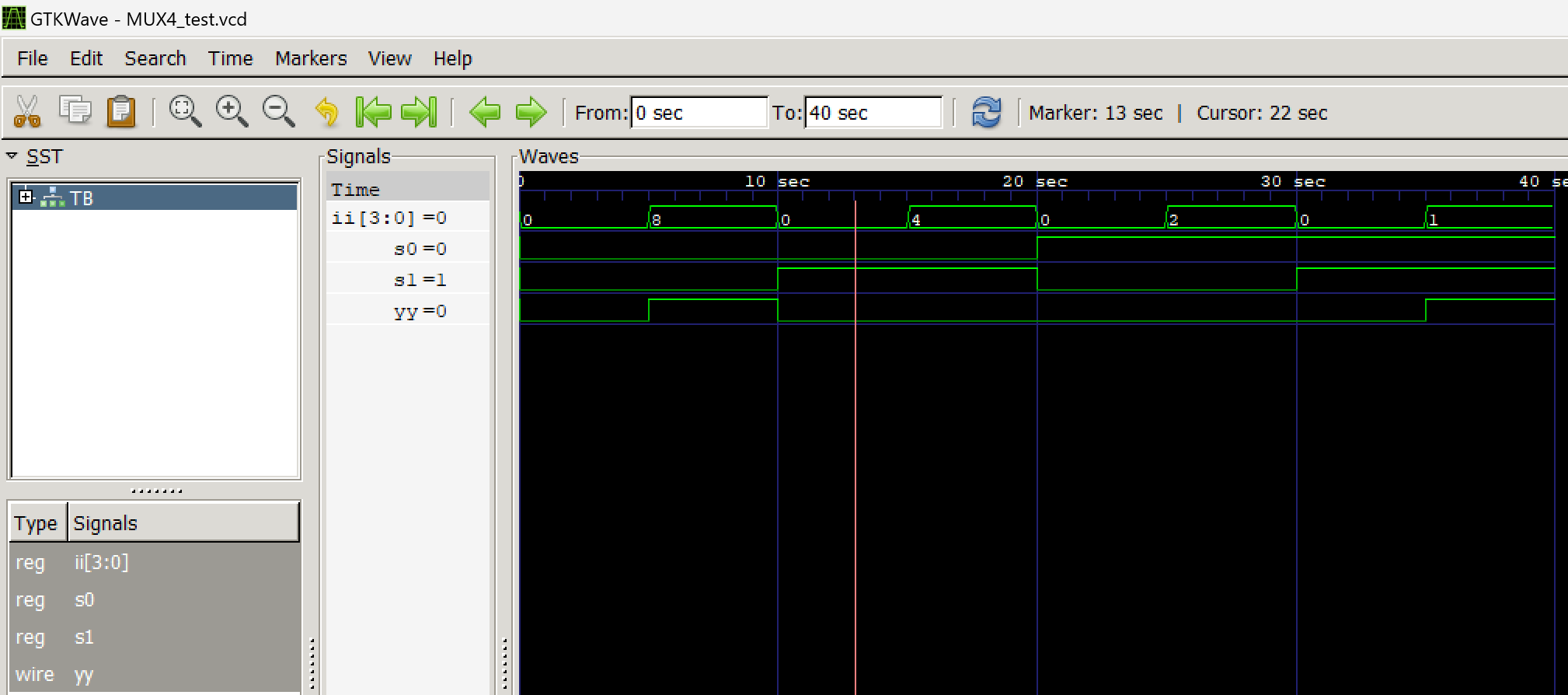
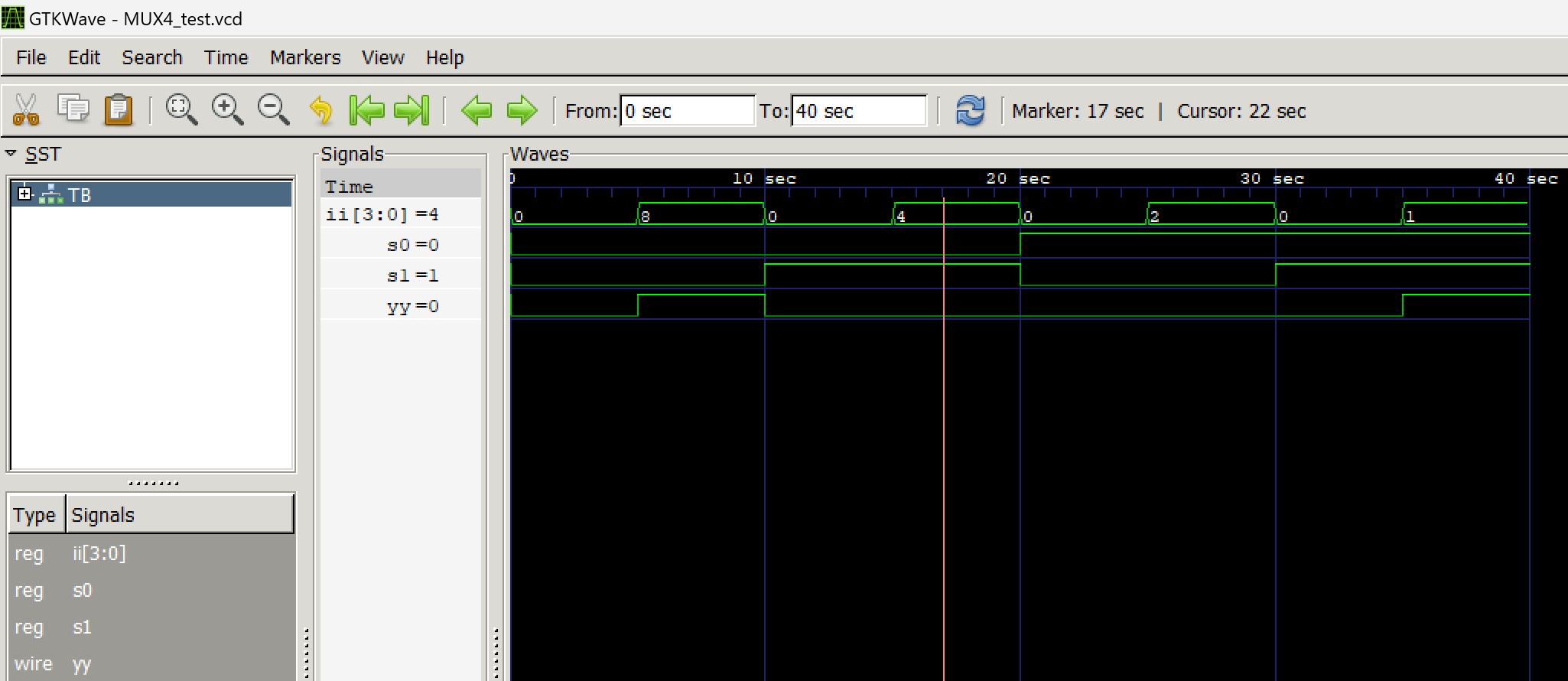
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

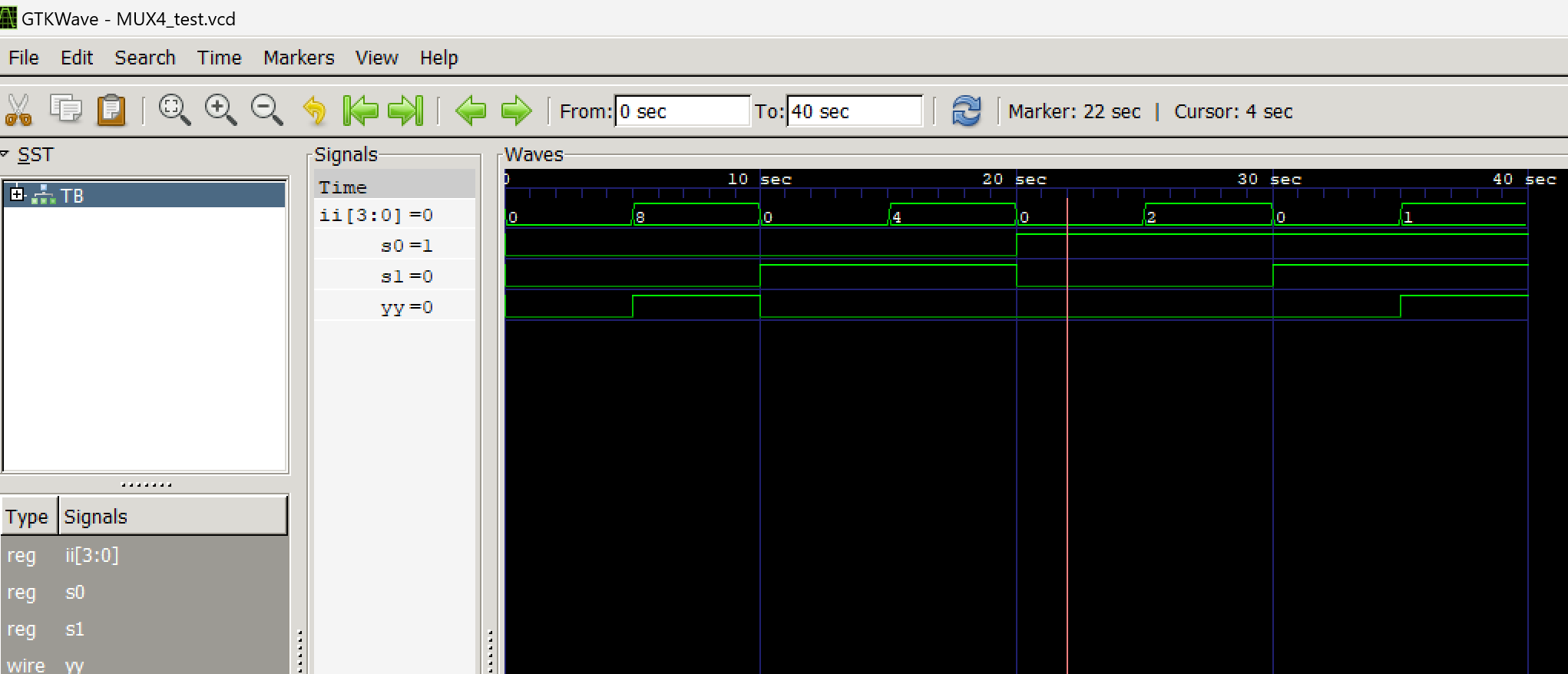


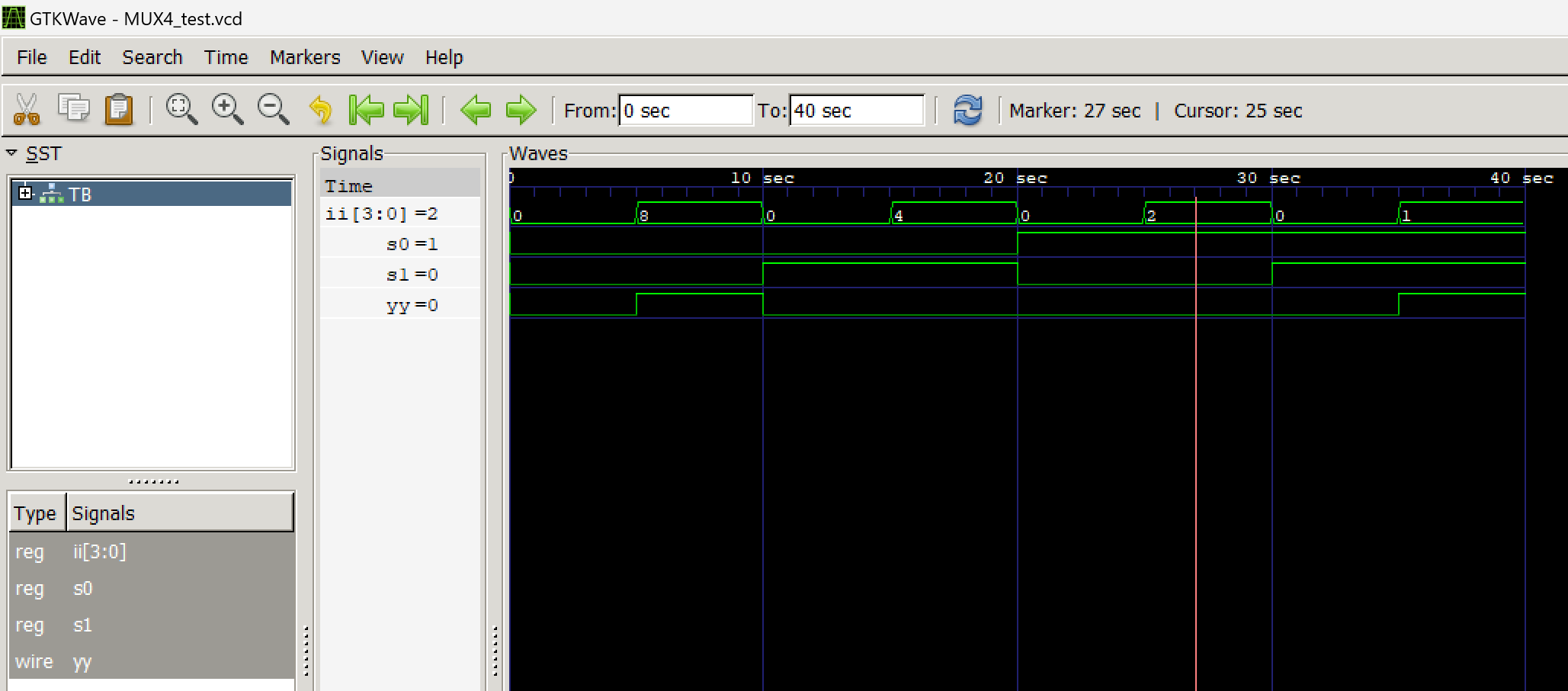
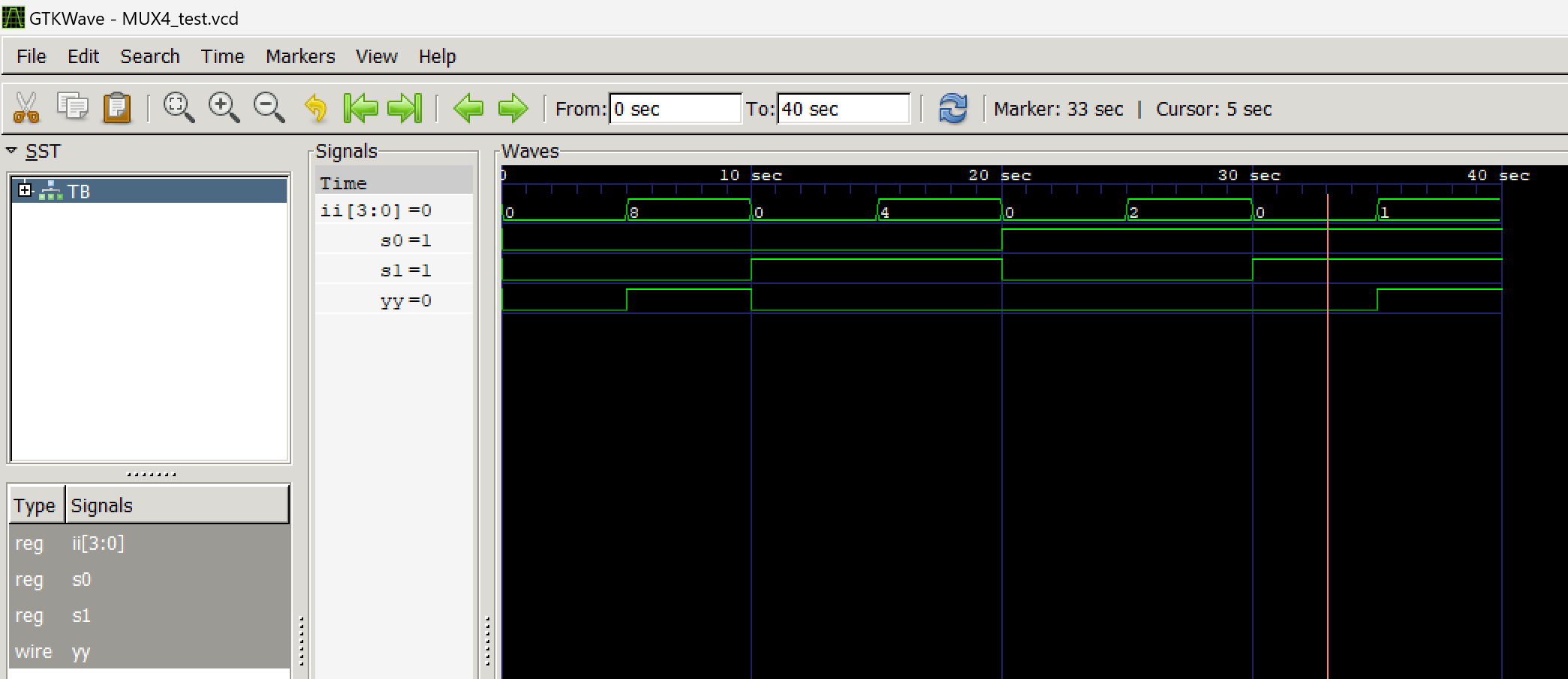
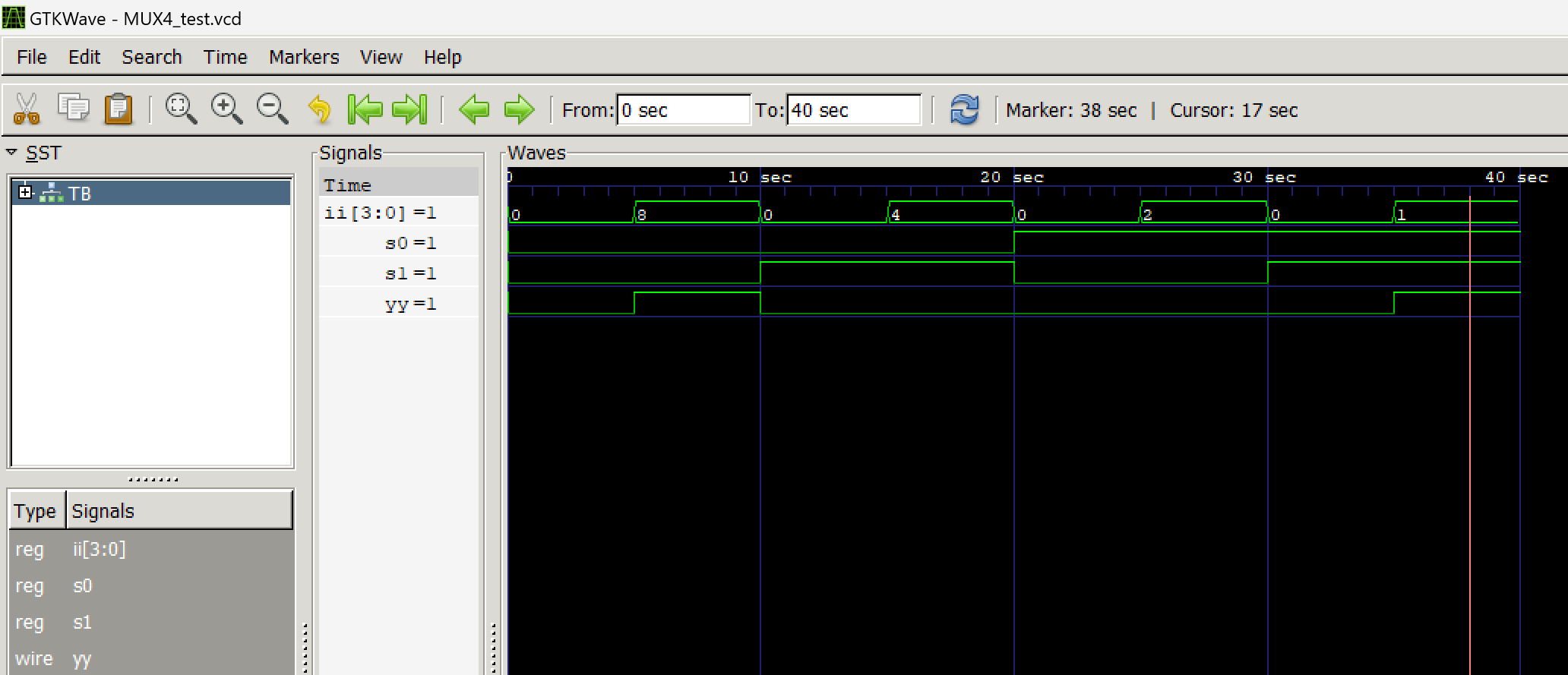


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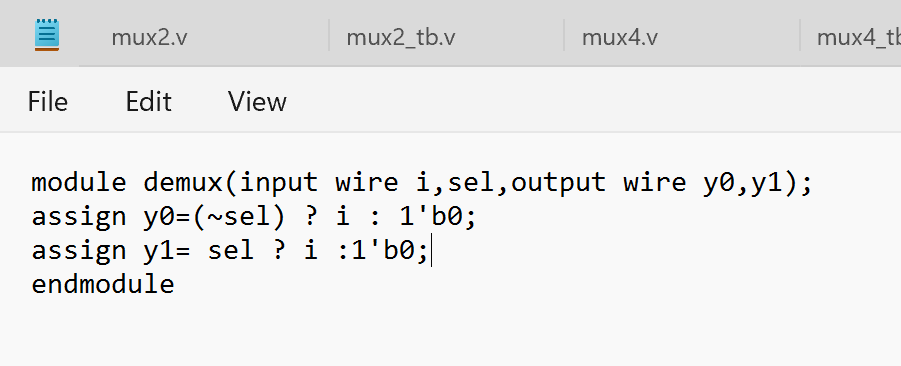
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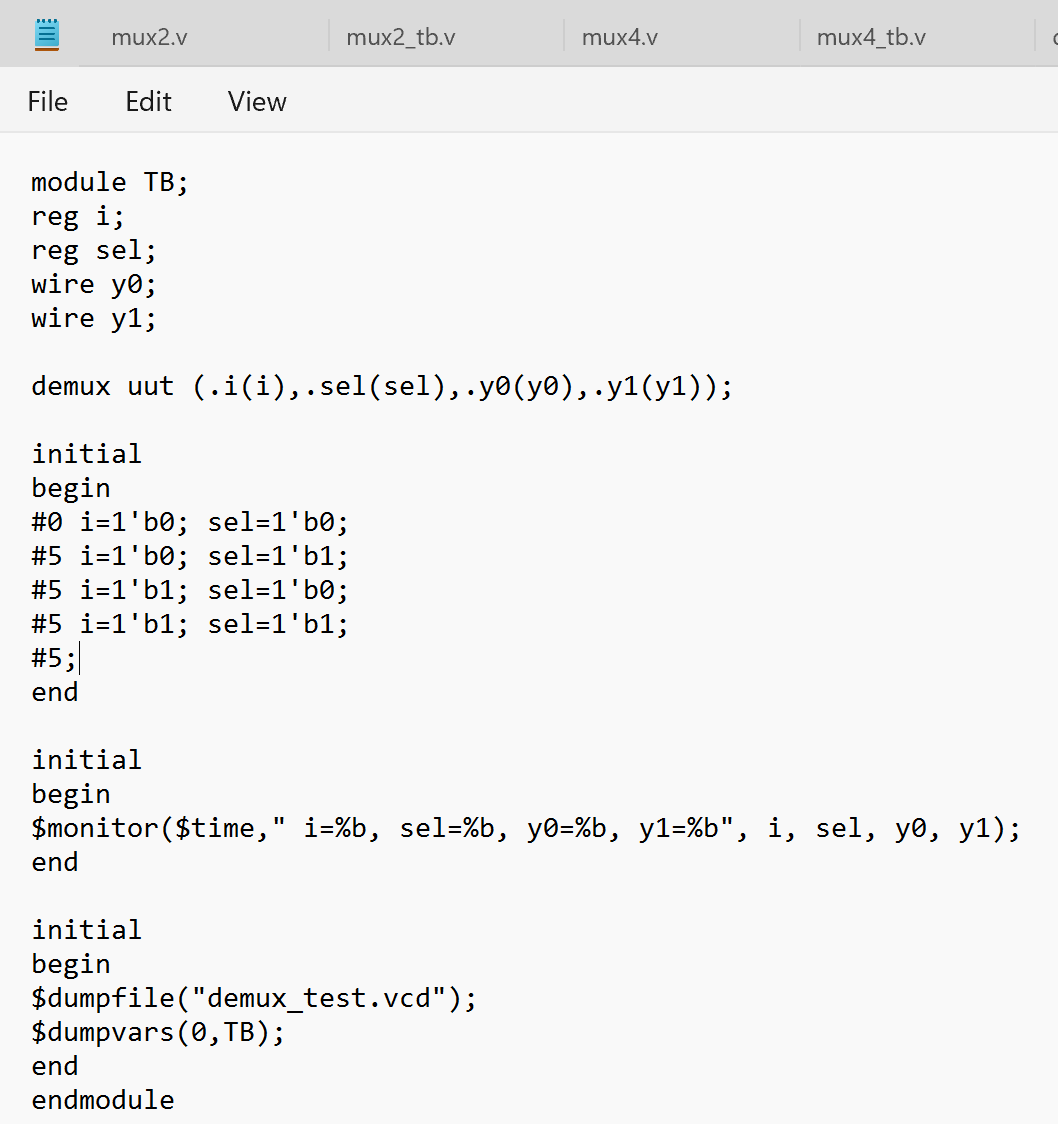
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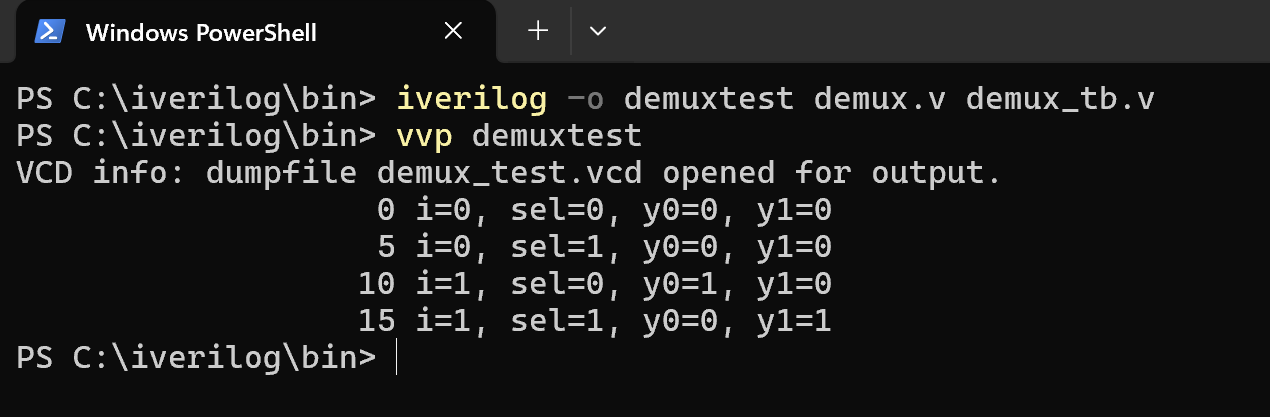
|  |  |  |  |
| --- | --- | --- | --- |
| ii | S0 | S1 | yy |
| 0000 | 0 | 0 | 0 |
| 1000 | 0 | 0 | 1 |
| 0000 | 0 | 1 | 0 |
| 0100 | 0 | 1 | 0 |
| 0000 | 1 | 0 | 0 |
| 0010 | 1 | 0 | 0 |
| 0000 | 1 | 1 | 0 |
| 0001 | 1 | 1 | 1 |

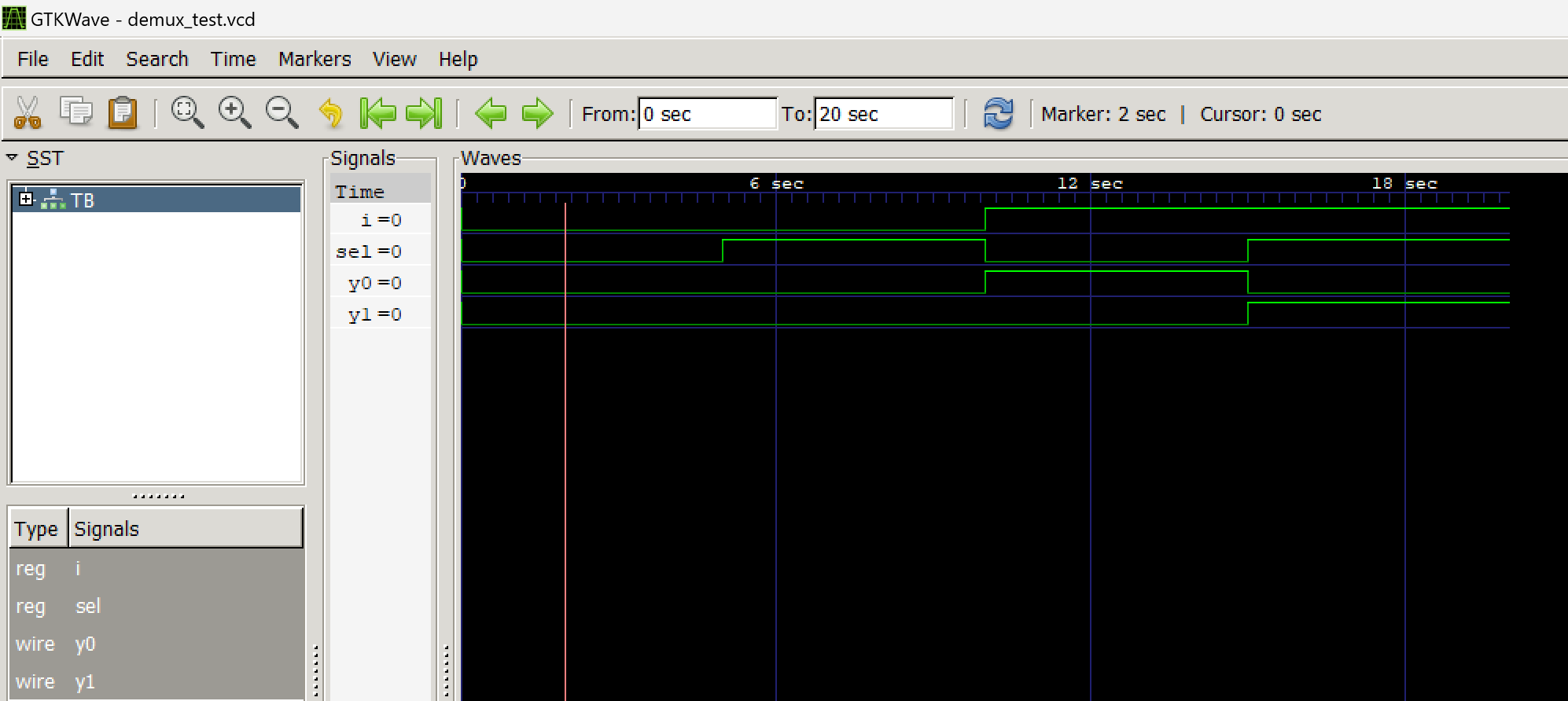
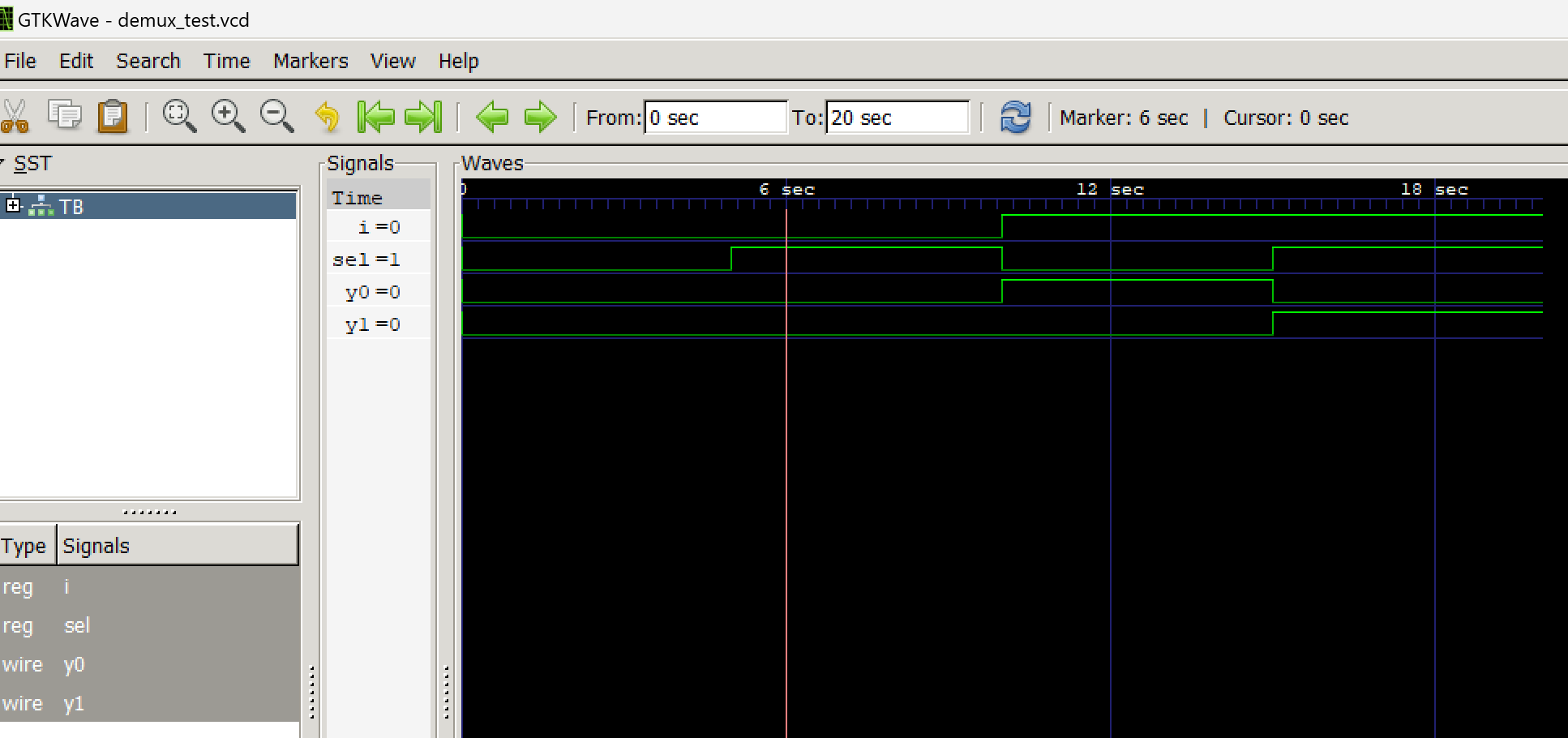
**WRITE A VERILOG PROGRAM TO MODEL A 2:1 DEMUX . GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE**

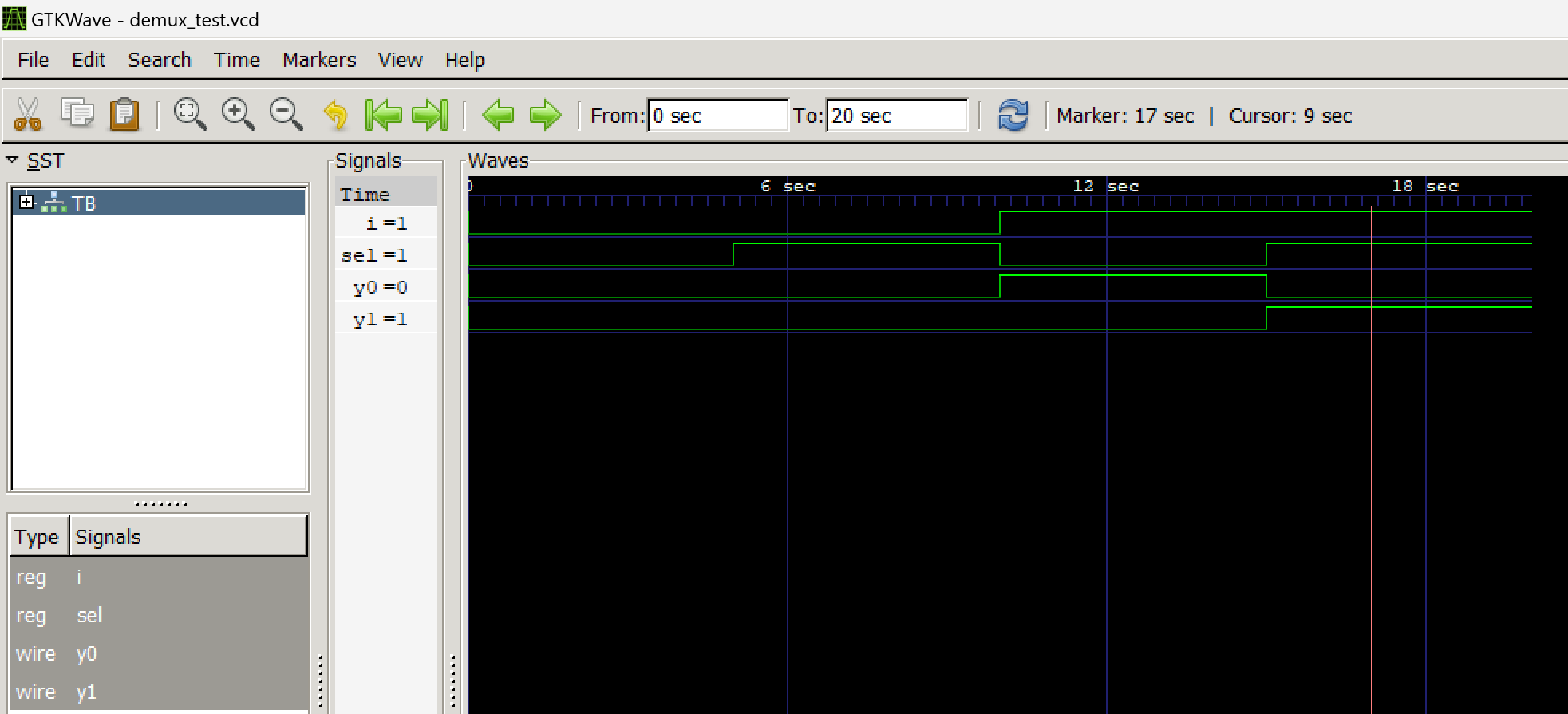
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included



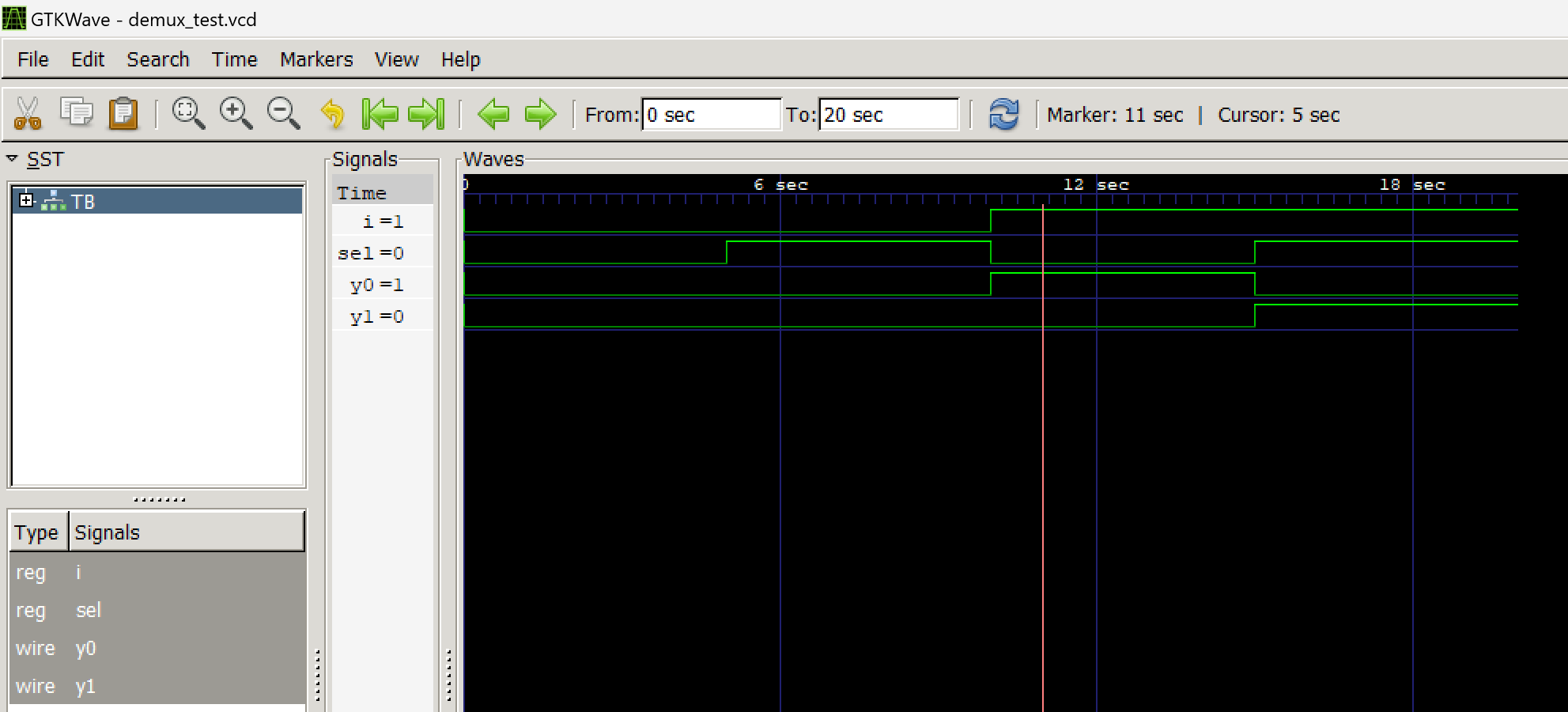
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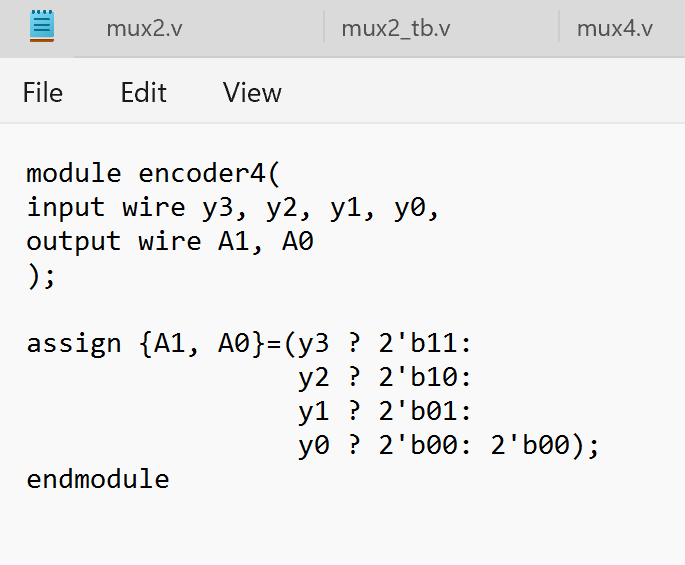
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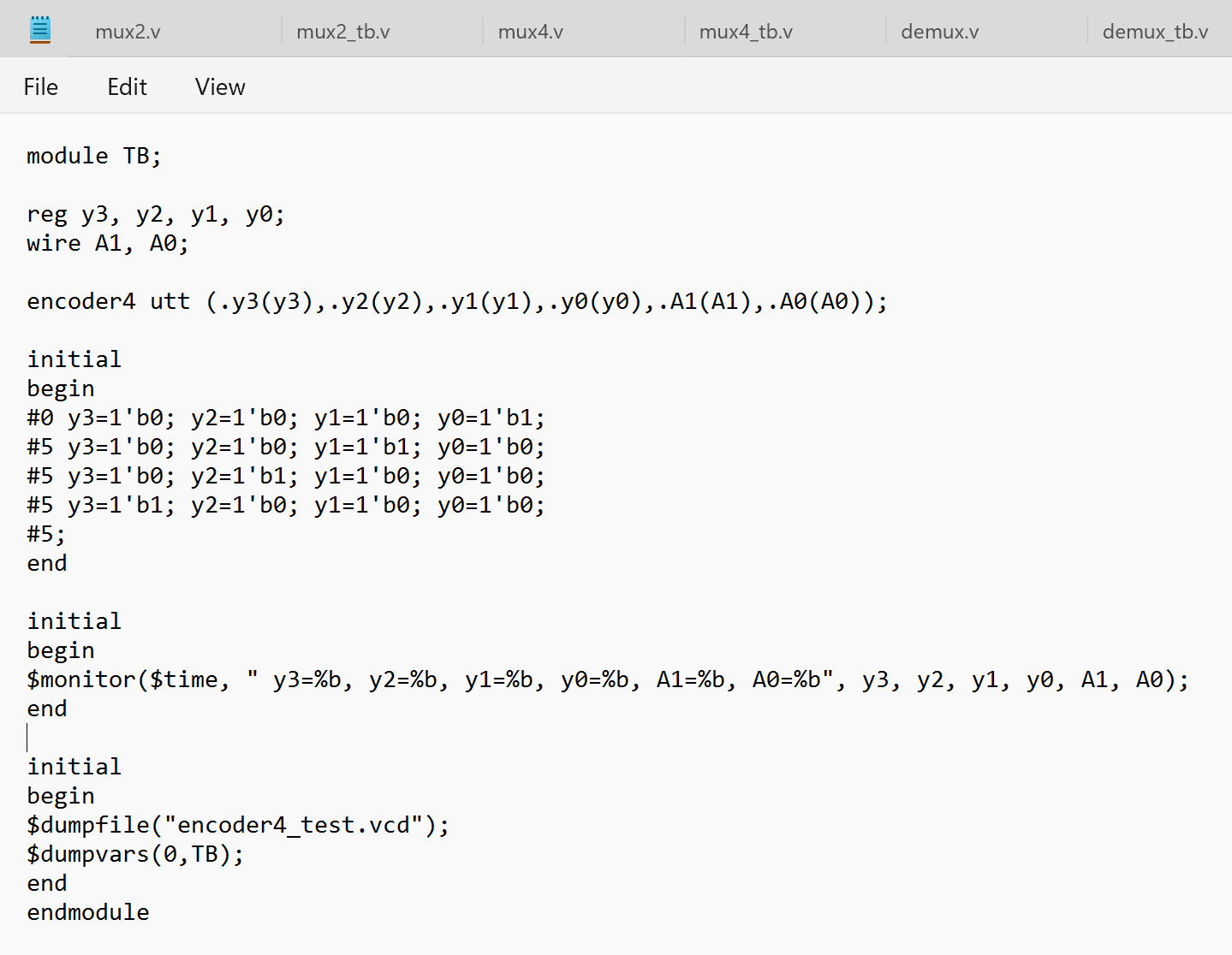
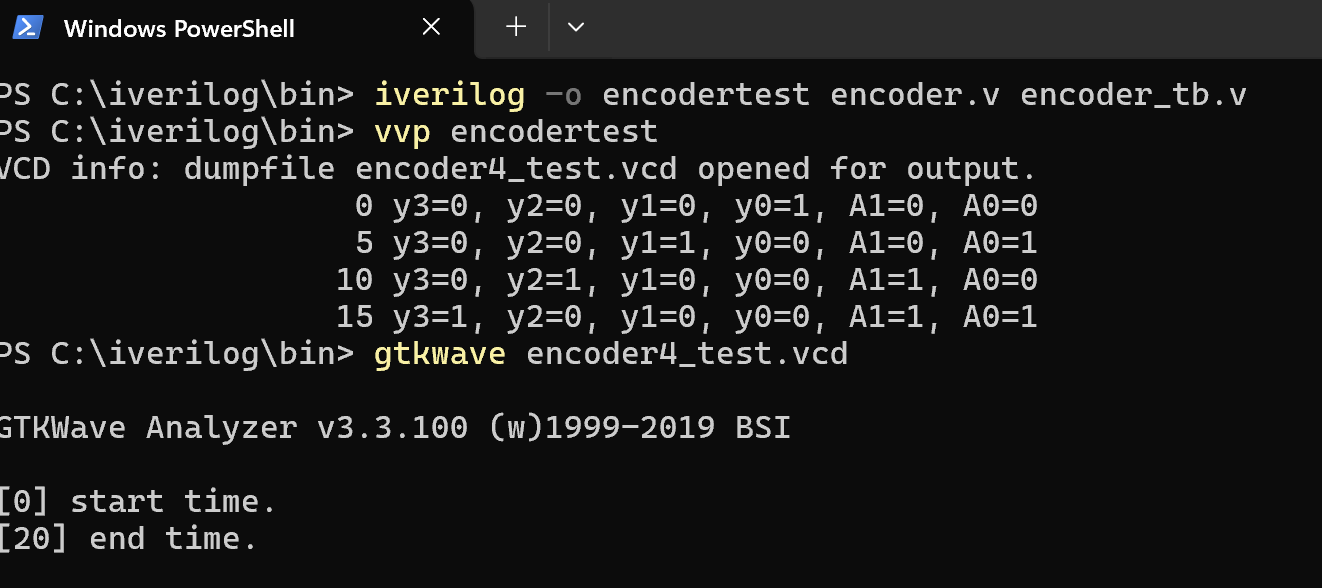
|  |  |  |  |
| --- | --- | --- | --- |
| I | Sel | Y0 | Y1 |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

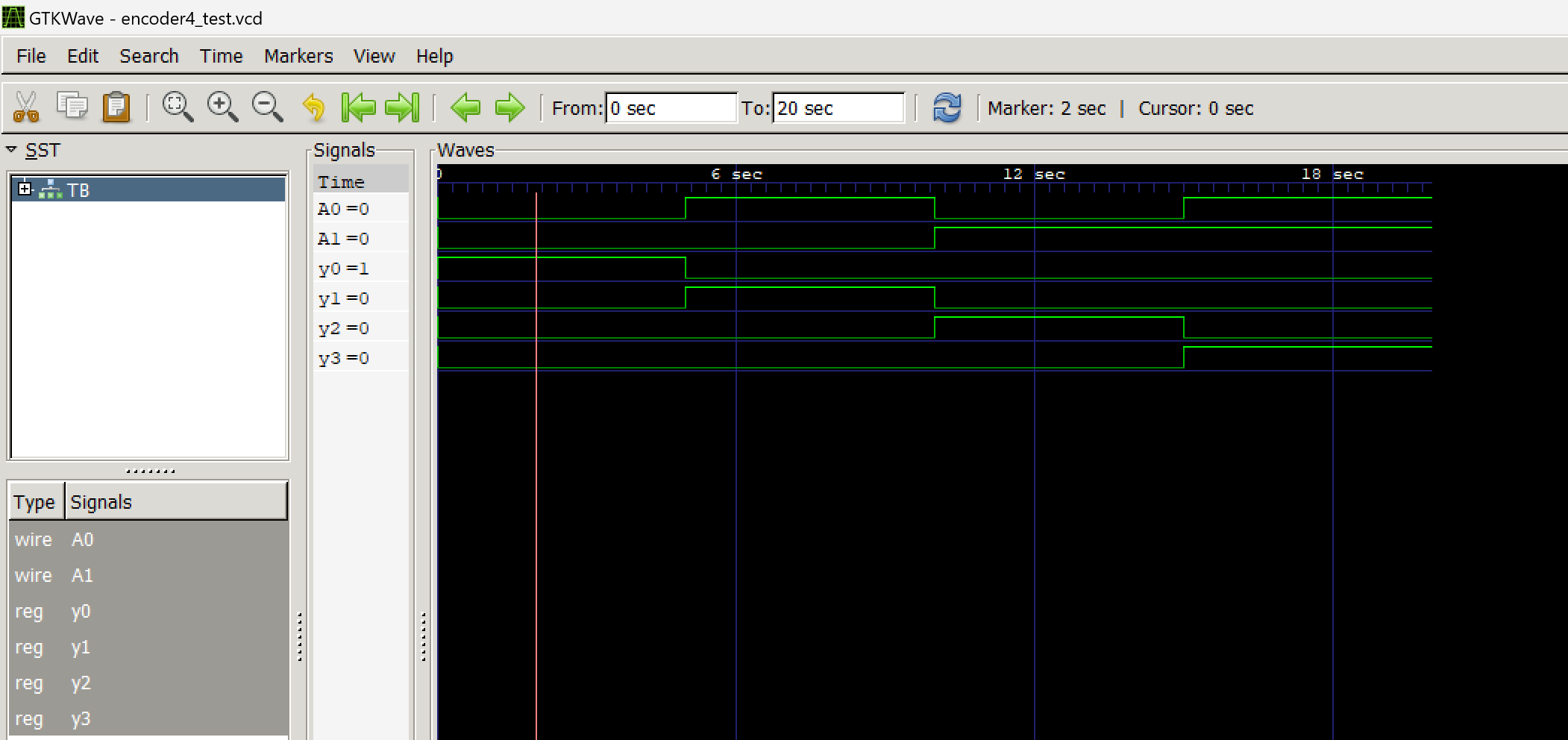
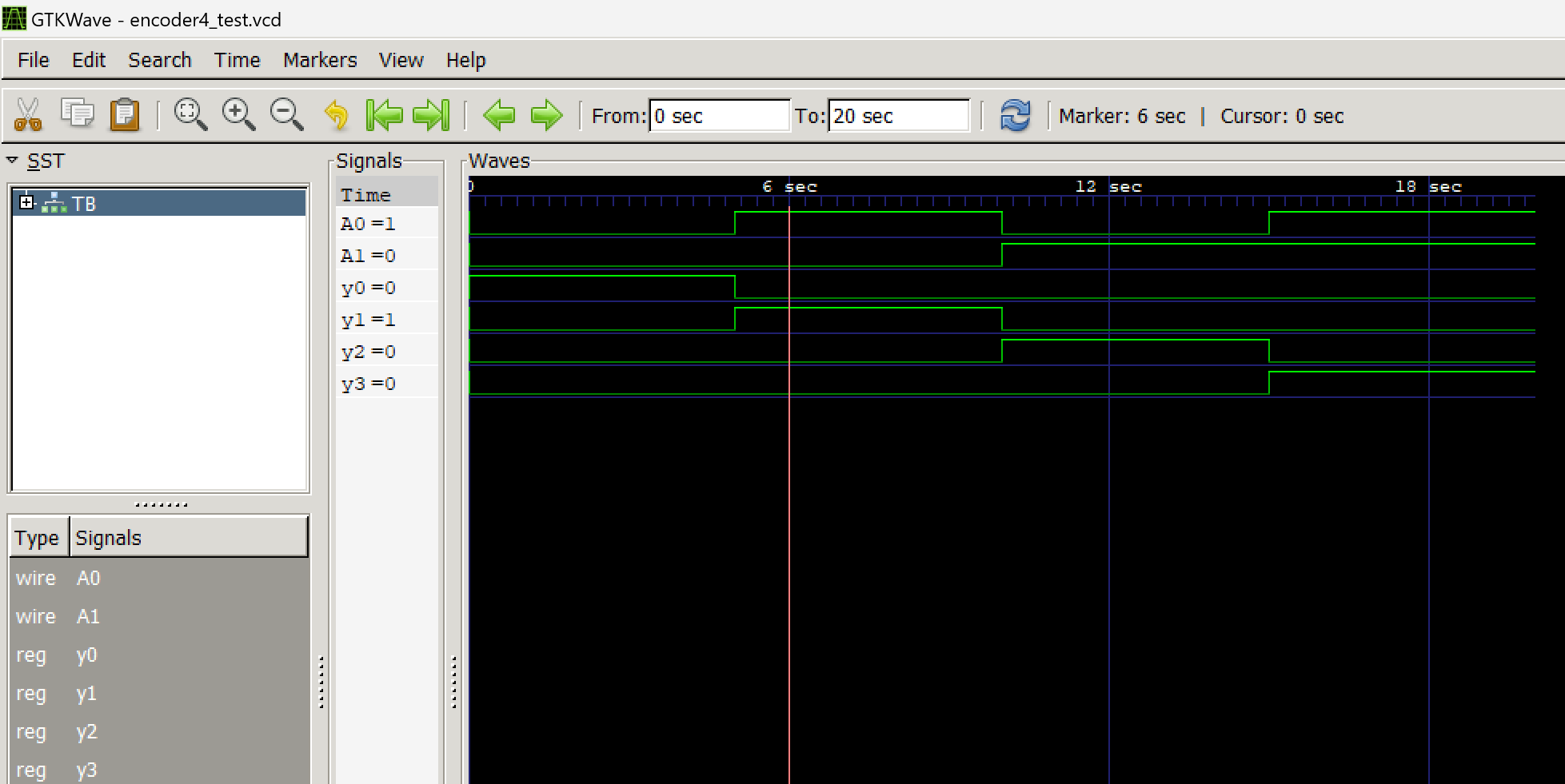
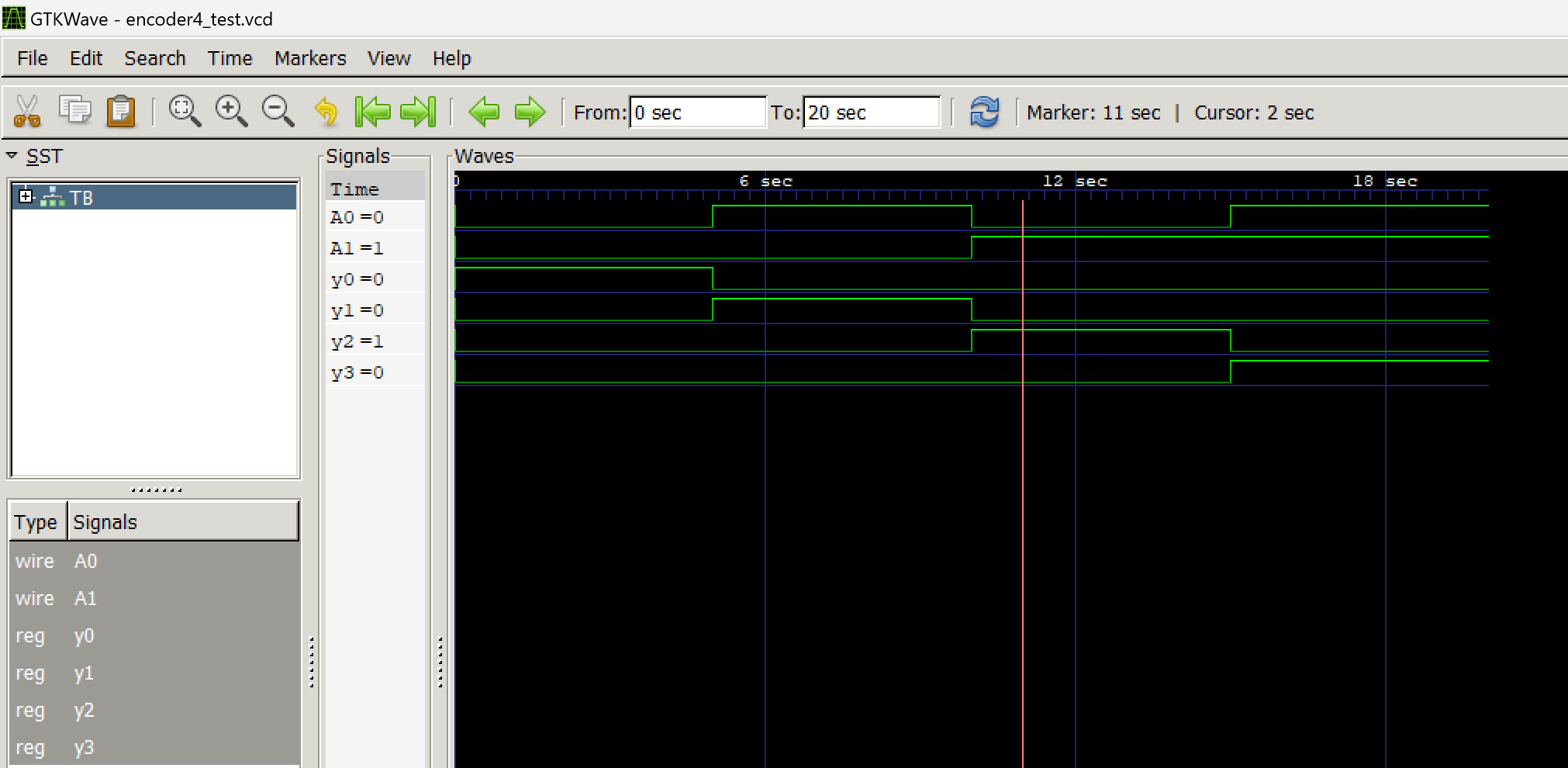
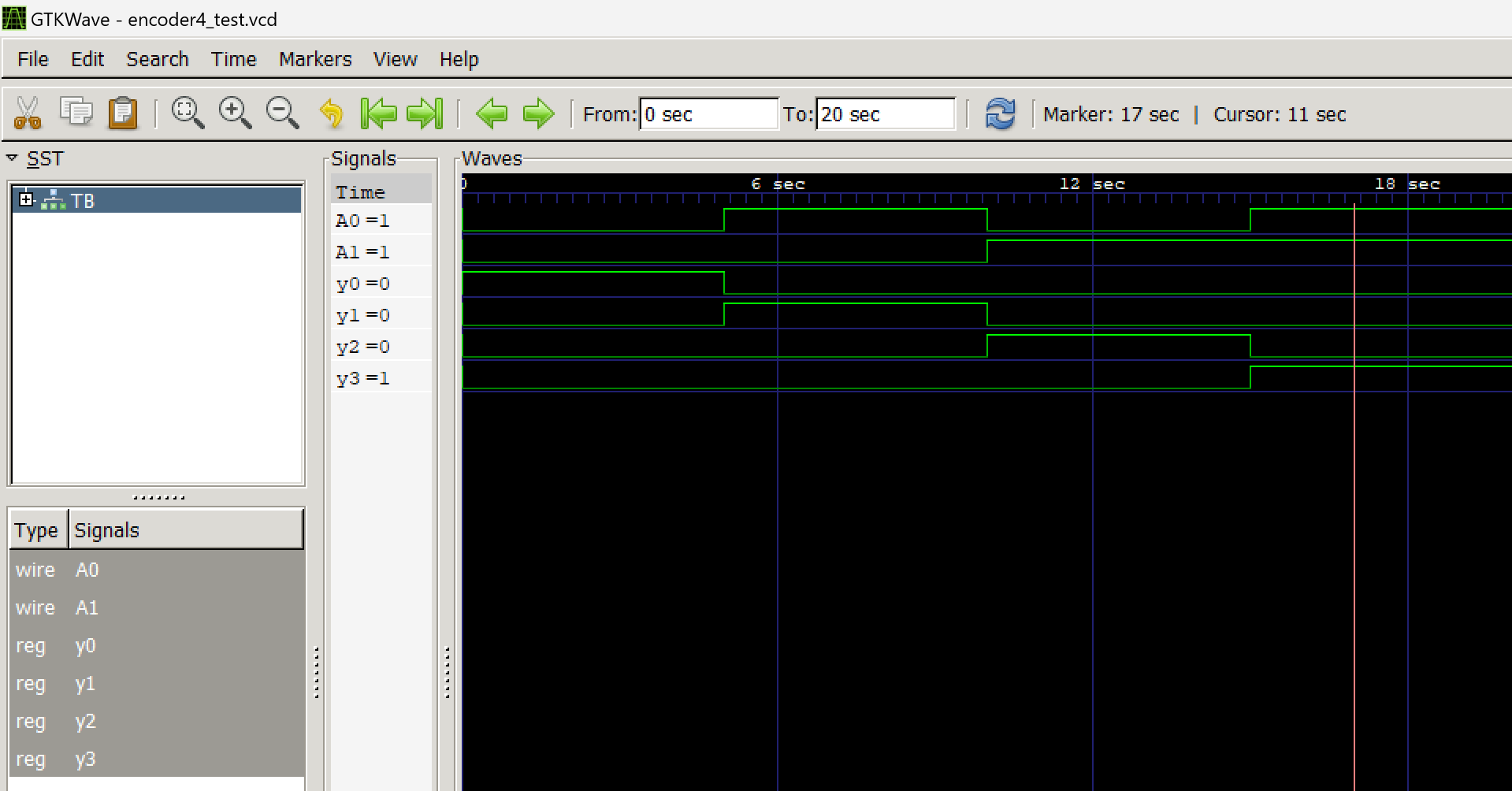


**WRITE A VERILOG PROGRAM TO MODEL A ENCODER. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE**

1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

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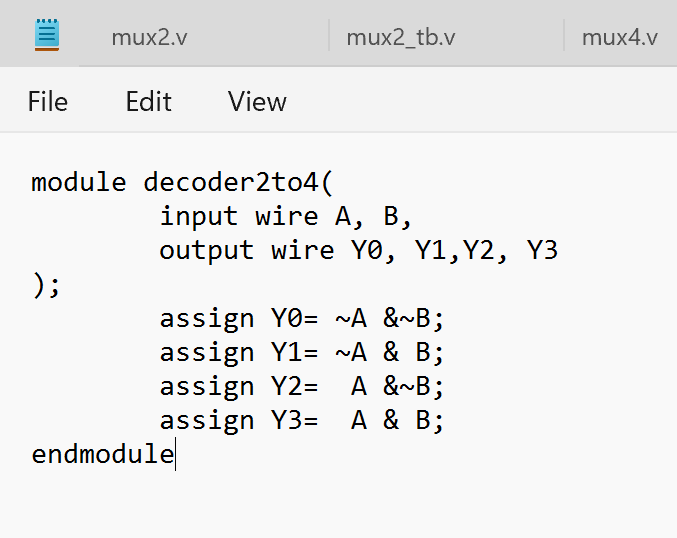
 

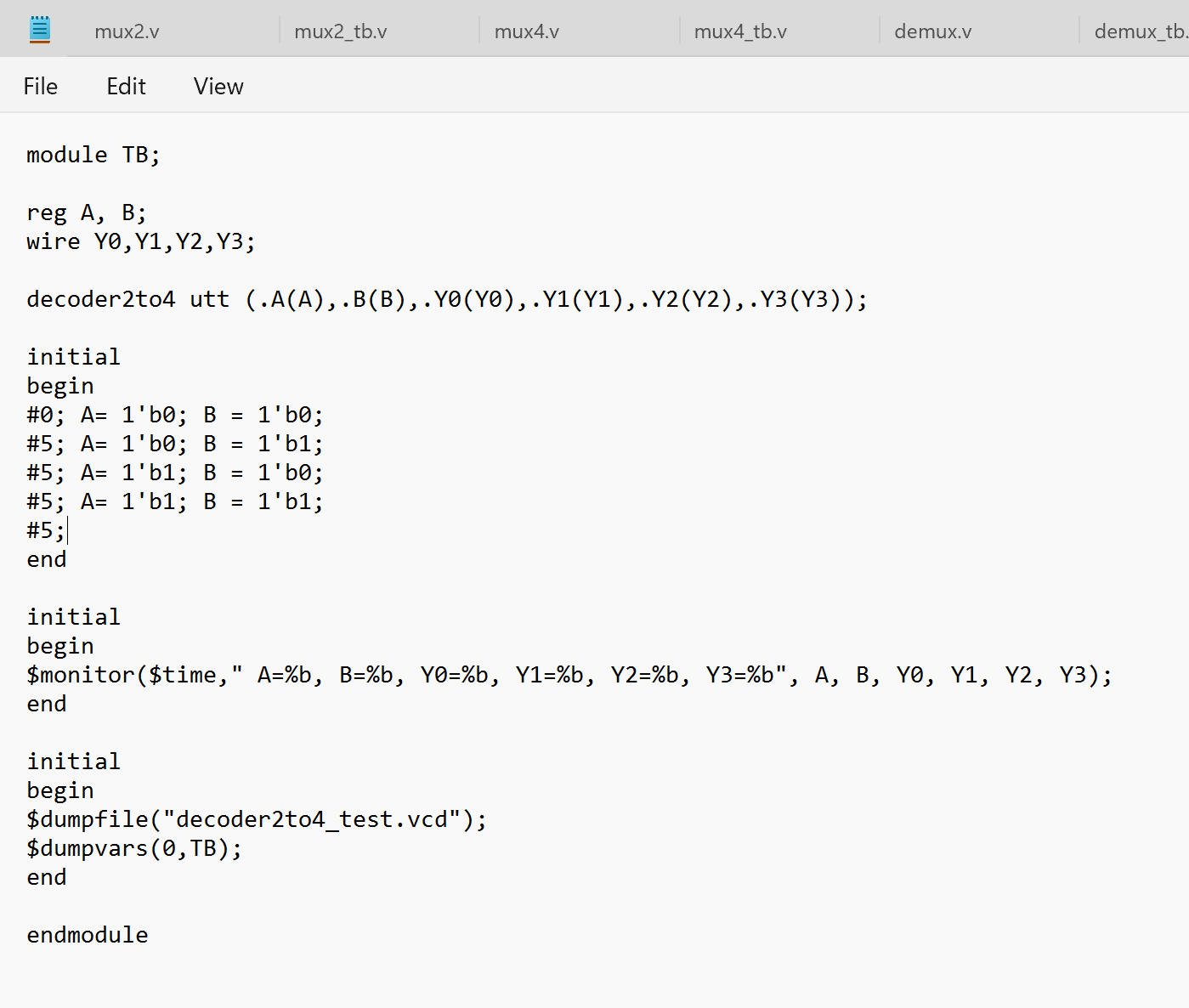
   

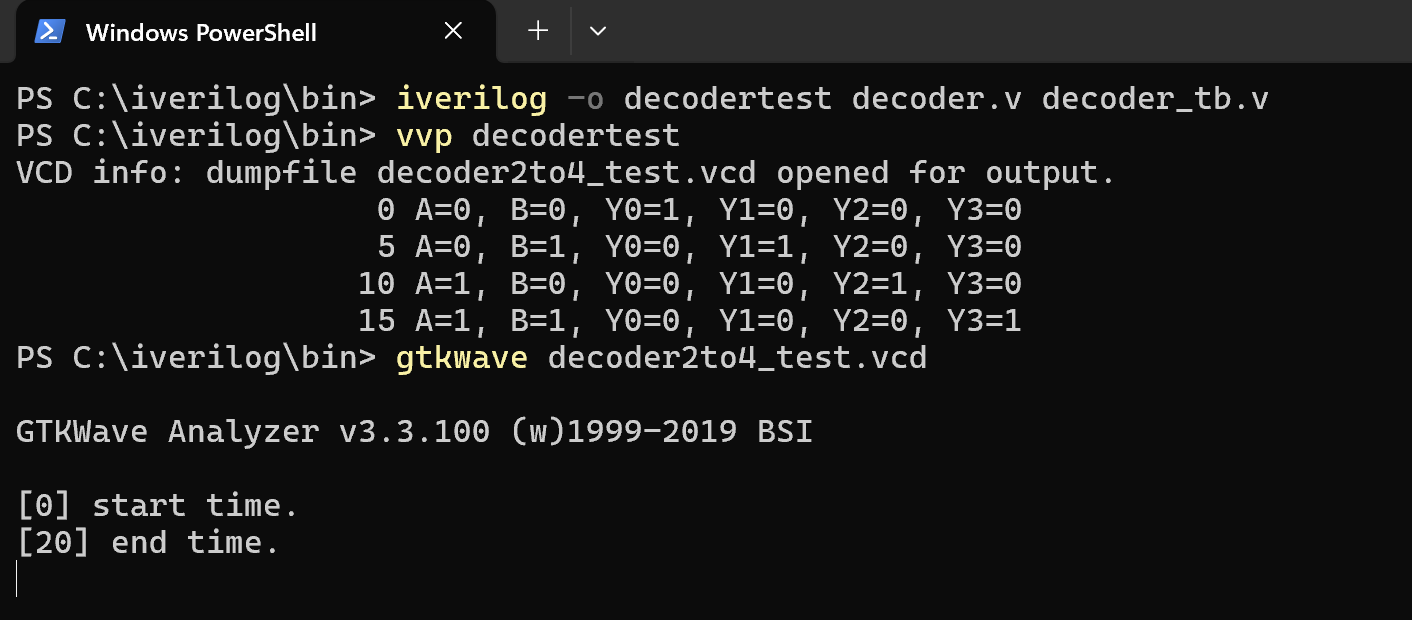
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Y3 | Y2 | Y1 | Y0 | A1 | A0 |
| 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 |

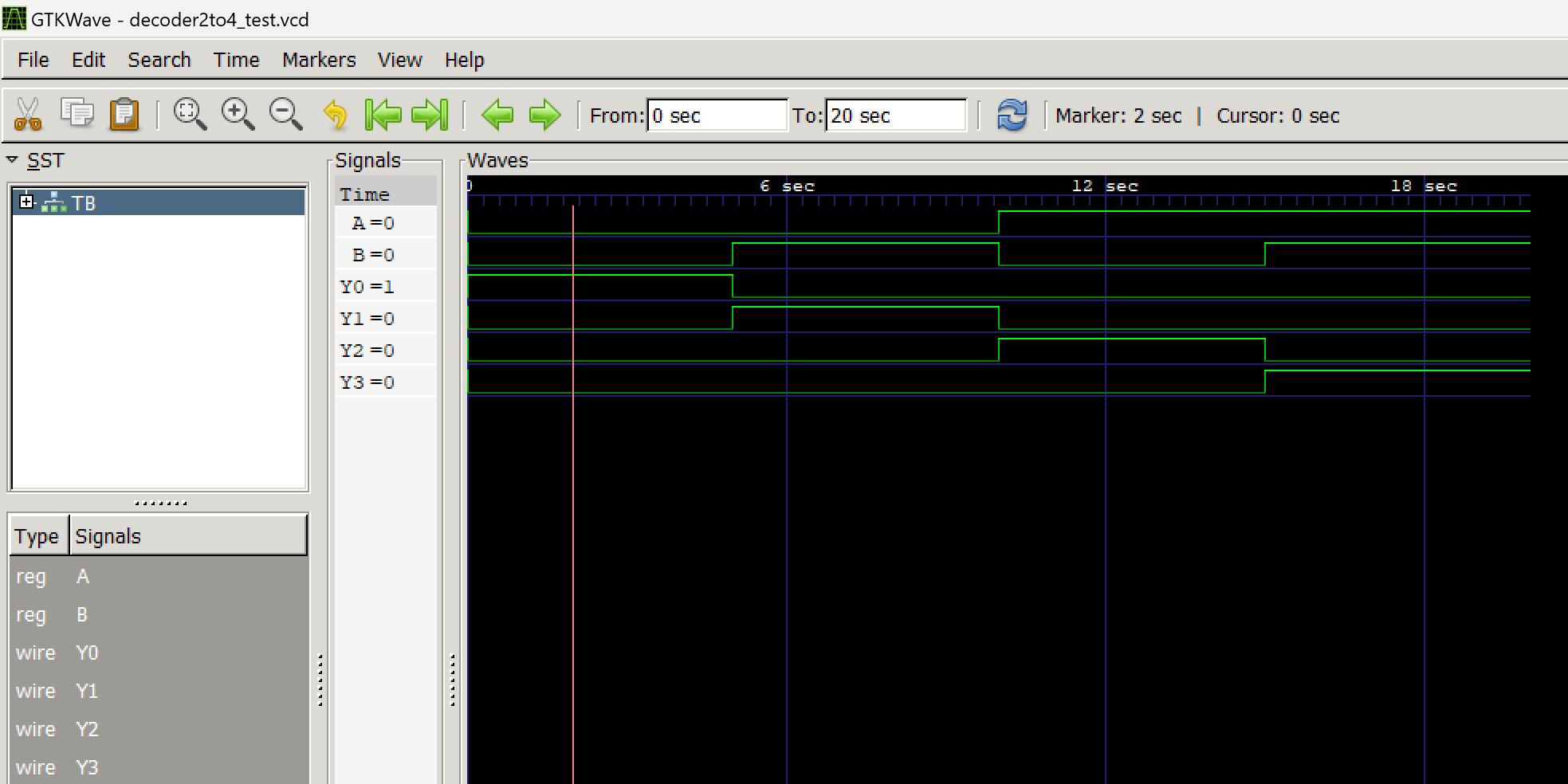
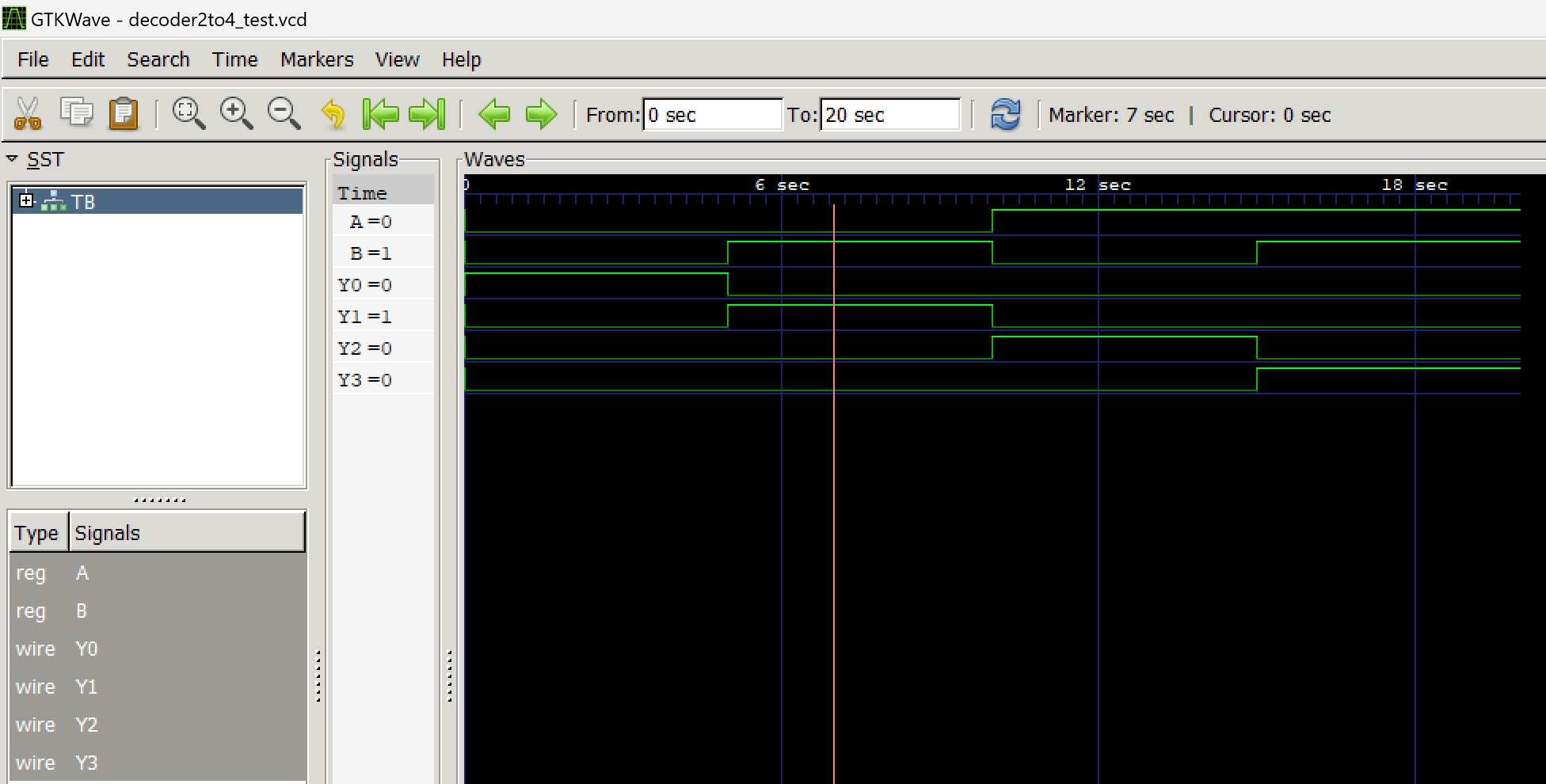
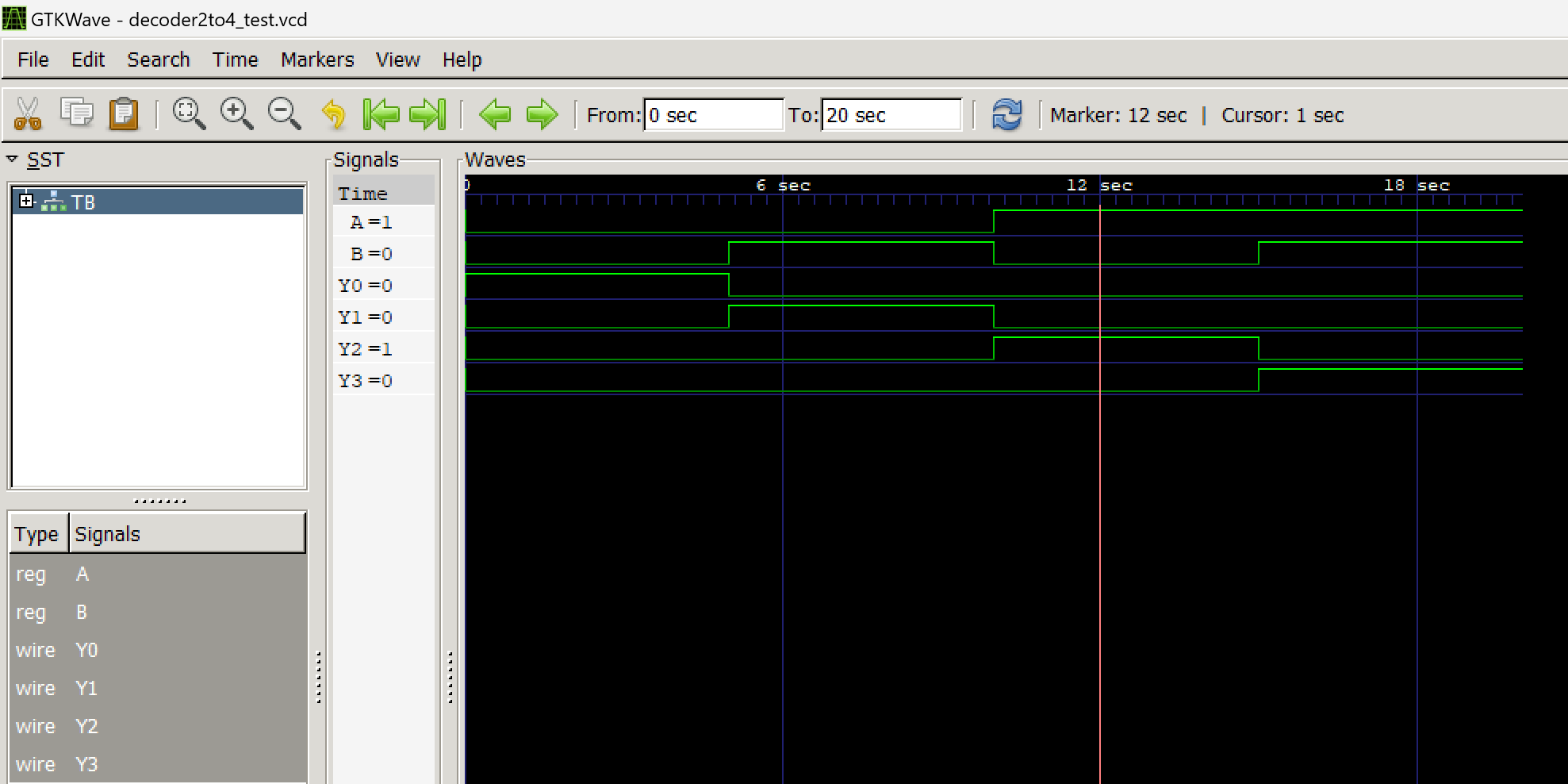
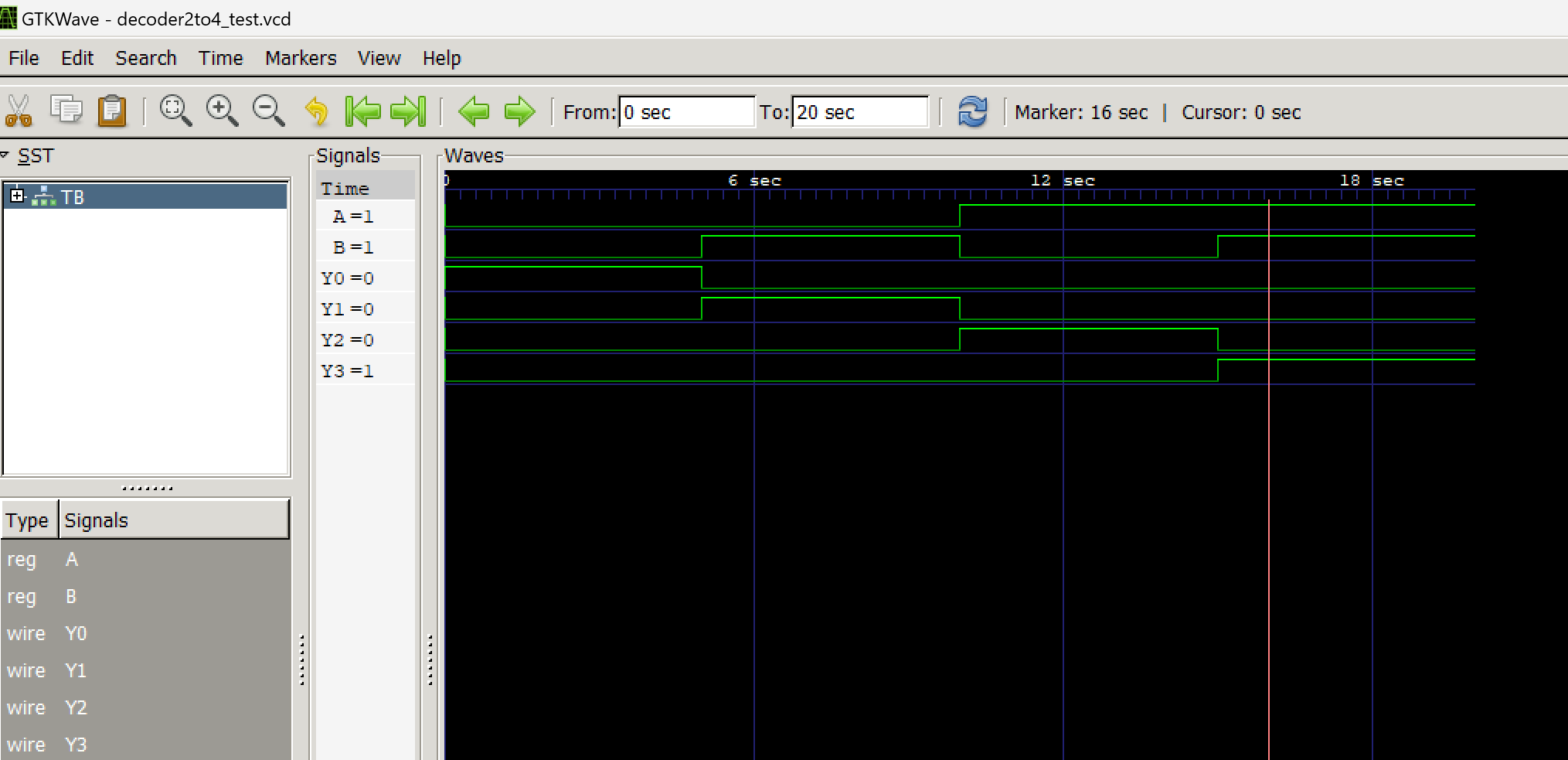
**WRITE A VERILOG PROGRAM TO MODEL A DECODER. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE**

1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included







|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A | B | Y0 | Y1 | Y2 | Y3 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |

If found plagiarized, I will abide with the disciplinary action of the University.

Name: Rohan Cyriac Suraj

SRN: PES2UG23CS490

Section: H

Date:06/09/2024