Tutor Marked Assignment #1 | 2021

- Submit your written assignment to the drop box provided in the Moodle on or before **11th July 2022**; late submissions will not be accepted!
- Clearly show your assumptions, if any, when you answer the questions.

[Q1] Consider the following Boolean functions F1, F2, F3 and F4. 3,5,9,7

F1 (w, x, y, z) = Σ(0, 1, 5), F2 (w, x, y, z) = Π(*a, b, c, d*)

F3 (w, x, y, z) = Σ(2, 6, 10, 12, 14, 15), F4 (w, x, y, z) = Σ(*a, b, c, d*)

Where *a, b, c,* and *d,* are the last four digits of your registration number.

(a) Draw the K-map for F1, F2, F3, F4 and find optimize expressions for F1, F2, F3, F4.
(b) Draw truth tables for the above expressions.
(c) Draw circuit diagrams to realize the same functions by using the following PLDs. (Clearly, show the size of the each PLD)

(i) ROM (ii) PLA (iii) PAL

(d) Compare and contrast each implementation above.

[Q2]

(a) Draw a timing diagram and show how the propagation delay affects the T-Flip Flop using an example. (Clearly, show the propagation delay, setup time, hold time, and clock period of your example).
(b) Hence derive the equations showing the relations between propagation delay, setup time, hold time, and clock period.
(c) Figure 1 depicts a network which has inputs (X, T_A) and output (Q_A, Q'_A) as below. Where; HIGH to LOW propagation delay (t_{PHL}) = 100 ns, LOW to HIGH propagation delay (t_{PLH}) = 60 ns, set-up time (t_{SU}) = 20 ns, hold time (t_H) = 0 ns, maximum clock frequency (f_{CLKMAX}) = 10MHz.

Draw a timing diagram for the network showing X, T_A, Q'_A. Assume that X is initially 1 and X becomes 0 for 10 ns, then X becomes 1 for 180 ns. Clearly, state other assumptions, if any.

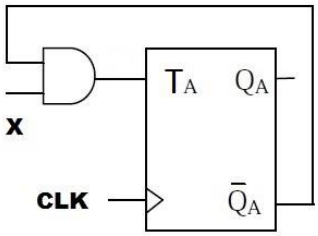

Figure 1

[Q3]

(a) Draw a block diagram of the 1-bit Full Adder (FA).
(b) Implement the data flow model of the 1-bit FA using the VHDL program.
(c) Write the Test Bench model for the 1-bit FA.

[Q4]

(a) Draw a block diagram of the 4-bit FA using 1-bit FAs.

(b) Implement the data flow model of the 4-bit FA using the VHDL program.

(c) Write the Test Bench model for the 4-bit FA.

[Q5]

(a) Briefly explain the method of integrating propagation delay into your VHDL simulation.

(b) Modify the Test bench written in Q5.c with suitable delays.

(c) Modify the same test bench written in Q5.c with a file I/O. You may use text files to read inputs and write output signals.