Tutor Marked Assignment #2 | 2021

- Submit your assignment on or before **14th September 2022,** and late submissions will not be accepted!
- Clearly show your assumptions, if any, when you are answering the questions.
- Refer to Moodle's learning resources (VHDL video lectures) before answering the questions.
- Use Xilinx web pack/Active HDL/Modelsim software to write a VHDL program. (You can get a copy of this software from the laboratory)

[Q1]

(a) Draw an Algorithmic State Machine (ASM) chart for the state table in Table Q1.

(b) Construct the circuit for the state table shown in Figure Q1 using digital logic gates and D-Flip Flops.

Table Q1: State Table

Present State	Next State (AB)				Output
	00	01	10	11	z
S1	S1	S3	S2	-	0
S2	S2	S4	S5	-	0
S3	S3	S2	S4	-	0
S4	S1	-	-	-	1
S5	S3	-	-	-	1

(c) Write VHDL code to implement the circuit above.
(d) Write test bench for the above circuit.

[Q2] Design a Sequence detector for detecting 011 with overlapping and non-overlapping sequences using Mealy and Moore machines. Include the followings

(a) State Diagrams (b) ASM Charts (c) State Table (d) K-Maps
(e) Circuit Diagrams (f) VHDL Code for data flow model (g) Comparison

[Q3]

(a) Briefly explain each digital testing phase in a VLSI design flow using an illustration.
(b) Briefly explain functional and structural testing with the fault model by considering the above circuit diagram Q1.(b).

[Q4]

(a) Briefly explain the path sensitisation method using the above circuit diagram Q1.(b).
(b) List commonly used algorithms for testing digital circuits.