

Putting Microblaze processor on Papilio One + LogiStart MegaWing

This flow explains implementing Microblaze processor based system on Papilio One Spartan 3E 500k FPGA board with Logi Start MegaWing using ISE Project Navigator.

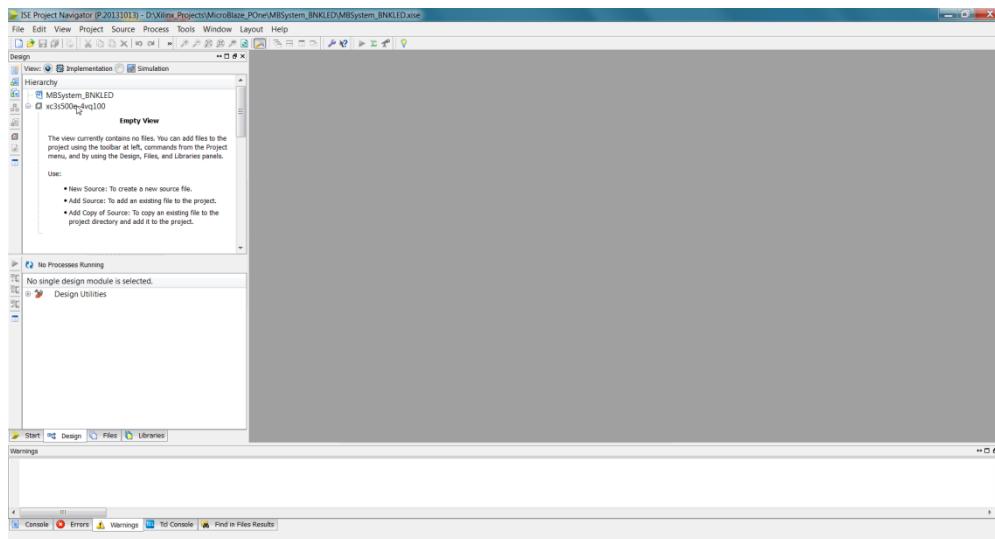
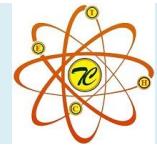
Step by Step Process:

1. Create new project *MBSystem_BNKLED* in ISE Navigator

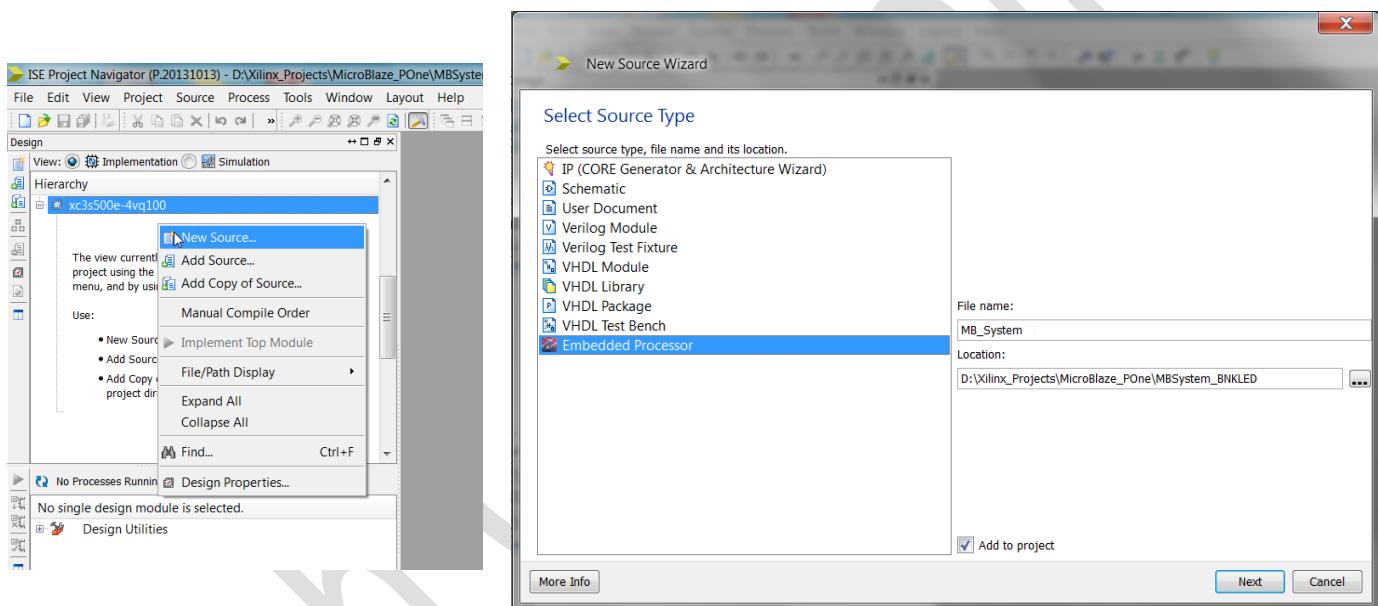
Property Name	Value
Evaluation Development Board	None Specified
Product Category	All
Family	Spartan3E
Device	XC3S500E
Package	VQ100
Speed	-4
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	VHDL
Property Specification in Project File	Store all values
Manual Compile Order	
VHDL Source Analysis Standard	VHDL-93

2. Click Next & Check summary & then click finish. This step will create new project in ISE navigator

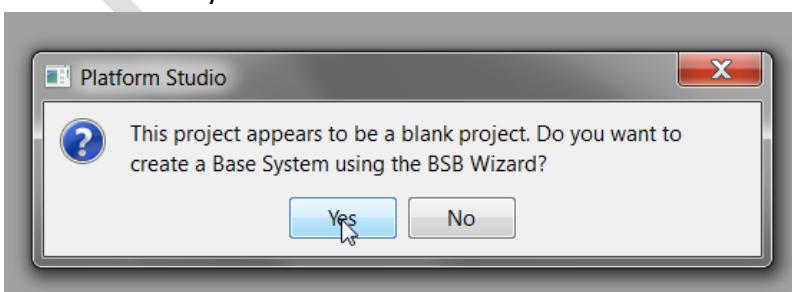
Project:	Project Name: MBSystem_BNKLED
Project:	Project Path: D:\Xilinx_Projects\MicroBlaze_POne\MBSystem_BNKLED
Project:	Working Directory: D:\Xilinx_Projects\MicroBlaze_POne\MBSystem_BNKLED
Project:	Description:
Project:	Top Level Source Type: HDL
Device:	Device Family: Spartan3E
Device:	Device: xc3s500e
Device:	Package: vq100
Device:	Speed: -4
Top-Level Source Type:	HDL
Synthesis Tool:	XST (VHDL/Verilog)
Simulator:	ISim (VHDL/Verilog)
Preferred Language:	VHDL
Property Specification in Project File:	Store all values
Manual Compile Order:	false
VHDL Source Analysis Standard:	VHDL-93
Message Filtering:	disabled

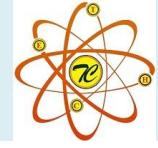


3. Create embedded processor hardware

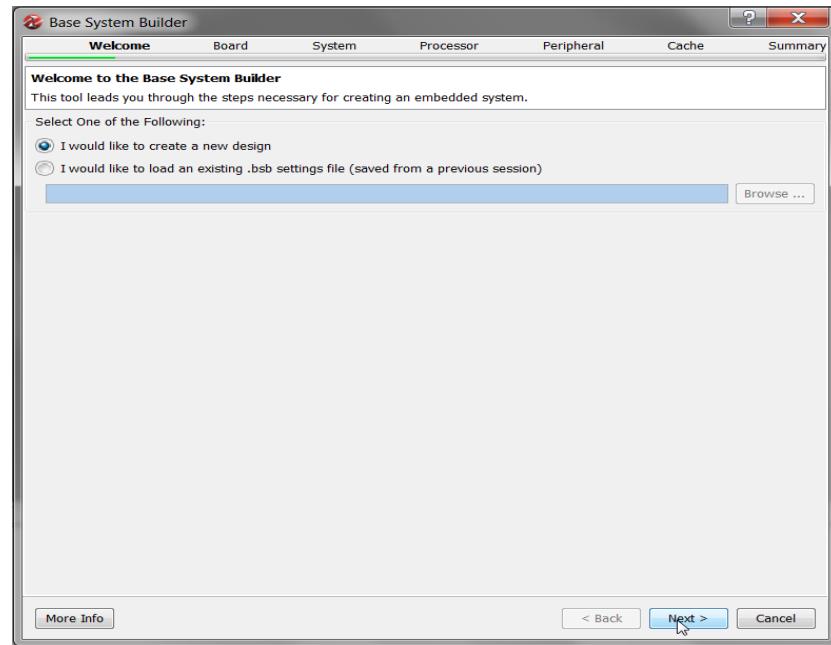
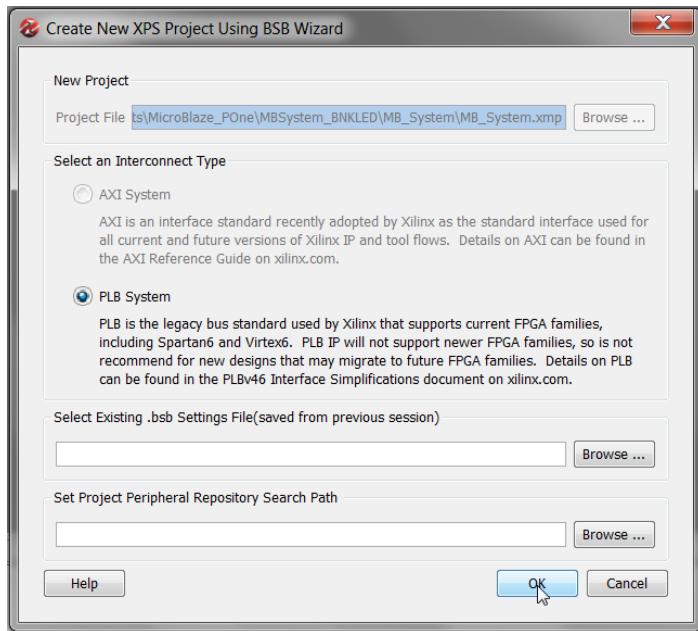


4. Click on embedded processor & provide name *MB_System*. Click next, check summary & Click Finish.
5. ISE navigator will create *MB_System.xmp* and it will open up Platform Studio
6. Setting up Microblaze hardware: Platform studio will open up with display dialogue "Do you want to create Base system with BSB Wizard?" Click Yes.

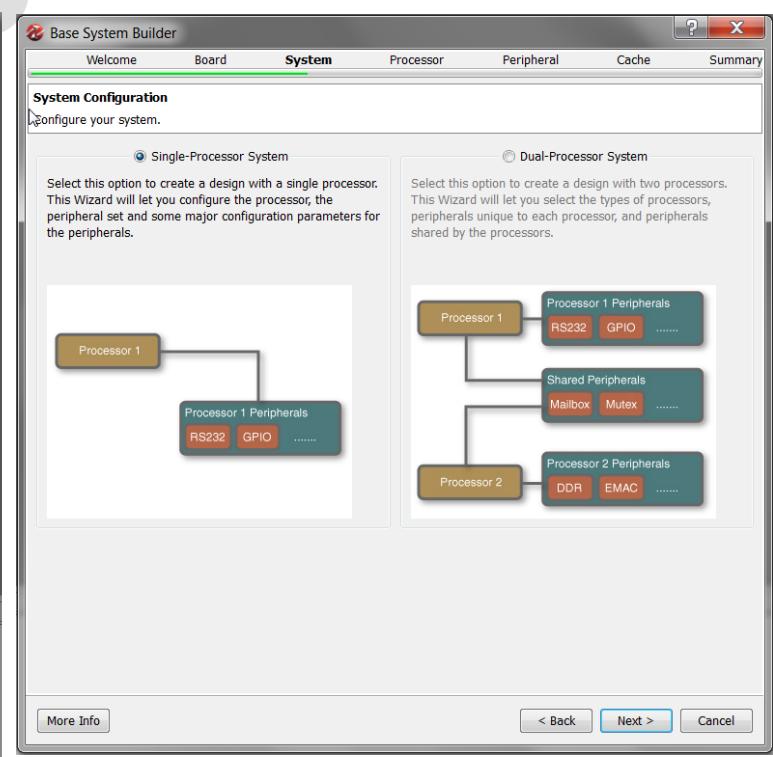
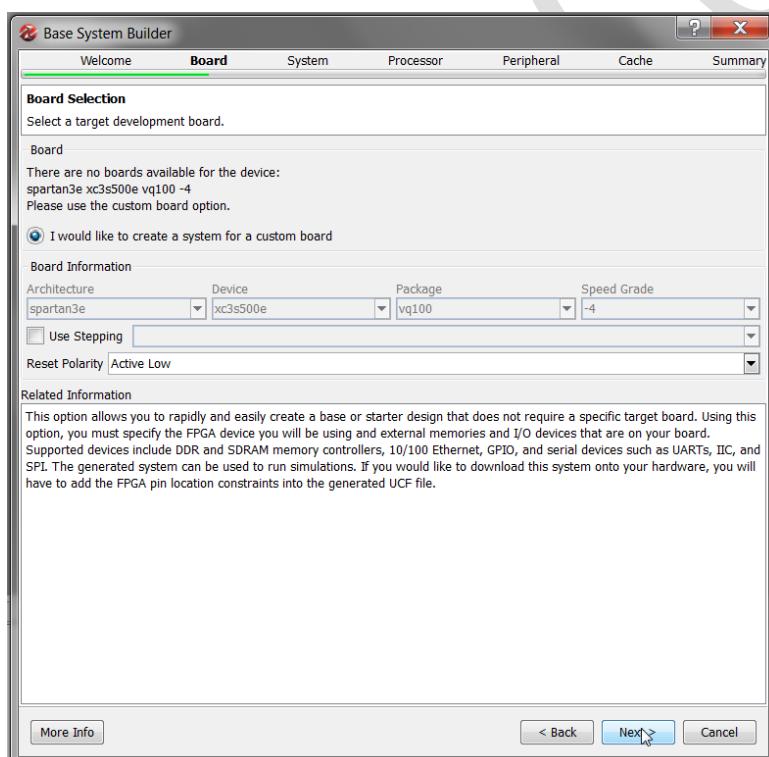


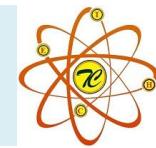


7. Select PLB System & leave other parameter to default. Click OK
8. Select "I would like to create a new design" & Click Next



9. Board window will take default parameters from ISE. You can change reset polarity from default Active Low to Active High.
 In this tutorial this value will be set to default i.e. Active Low (We are going to setup reset pin on Joystick button of Papilio). Click Next.
10. Select Single-Processor System and Click Next.



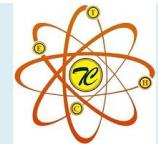


11.In Processor tab change Reference clock frequency to 32MHz (Papilio One oscillator frequency). Leave other parameters to default and Click Next.

12.In peripheral configuration, Click on Add Device

13.After clicking on Add device for Generic Board, Select GPIO in IO Interface type & LED in device. Tick Add Device to system option.

14.In Peripherals Click on LEDS : Ok then change GPIO Data width to 8



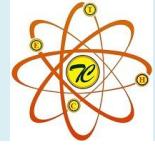
15.then change GPIO Data width to 8

16.Similarly Add DIP Switches with GPIO Interface and change GPIO data width to 4

The screenshots show the 'Peripheral Configuration' tab of the Base System Builder. In the first screenshot, the 'Core' dropdown is set to 'xps_gpio' and the 'Parameter' dropdown is set to '32'. In the second screenshot, the 'Core' dropdown is set to 'DIP_Switches' and the 'Parameter' dropdown is set to '4'. Both screenshots show a list of peripherals including 'dlimb_cntlr' and 'ilimb_cntlr'.

17.In Cache configuration, As there is no cacheable memory just click Next.

The left screenshot shows the 'Add IO Devices for Generic Board' dialog. The 'IO Interface Type' dropdown is set to 'GPIO' and the 'Device' dropdown is set to 'DIP_Switches'. A checkbox 'Add Device to system' is checked. The right screenshot shows the 'Cache Configuration' dialog for 'Processor 1 (MicroBlaze) Cache', which displays the message 'There is no cacheable memory for this processor'.



18.Check summary & click Finish.

Base System Builder

Summary

Below is the summary of the system you are creating.

System Summary

Core Name	Instance Name	Base Address	High Address
Processor 1	microblaze_0		
xps_gpio	DIP_Switches	0x81420000	0x8142FFFF
xps_gpio	LEDS	0x81400000	0x8140FFFF
lmb_bram_if_cntlr	dlmb_ctrlr	0x00000000	0x00001FFF
lmb_bram_if_cntlr	ilmb_ctrlr	0x00000000	0x00001FFF

File Location

Overall

- D:\Xilinx_Projects\MicroBlaze_POne\MBSYSTEM_BNKLED\MB_System\xmp
- D:\Xilinx_Projects\MicroBlaze_POne\MBSYSTEM_BNKLED\MB_System\MB_System.mhs
- D:\Xilinx_Projects\MicroBlaze_POne\MBSYSTEM_BNKLED\MB_System\data\MB_System.ucf
- D:\Xilinx_Projects\MicroBlaze_POne\MBSYSTEM_BNKLED\MB_System\etc\fast_runtime.opt
- D:\Xilinx_Projects\MicroBlaze_POne\MBSYSTEM_BNKLED\MB_System\etc\download.cmd
- D:\Xilinx_Projects\MicroBlaze_POne\MBSYSTEM_BNKLED\MB_System\etc\bitgen.ut

Save Base System Builder (.bsb) Settings File
D:\Xilinx_Projects\MicroBlaze_POne\MBSYSTEM_BNKLED\MB_System\MB_System.bsb

More Info

< Back **Finish** Cancel Help

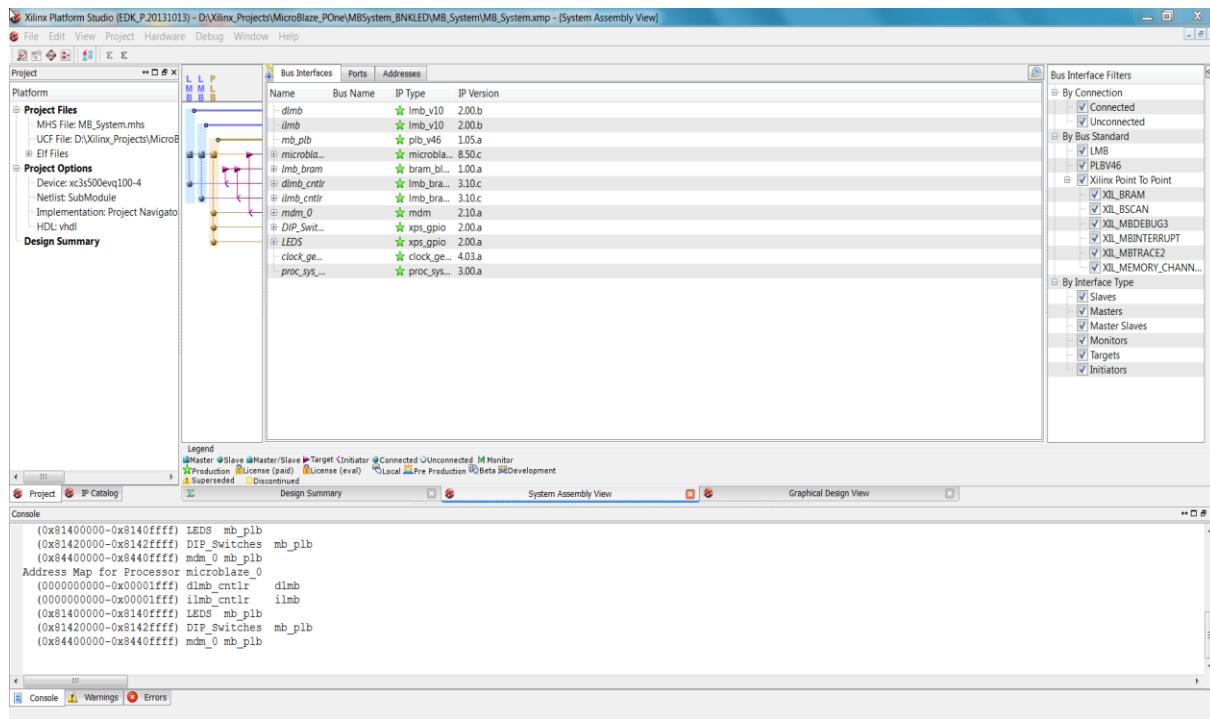
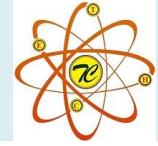
19.Just click OK for Dialogue box Running Design



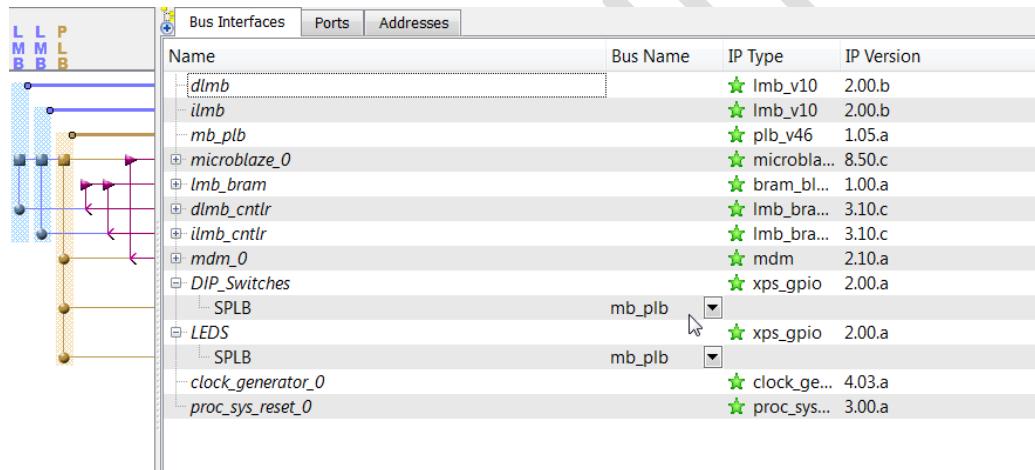
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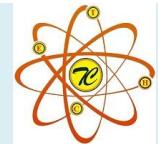


21.In Bus Interface tab, Check GPIO LED & Switches are connected to **mb_plb** or not.



22.In Ports tab, Check for LED & Switches are connected or not.

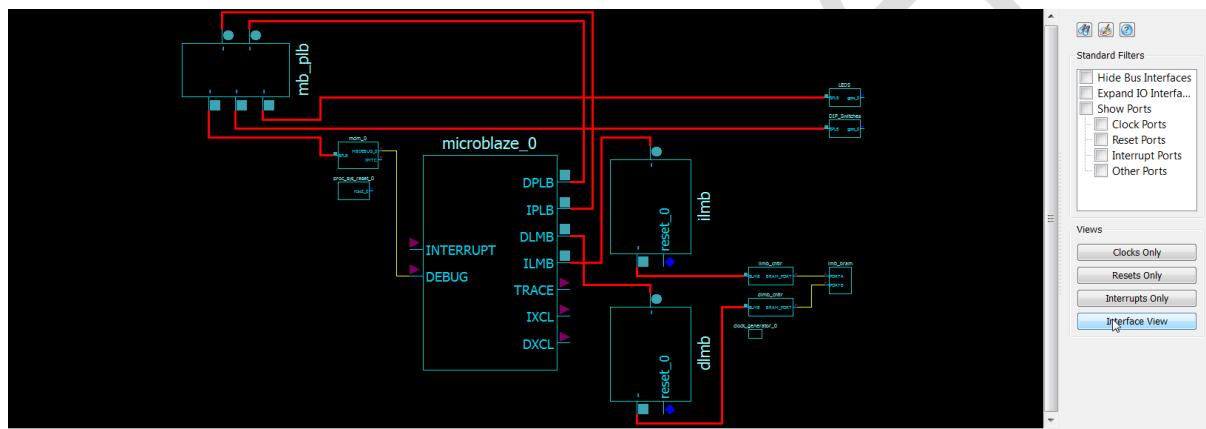
Name	Connected Po	Direction	Range	Class	Frequency(Hz)	Reset Polarity	Sensitivity	IP Type	Differential Polarity
External Ports									
dlmb								Imb_v10	
ilmb								Imb_v10	
mb_plb								plb_v46	
microblaze_0								microbla...	
lmb_bram								bram_bl...	
dlmb_cntlr								lmb_bra...	
ilmb_cntlr								lmb_bra...	
mdm_0								mdm	
DIP_Switches								xps_gpio	
LEDS								xps_gpio	
clock_generator_0								clock_ge...	
proc_sys_reset_0								proc_sys...	



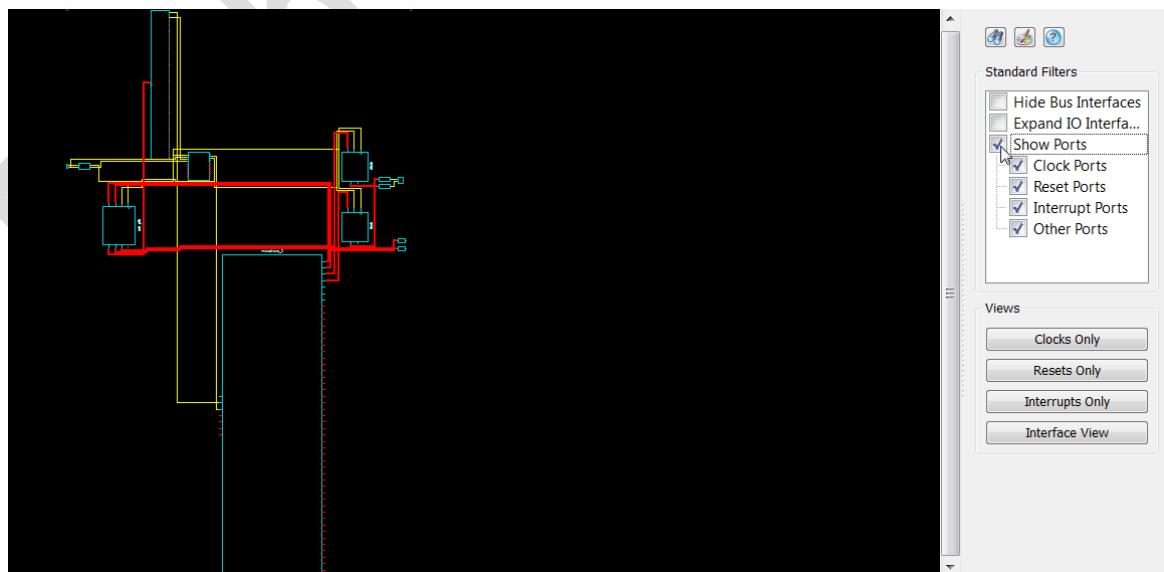
23. Check address in Address tab

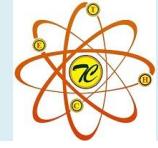
Instance	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name	Lock
microblaze_0's Address ...							
dlmb_cntlr	C_BASEADDR	0x00000000	0x00001FFF	8K	<input checked="" type="checkbox"/> SLMB	dlmb	<input type="checkbox"/>
ilmb_cntlr	C_BASEADDR	0x00000000	0x00001FFF	8K	<input checked="" type="checkbox"/> SLMB	ilmb	<input type="checkbox"/>
LEDS	C_BASEADDR	0x81400000	0x8140FFFF	64K	<input checked="" type="checkbox"/> SPLB	mb_plb	<input type="checkbox"/>
DIP_Switches	C_BASEADDR	0x81420000	0x8142FFFF	64K	<input checked="" type="checkbox"/> SPLB	mb_plb	<input type="checkbox"/>
mdm_0	C_BASEADDR	0x84400000	0x8440FFFF	64K	<input checked="" type="checkbox"/> SPLB	mb_plb	<input type="checkbox"/>

24. View Block diagram in Graphical view



25. If you click on Show ports





26. Now edit ucf file according to Logistart Megawing of Papilio one. In this tutorial ucf file of Indian version of Logistart Megawing is followed.

Xilinx Platform Studio (EDK_P_20131013) - D:\Xilinx_Projects\MicroBlaze_POne\MBSystem_BNKLED\MB_System.xmp - [MB_System.ucf]

```

1 # Generic Template
2 ## Net fpga_0_LEDs_GPIO IO_0_pin<0> LOC="";
3 ## Net fpga_0_LEDs_GPIO IO_0_pin<1> LOC="";
4 ## Net fpga_0_LEDs_GPIO IO_0_pin<2> LOC="";
5 ## Net fpga_0_LEDs_GPIO IO_0_pin<3> LOC="";
6 ## Net fpga_0_LEDs_GPIO IO_0_pin<4> LOC="";
7 ## Net fpga_0_LEDs_GPIO IO_0_pin<5> LOC="";
8 ## Net fpga_0_LEDs_GPIO IO_0_pin<6> LOC="";
9 ## Net fpga_0_LEDs_GPIO IO_0_pin<7> LOC="";
10 ## Net fpga_0_DIP_Switches_GPIO IO_I_1_pin<0> LOC="";
11 ## Net fpga_0_DIP_Switches_GPIO IO_I_1_pin<1> LOC="";
12 ## Net fpga_0_DIP_Switches_GPIO IO_I_1_pin<2> LOC="";
13 ## Net fpga_0_DIP_Switches_GPIO IO_I_1_pin<3> LOC="";
14 Net fpga_0_clk_1_svs_clk_pin TNM_NET = sys_clk_pin;
15 TIMESPEC TS_sys_clk_pin = PERIOD sys_clk_pin 32000 kHz;
16 ## Net fpga_0_clk_1_svs_clk_pin LOC="";
17 Net fpga_0_rst_1_svs_rst_pin TIG;
18 ## Net fpga_0_rst_1_svs_rst_pin LOC="";
19

```

Project IP Catalog Design Summary System Assembly View Graphical Design View MB_System.ucf

Console

```

(0x81420000-0x8142ffff) DIP_Switches mb_plb
(0x84400000-0x8440ffff) mdm_0_mb_plb
Address Map for Processor microblaze_0
(0000000000-0x000001ff) dlmbs_c0_dlmbs ilmb
(0000000000-0x000001ff) ilmb_cntr ilmb
(0x81400000-0x8140ffff) LEDs_mb_plb
(0x81420000-0x8142ffff) DIP_Switches mb_plb
(0x84400000-0x8440ffff) mdm_0_mb_plb
Overriding Xilinx file <TextEditor.cfg> with local file <D:/XilinxInstallation/14.7/ISE_DS/EDK/data/TextEditor.cfg>

```

Console Warnings Errors

Xilinx Platform Studio (EDK_P_20131013) - D:\Xilinx_Projects\MicroBlaze_POne\MBSystem_BNKLED\MB_System.xmp - [MB_System.ucf]

```

1 # Generic Template
2 Net fpga_0_LEDs_GPIO IO_0_pin<0> LOC="P4";
3 Net fpga_0_LEDs_GPIO IO_0_pin<1> LOC="P3";
4 Net fpga_0_LEDs_GPIO IO_0_pin<2> LOC="P2";
5 Net fpga_0_LEDs_GPIO IO_0_pin<3> LOC="P9";
6 Net fpga_0_LEDs_GPIO IO_0_pin<4> LOC="P8";
7 Net fpga_0_LEDs_GPIO IO_0_pin<5> LOC="P9A";
8 Net fpga_0_LEDs_GPIO IO_0_pin<6> LOC="P9B";
9 Net fpga_0_LEDs_GPIO IO_0_pin<7> LOC="P9I";
10 Net fpga_0_DIP_Switches_GPIO IO_I_1_pin<0> LOC= "P5";
11 Net fpga_0_DIP_Switches_GPIO IO_I_1_pin<1> LOC= "P4";
12 Net fpga_0_DIP_Switches_GPIO IO_I_1_pin<2> LOC= "P10";
13 Net fpga_0_DIP_Switches_GPIO IO_I_1_pin<3> LOC= "P11";
14 Net fpga_0_clk_1_svs_clk_pin TNM_NET = sys_clk_pin;
15 TIMESPEC TS_sys_clk_pin = PERIOD sys_clk_pin 32000 kHz;
16 Net fpga_0_clk_1_svs_clk_pin LOC= "P9";
17 Net fpga_0_rst_1_svs_rst_pin TIG;
18 Net fpga_0_rst_1_svs_rst_pin LOC= "P17";
19

```

Project IP Catalog Design Summary System Assembly View Graphical Design View MB_System.ucf

Console

```

(0x81420000-0x8142ffff) DIP_Switches mb_plb
(0x84400000-0x8440ffff) mdm_0_mb_plb
Address Map for Processor microblaze_0
(0000000000-0x000001ff) dlmbs_c0_dlmbs ilmb
(0000000000-0x000001ff) ilmb_cntr ilmb
(0x81400000-0x8140ffff) LEDs_mb_plb
(0x81420000-0x8142ffff) DIP_Switches mb_plb
(0x84400000-0x8440ffff) mdm_0_mb_plb
Overriding Xilinx file <TextEditor.cfg> with local file <D:/XilinxInstallation/14.7/ISE_DS/EDK/data/TextEditor.cfg>

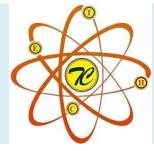
```

Console Warnings Errors

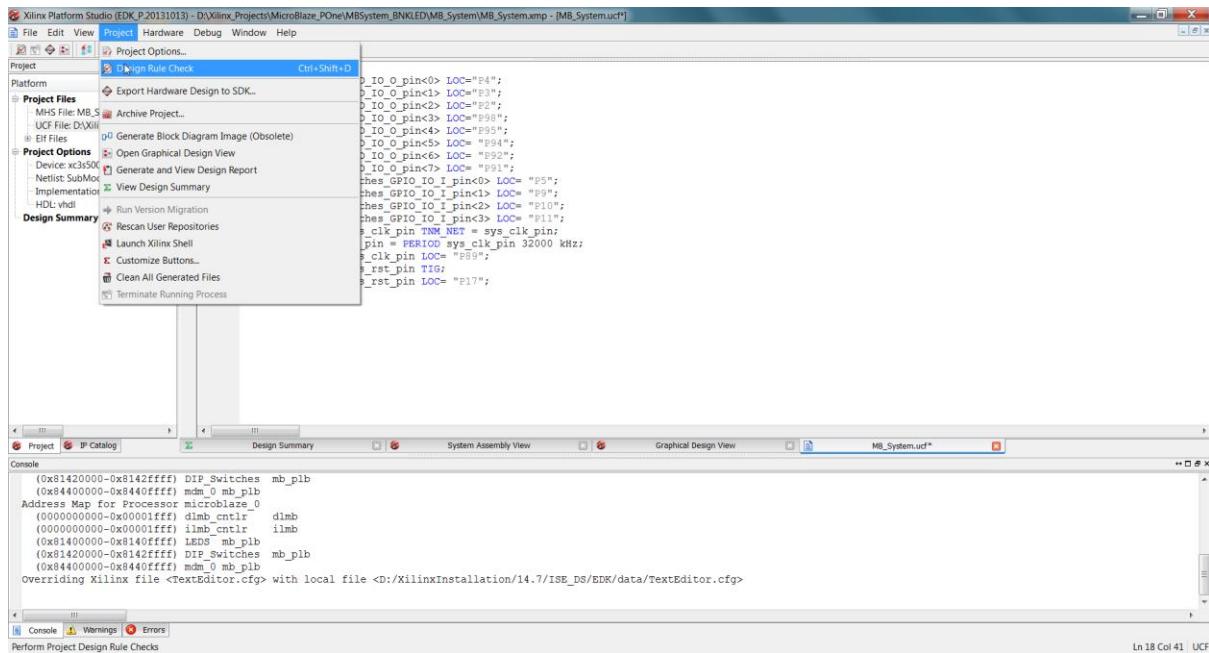
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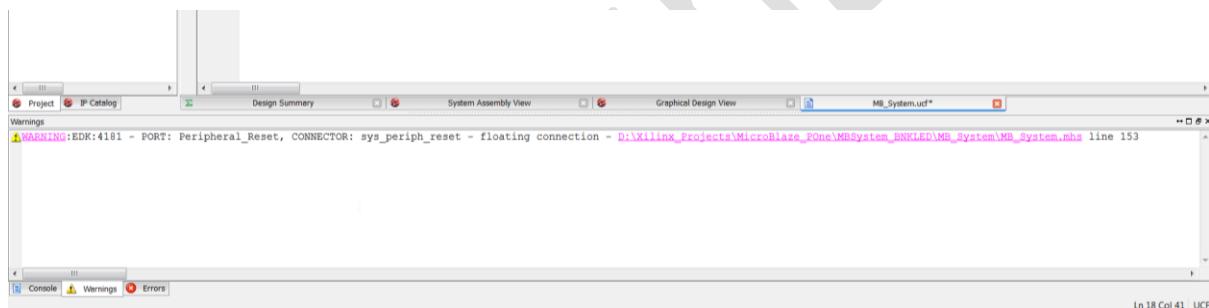
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27. Now Perform Design Rule Check

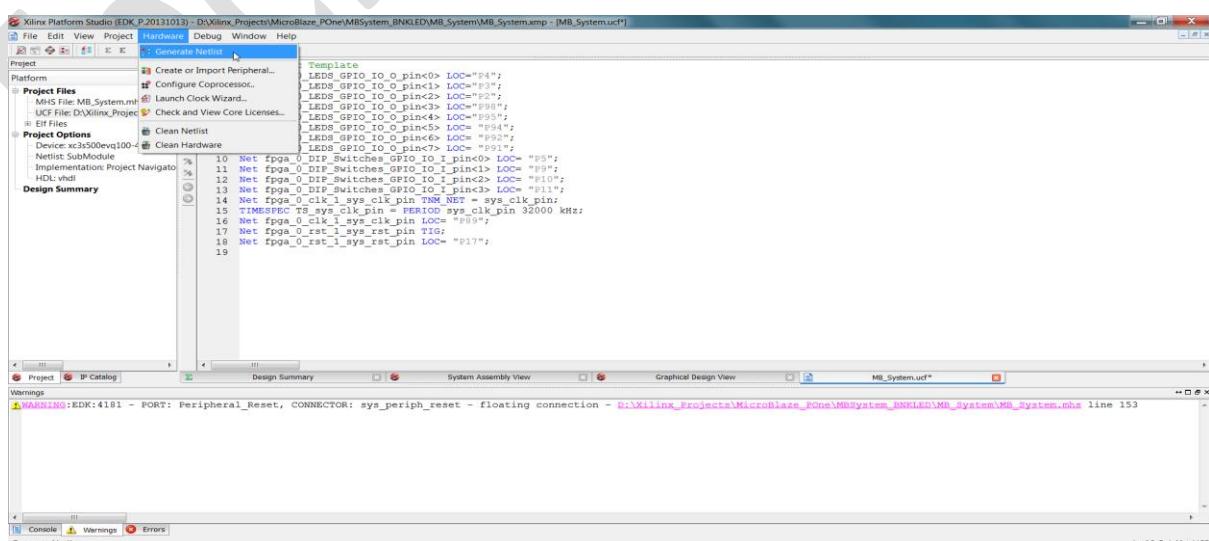


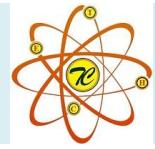
28. Ignore following warning



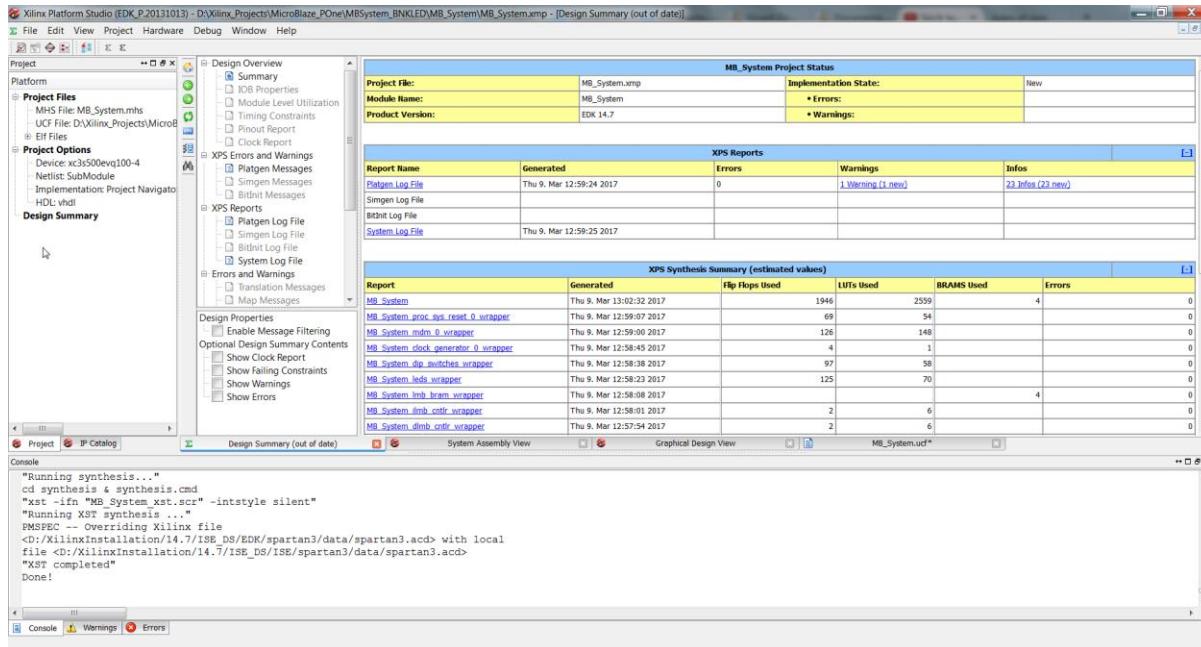
29. If other warnings are present then kindly check previous flow steps & ucf file

30. Generate netlist for embedded processor. Be patient for 15-30 minutes, Have a break!!!!



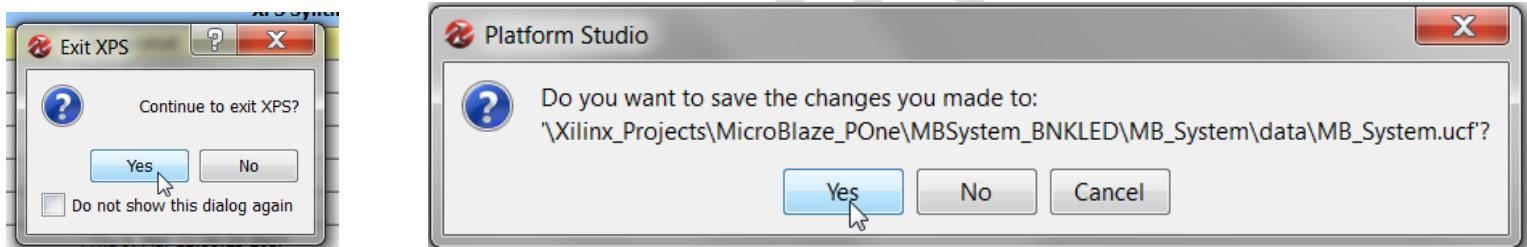


31. After netlist generation console will show "XST completed" Done!

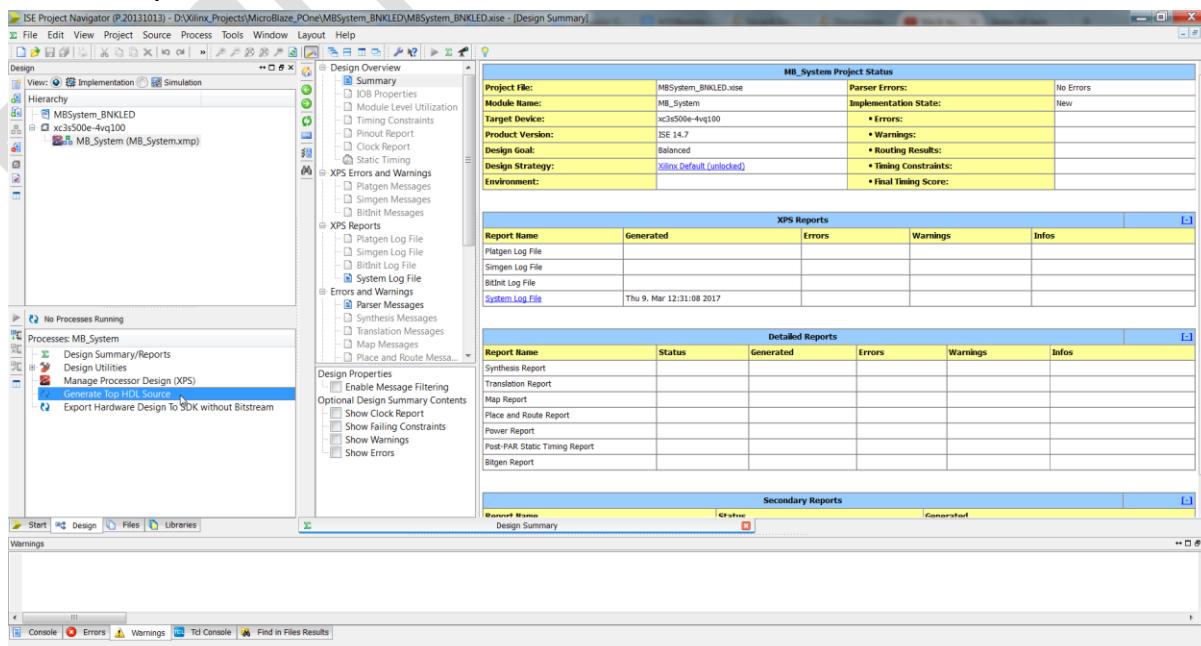


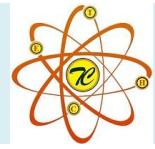
32. Close platform studio

33. Platform studio will ask for save changes in MB_System.ucf, Click Yes!!



34. Return to ISE navigator & click on MB_system in design window & generate Top HDL Source in process window.





35.After generating TOP HDL source, ISE will generate MB_System_Top.vhd and automatically assign MB_System (i.e. microblaze procesor) pins to top level VHDL code.

```

ISE Project Navigator (P.20131013) - D:\Xilinx_Projects\MicroBlaze_POne\MBSystem_BNKLED\MBSystem_BNKLED.xise - [MB_System_top.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design View: Implementation Simulation
Hierarchy
  MBSystem_BNKLED
    xc3s500e-4vq100
      MB_System_top - STRUCTURE (MB_System_top.vhd)
        MB_System_i - MB_System (MB_System.xmp)
No Processes Running
Processes: MB_System_top - STRUCTURE
  Design Summary/Reports
  Design Utilities
  User Constraints
  Synthesize - XST
  Implement Design
  Generate Programming File
  Configure Target Device
  Analyze Design Using ChipScope
Start Design Files Libraries
Design Summary MB_System_top.vhd
MB_System_top.vhd
Ln 19 Col 1 VHDL

```

36.Click on MB_System_Top.vhd and double click on generate programming file. Be patient for 15-30 minutes, Have a break!!!!

```

ISE Project Navigator (P.20131013) - D:\Xilinx_Projects\MicroBlaze_POne\MBSystem_BNKLED\MBSystem_BNKLED.xise - [MB_System_top.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design View: Implementation Simulation
Hierarchy
  MBSystem_BNKLED
    xc3s500e-4vq100
      MB_System_top - STRUCTURE (MB_System_top.vhd)
        MB_System_i - MB_System (MB_System.xmp)
No Processes Running
Processes: MB_System_top - STRUCTURE
  Design Summary/Reports
  Design Utilities
  User Constraints
  Synthesize - XST
  Implement Design
  Generate Programming File
  Configure Target Device
  Analyze Design Using ChipScope
Start Design Files Libraries
Design Summary (Programming File Generated) MB_System_top.vhd
MB_System_top.vhd
Ln 19 Col 1 VHDL

```

Warnings

WARNING:PhysDesignRules:367 - The signal <MB_System_i/dlmb_LMB_ABus<31> is incomplete. The signal does not drive any load pins in the design.

WARNING:PhysDesignRules:367 - The signal <MB_System_i/dlmb_LMB_ABus<30> is incomplete. The signal does not drive any load pins in the design.

WARNING:Par:288 - The signal MB_System_i/dlmb_LMB_ABus<31> has no load. PAR will not attempt to route this signal.

WARNING:Par:288 - The signal MB_System_i/dlmb_LMB_ABus<30> has no load. PAR will not attempt to route this signal.

Phase:Par:288 - 0.0ns routing; WARNING:Route:455 - CLK Net: fpga_0_clk_1_sys_clk_pin_IBUFG may have excessive skew because

WARNING:Par:288 - 0.0ns routing; DRC: /VDDC to GND has excessive skew because

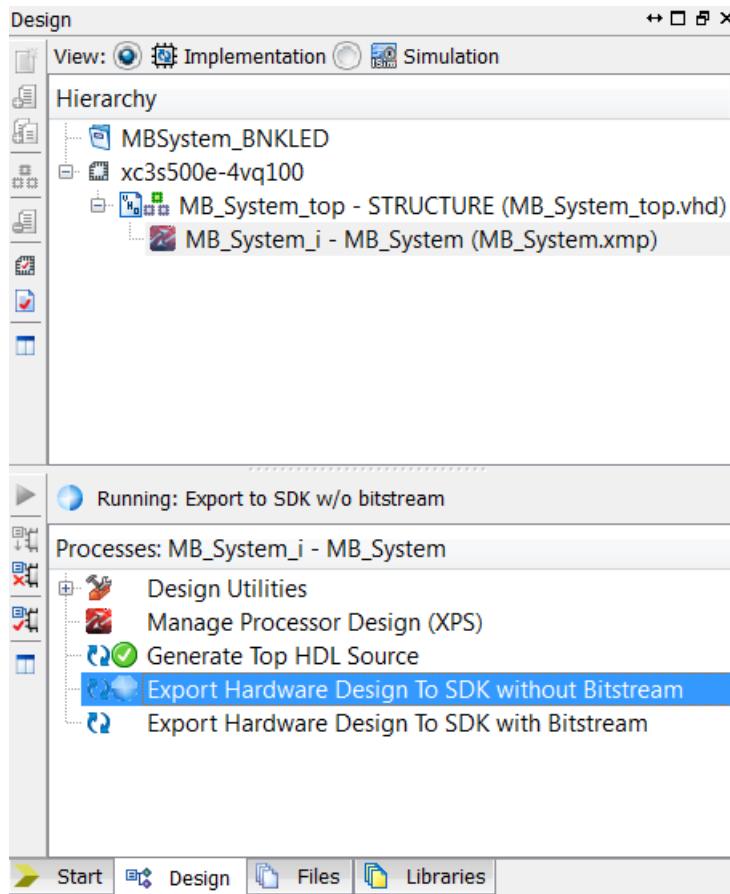
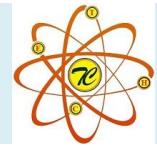
WARNING:Par:283 - There are 2 loadless signals in this design. This design will cause Bitgen to issue DRC warnings.

WARNING:PhysDesignRules:367 - The signal <MB_System_i/dlmb_LMB_ABus<31> is incomplete. The signal does not drive any load pins in the design.

WARNING:PhysDesignRules:367 - The signal <MB_System_i/dlmb_LMB_ABus<30> is incomplete. The signal does not drive any load pins in the design.

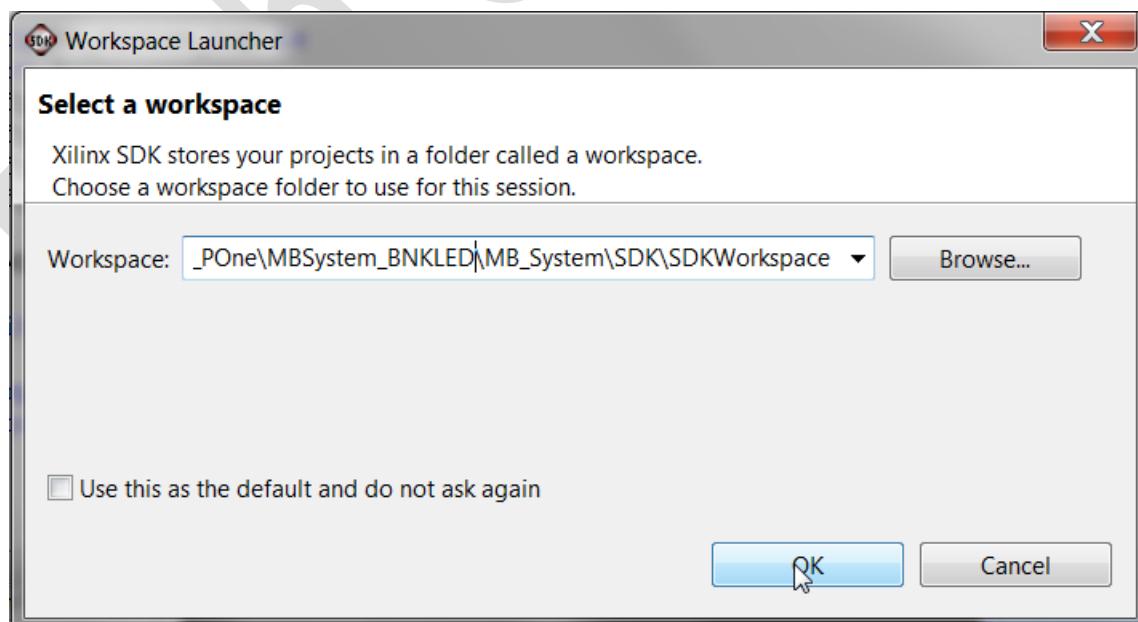
37.In console and warning window it will show some warnings related to JTAG signals not connected & clock skew. Ignore them.

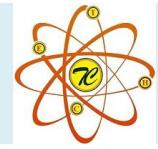
38.Now Click on MB_System.xmp in design process then Double click on Export hardware Design to SDK without Bitstream.



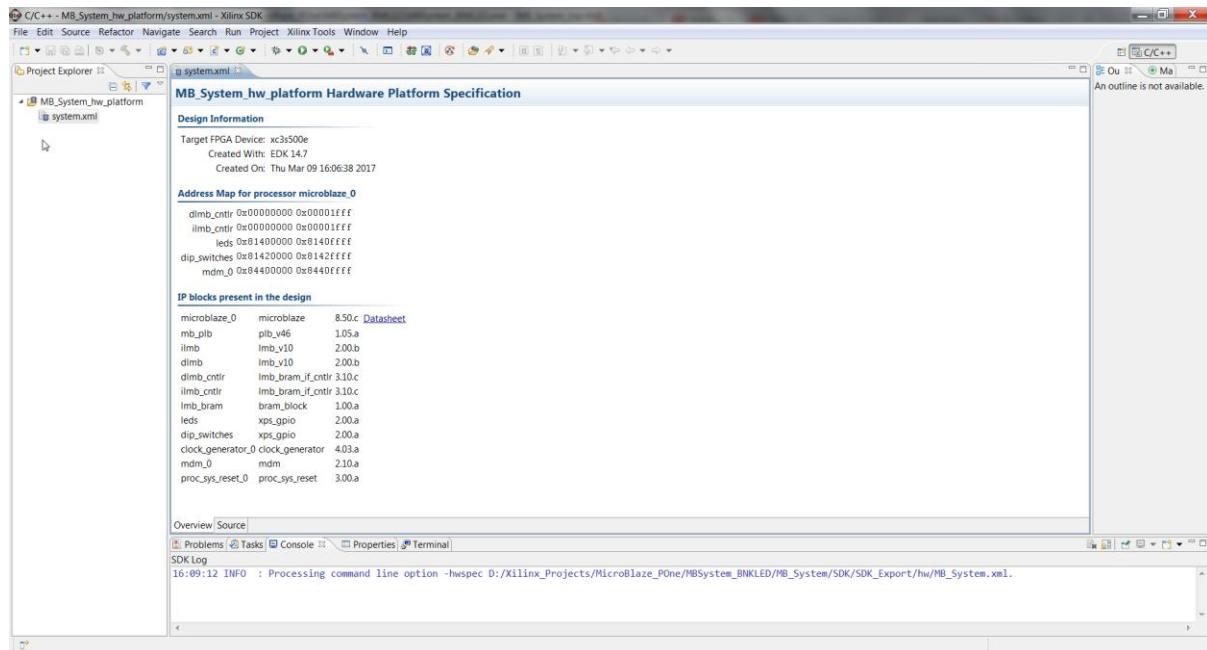
39. After double clicking on Export hardware Design to SDK without Bitstream ISE will launch Xilinx SDK with Select Workspace. Make new folder named "SDKWorkspace" inside of project Microblaze_BNKLED\MB_System\SDK\

40. Click OK

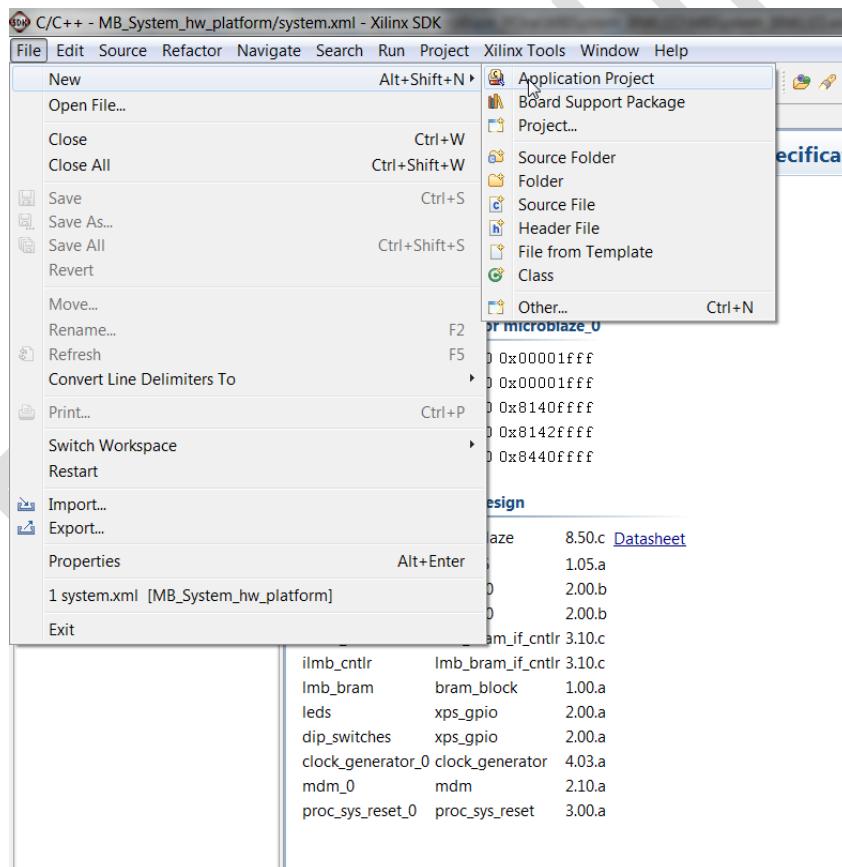


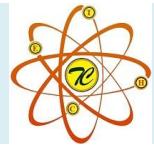


Xilinx SDK

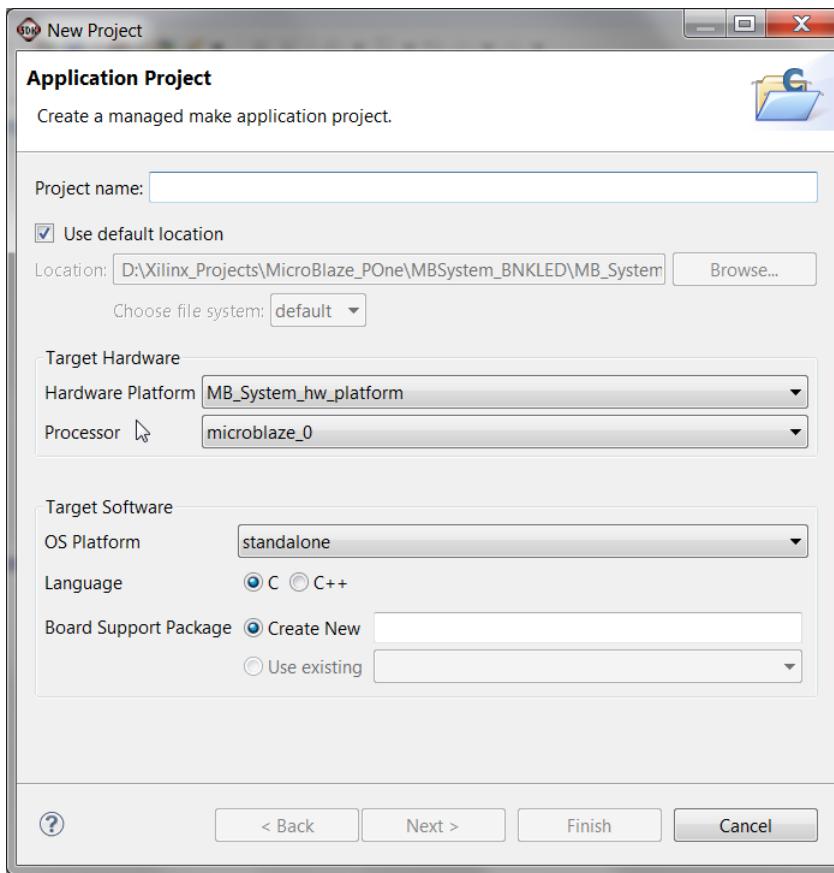


1. Create new Application project in Xilinx SDK





2. SDK will automatically locate our MB_System as our Target Hardware



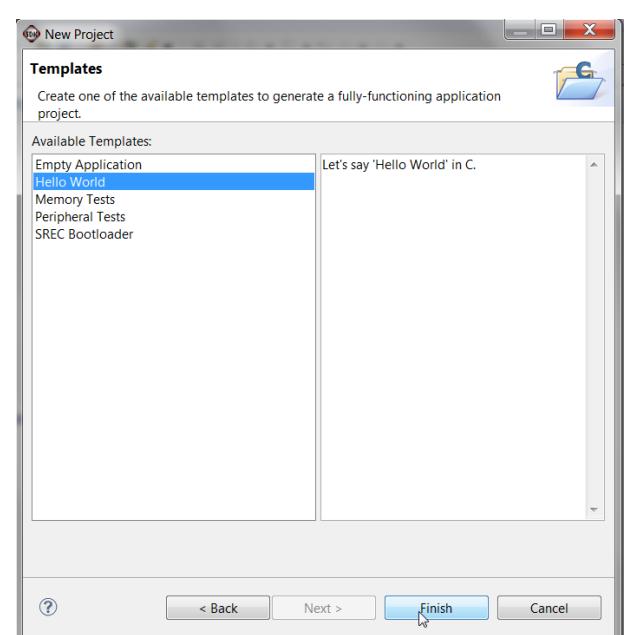
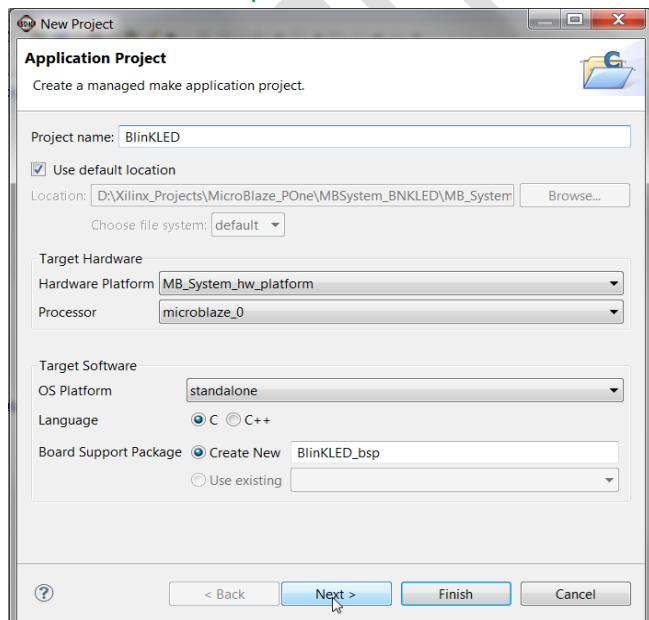
3. Provide inputs to Application project as follows:

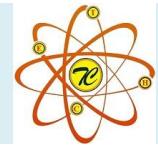
Project name: BlinkLED, OS Platform: standalone, Language : C,

Board Support Package: Create New

Click Next.

4. Select template Hello World & click finish





5. Project will get automatically compiled & create elf file.

```
File Edit Source Refactor Search Run Project Xilinx Tools Window Help
Project Explorer system.xml system.mss
BlinKLED BSP Board Support Package
Modify this BSP's Settings
Target Information
This Board Support Package is compiled to run on the following target.
Hardware Specification: D:\Xilinx\Projects\MicroBlaze_POne\MBSystem\BNKLED\MB_System\SDK\Workspace\MB_System_hw_platform\system.xml
Target Processor: microblaze_0
Operating System
Board Support Package OS.
Name: standalone
Version: 3.11.a
Description: Standalone is a simple, low-level software layer. It provides access to basic processor features such as caches, interrupts and exceptions as well as the basic features of a hosted environment, such as standard input and output, profiling, abort and exit.
Documentation: standalone v3.11.a
Peripheral Drivers
Drivers present in the Board Support Package.
dip_switches gpio Documentation Examples
dlimb_cntr bram Documentation Examples
ilimb_cntr bram Documentation Examples
leds gpio Documentation Examples
mdm_0 uartlite Documentation Examples
Overview [Source]
Problems Tasks Console Properties Terminal
CDT Build Console [BlinKLED]
microblaze_0_BlinKLED.elf
ELF file : BlinKLED.elf
elfcheck passed.
'Finished building: BlinKLED.elf.elfcheck'
16:11:53 Build Finished (took 3s.295ms)
```

6. Go to BlinkLED > src then double click on helloworld.c

Right click on helloworld.c & using rename option change file name to BlinkLED.c

```
File Edit Source Refactor Search Run Project Xilinx Tools Window Help
Project Explorer system.xml system.mss helloworld.c
BlinKLED Binaries Includes Debug src helloworld.c platform_config.h platform.c platform.h IspcifId BlinKLED BSP MB_System_hw_platform system.xml
/*
 * helloworld.c: simple test application
 *
 * This application configures WART 16550 to baud rate 9600.
 * PS7 UART (Zynq) is not initialized by this application, since
 * bootrom/bsp configures it to baud rate 115200
 *
 * -----
 * | UART TYPE BAUD RATE
 * -----
 * | warts550 9600
 * | uartlite Configurable only in HW design
 * | ps7_uart 115200 (configured by bootrom/bsp)
 */

#include <stdio.h>
#include "platform.h"

void print(char *str);

int main()
{
    init_platform();

    print("Hello World\n\r");

    return 0;
}

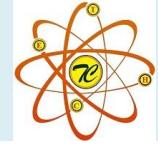
ELF file : BlinKLED.elf
elfcheck passed.
'Finished building: BlinKLED.elf.elfcheck'
16:11:53 Build Finished (took 3s.295ms)
```

For Code or any other detail please contact us

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7. Replace helloworld.c program to following program

```
/*
 * BlinkLED.c: simple test application
 */

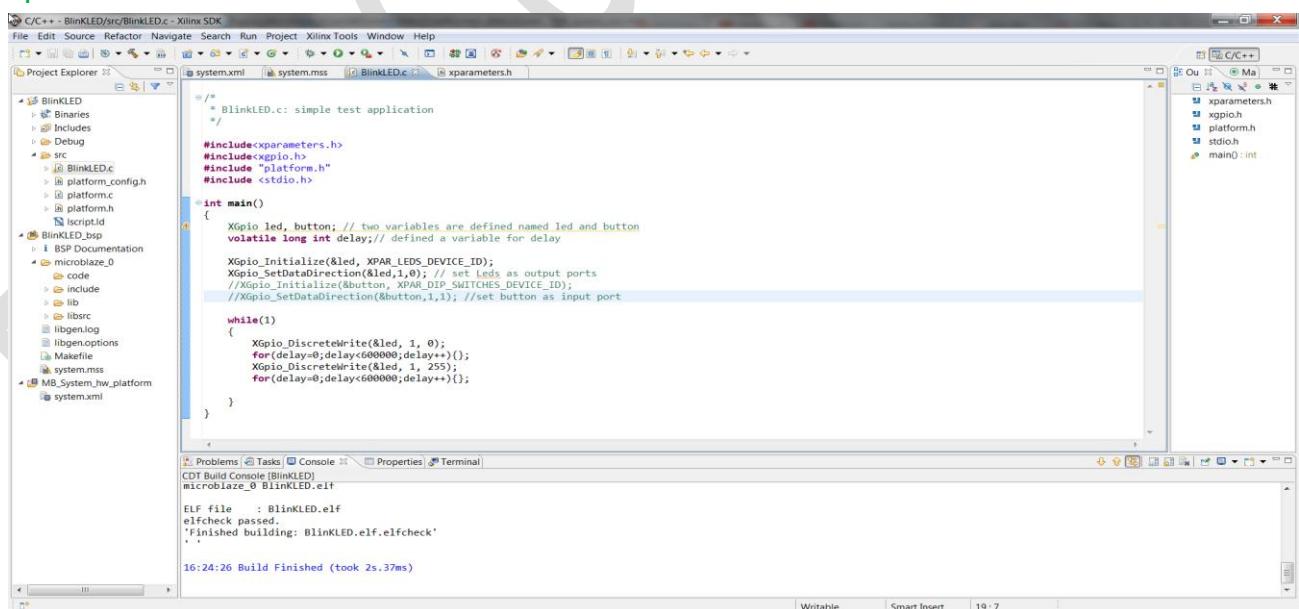
#include<xparameters.h>
#include<xgpio.h>
#include "platform.h"
#include <stdio.h>

int main()
{
    XGpio led, button; // two variables are defined named led and button
    volatile long int delay;// defined a variable for delay

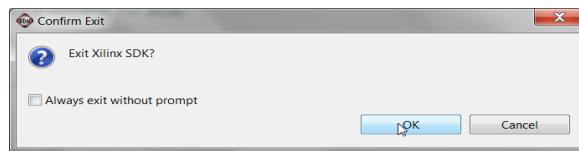
    XGpio_Initialize(&led, XPAR_LEDs_DEVICE_ID);
    XGpio_SetDataDirection(&led,1,0); // set Leds as output ports
    //XGpio_Initialize(&button, XPAR_DIP_SWITCHES_DEVICE_ID);
    //XGpio_SetDataDirection(&button,1,1); //set button as input port

    while(1)
    {
        XGpio_DiscreteWrite(&led, 1, 0);
        for(delay=0;delay<600000;delay++) {};
        XGpio_DiscreteWrite(&led, 1, 255);
        for(delay=0;delay<600000;delay++) {};
    }
}
```

8. After changing program, Click Save program will be compiled automatically and updated BlinkLED.elf will be created.



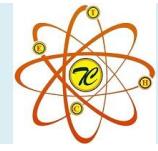
9. Exit Xilinx SDK



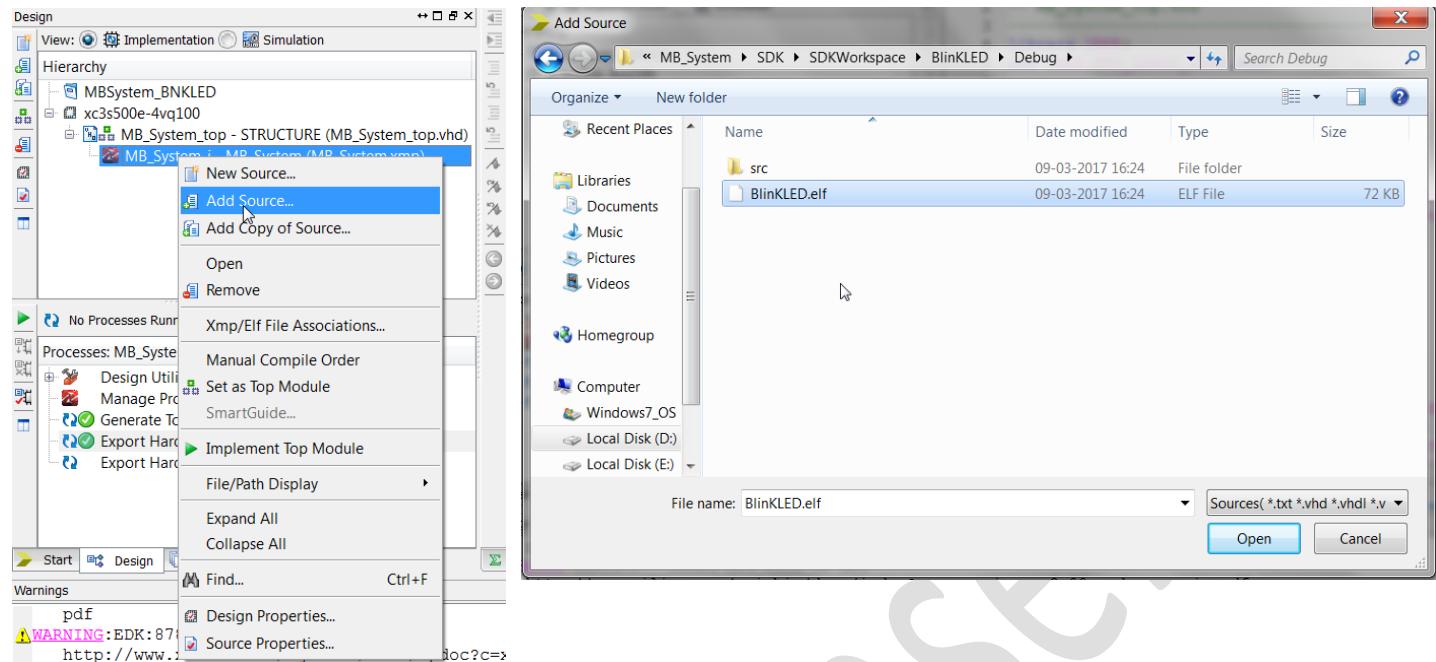
10.Return to

MB_System.xmp and right click on it & chose new source

Xilinx ISE. Click on

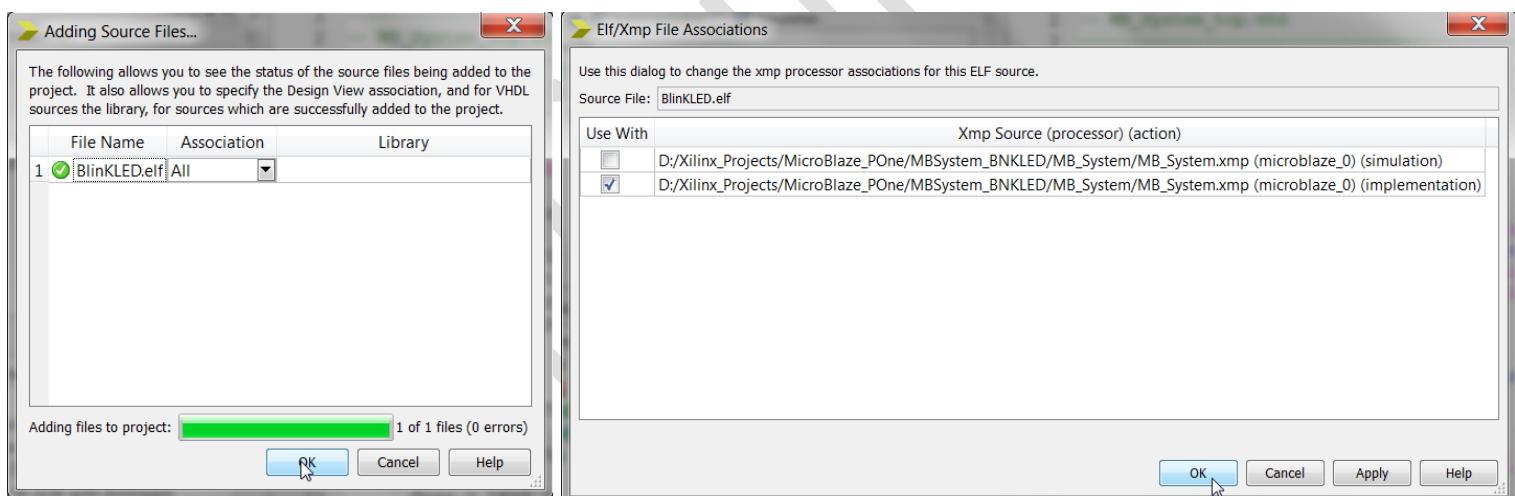


11.Then add BlinkLED.elf from



12.SDKWorkspace/BlinkLED/Debug: Click OK

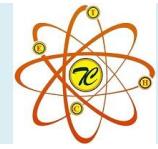
13.Provide elf file associations for implementation & click OK



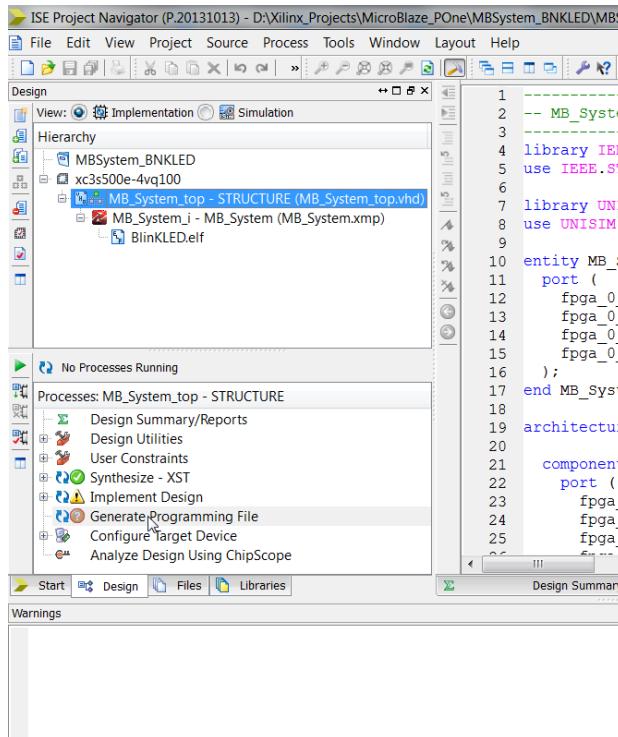
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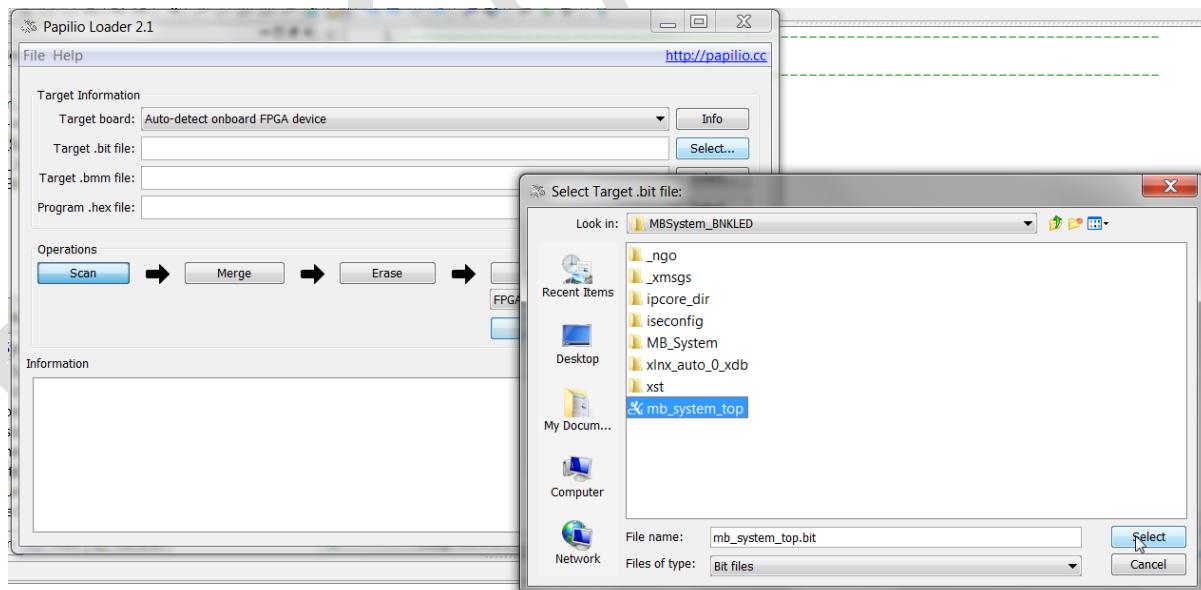


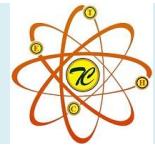
14. As we add BlinkLEDD.elf into ISE project, Generate Programming file option will get question mark



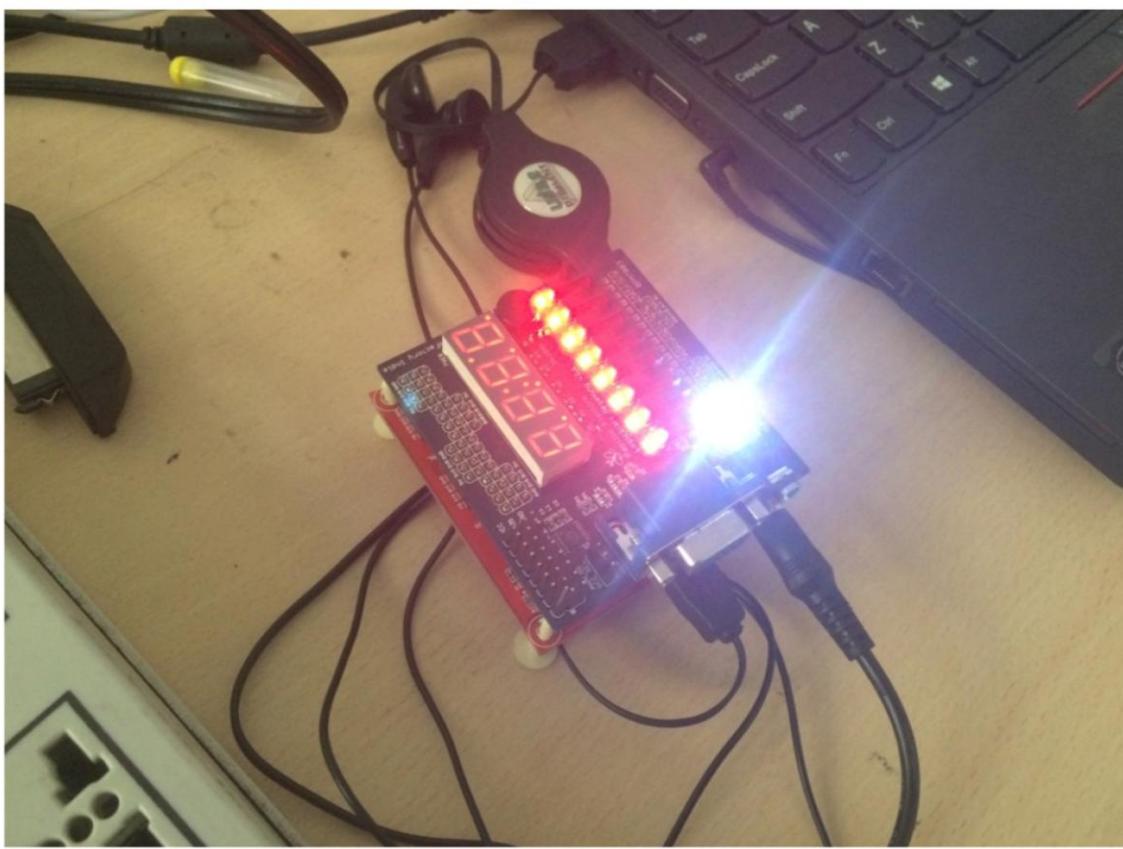
15. Double click on generate programming file. Now ISE navigator will update programming file with software program loaded into BRAM blocks of FPGA.

16. Now Program Papilio board with mb_system_top.bit





17. That's all Folk. When first pin of is active HIGH blinking LED program start running on our Papilio one board.



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