**EXPERIMENT NO: 1 ALU**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity SUNEETALUCODE is

Port ( A : in STD\_LOGIC\_VECTOR (03 downto 0);

B : in STD\_LOGIC\_VECTOR (03 downto 0);

SEL : in STD\_LOGIC\_VECTOR (02 downto 0);

Z : out STD\_LOGIC\_VECTOR (03 downto 0));

end SUNEETALUCODE;

architecture Behavioral of SUNEETALUCODE is

begin

process(SEL)

begin

case SEL is

when"000"=>Z<=A+B;

when"001"=>Z<=A-B;

when"010"=>Z<=A;

when"011"=>Z<=B;

when"100"=>Z<=A and B;

when"101"=>Z<=A or B;

when"110"=>Z<=not A;

when others=>Z<=not B;

end case;

end process;

end Behavioral;

**UCF FILE :**

net "A(3)" LOC = P205;

net "A(2)" LOC = P206;

net "A(1)" LOC = P203;

net "A(0)" LOC = P200;

net "B(3)" LOC = P192;

net "B(2)" LOC = P193;

net "B(1)" LOC = P189;

net "B(0)" LOC = P190;

net "SEL(2)" LOC = P179;

net "SEL(1)" LOC = P180;

net "SEL(0)" LOC = P177;

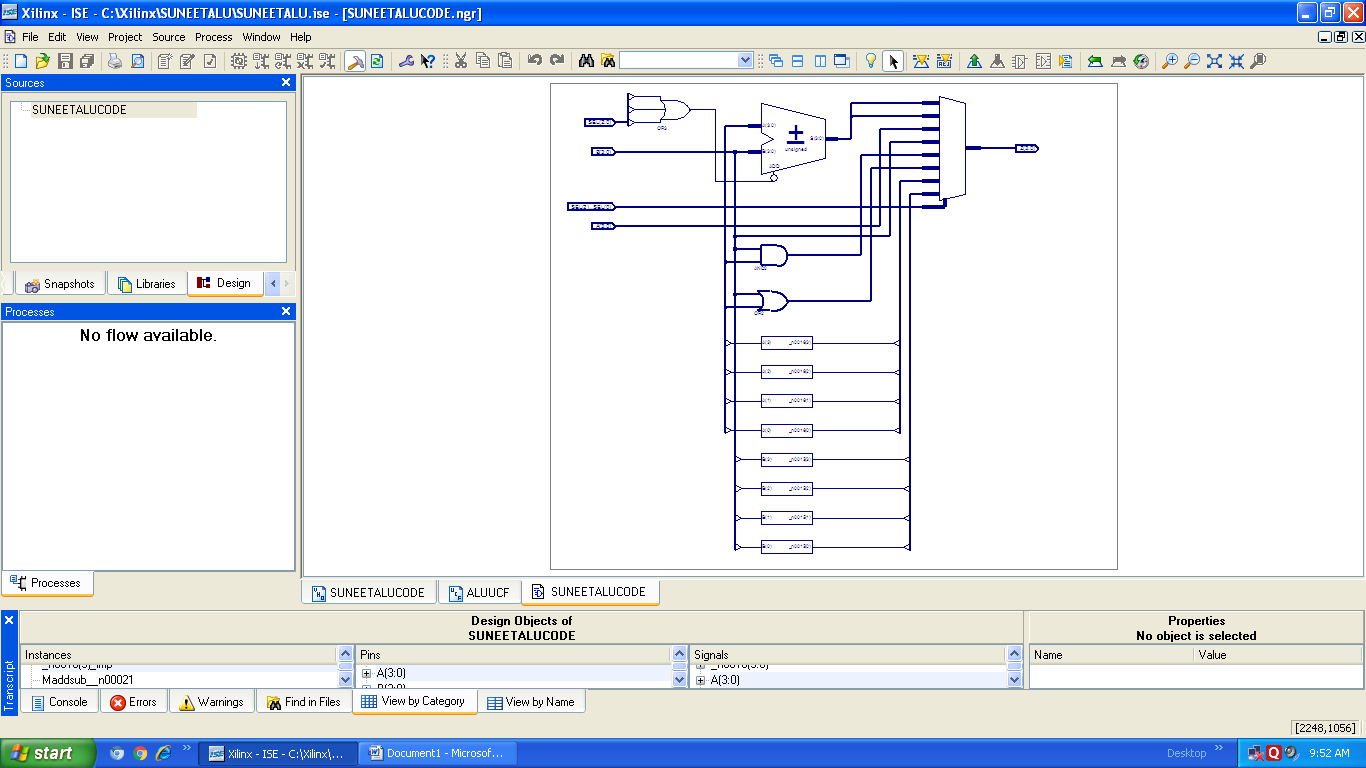
net "Z(3)" LOC = P165;

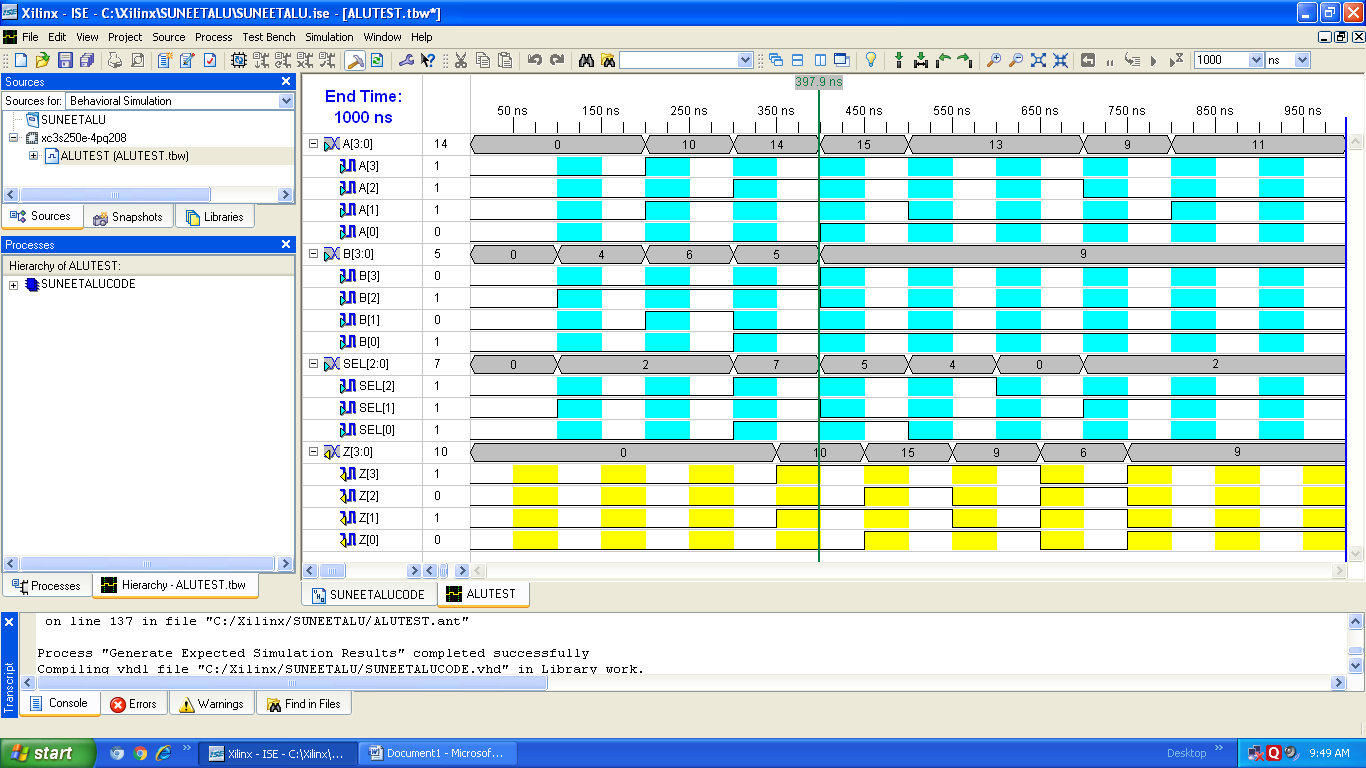
net "Z(2)" LOC = P167;

net "Z(1)" LOC = P163;

net "Z(0)" LOC = P164;

**OUTPUT:**

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**EXPERIMENT NO: 3 FIFO**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

ENTITY FIFO12 is

port(clk:in std\_logic;

enr : in std\_logic;

enw : in std\_logic;

dataout: out std\_logic\_vector(3 downto 0);

datain: in std\_logic\_vector(3 downto 0);

empty : out std\_logic;

full : out std\_logic);

end FIFO12;

architecture Behavioral of FIFO12 is

type memory\_type is array(0 to 7) of std\_logic\_vector(3 downto 0);

signal memory : memory\_type;

signal readptr,writeptr: std\_logic\_vector(3 downto 0):="0000";

begin

process(clk)

begin

if(clk'event and clk='1' and enw='1')then

memory(conv\_integer(writeptr))<=datain;

writeptr<=writeptr + '1';

end if;

if(clk'event and clk='1' and enr='1')then

dataout <= memory(conv\_integer(readptr));

readptr<=readptr + '1';

end if;

if(readptr="1000")then

empty<='1';

readptr<="0000";

else

empty<='0';

end if;

if(writeptr="1000")then

full<='1';

writeptr<="0000";

else

full<='0';

end if;

end process;

end Behavioral;

**UCF FILE:**

net "clk" LOC = P205;

net "enr" LOC = P206;

net "enw" LOC = P203;

net "dataout(3)" LOC = P192;

net "dataout(2)" LOC = P193;

net "dataout(1)" LOC = P189;

net "dataout(0)" LOC = P190;

net "datain(3)" LOC = P179;

net "datain(2)" LOC = P180;

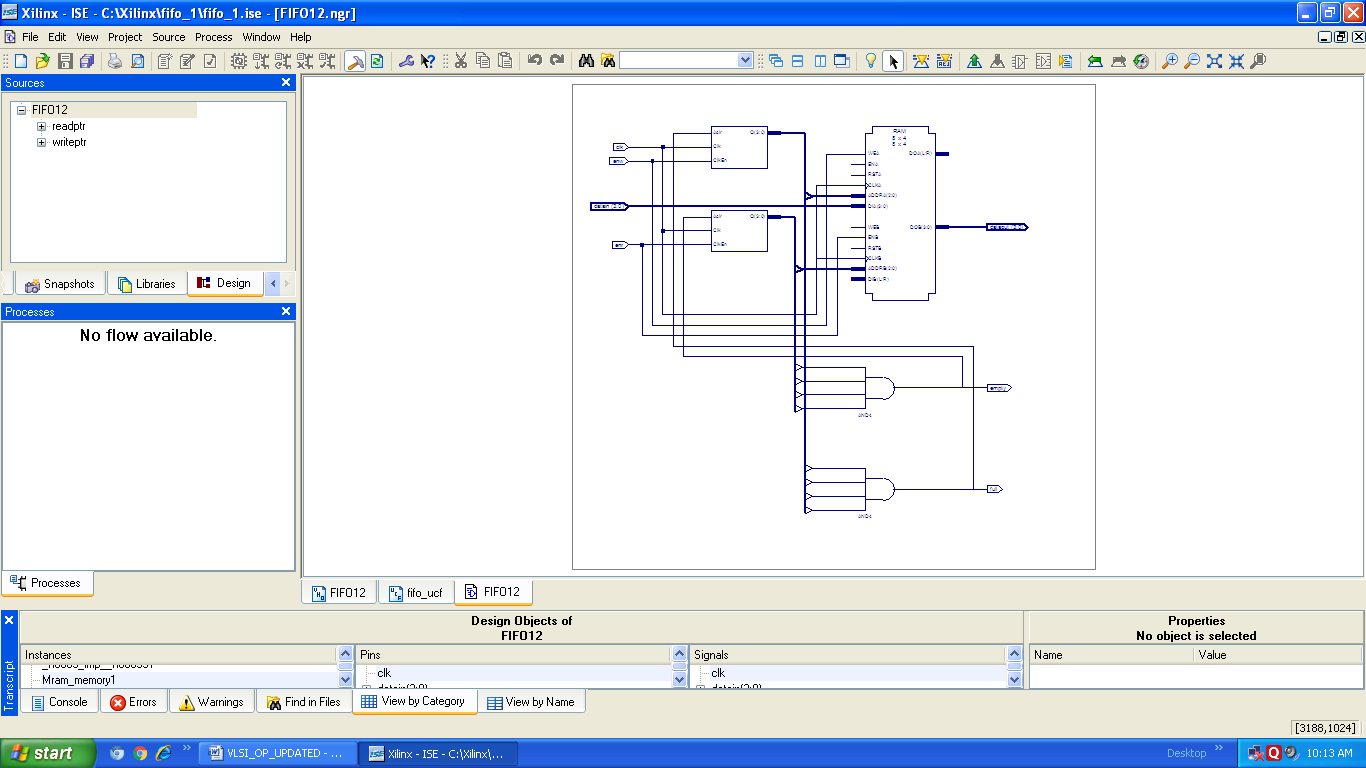
net "datain(1)" LOC = P177;

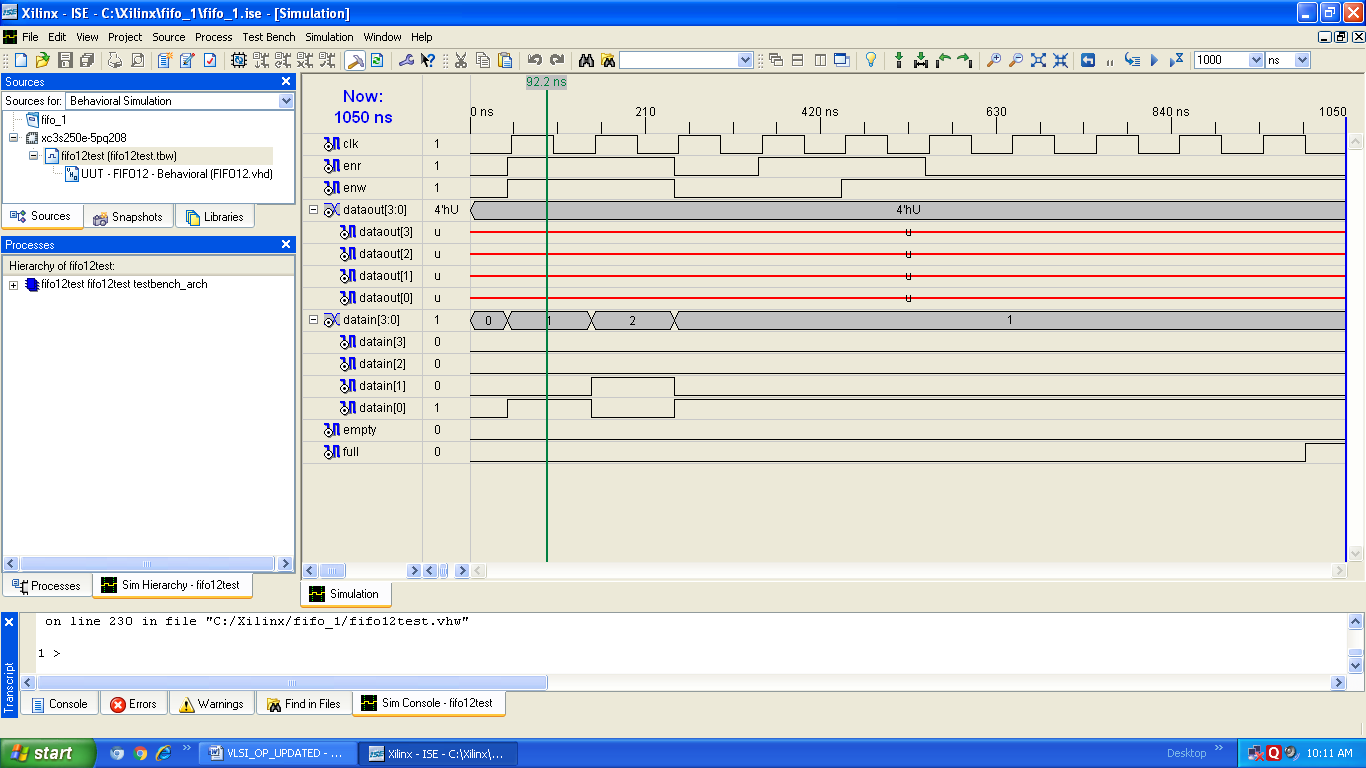
net "datain(0)" LOC = P178;

net "empty" LOC = P167;

net "full" LOC = P163;

**OUTPUT:**

****

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**EXPERIMENT NO: 2 UNISHIFT**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity unishift\_123 is

Port ( Pin : in STD\_LOGIC\_VECTOR (3 downto 0);

Pout : out STD\_LOGIC\_VECTOR (3 downto 0);

mode : in STD\_LOGIC\_VECTOR (1 downto 0);

clk : in STD\_LOGIC;

rst : in STD\_LOGIC;

Sin : in STD\_LOGIC;

Sout : out STD\_LOGIC);

end unishift\_123;

architecture Behavioral of unishift\_123 is

signal tmp : std\_logic\_vector (3 downto 0);

begin

process(clk,rst)

begin

if(rst='1')then

tmp<="0000";

elsif rising\_edge(clk)then

if mode="01" then

tmp(0)<=Sin;

tmp(1)<=tmp(0);

tmp(2)<=tmp(1);

tmp(3)<=tmp(2);

elsif mode="10" then

tmp(3)<=Sin;

tmp(2)<=tmp(3);

tmp(1)<=tmp(2);

tmp(0)<=tmp(1);

elsif mode="11" then

tmp<=Pin;

end if;

end if;

end process;

Pout<=tmp;

Sout<=tmp(3);

end Behavioral;

**UCF FILE:**

net "Pin(3)" LOC = P205;

net "Pin(2)" LOC = P206;

net "Pin(1)" LOC = P203;

net "Pin(0)" LOC = P200;

net "Pout(3)" LOC = P192;

net "Pout(2)" LOC = P193;

net "Pout(1)" LOC = P189;

net "Pout(0)" LOC = P190;

net "mode(1)" LOC = P179;

net "mode(0)" LOC = P180;

net "clk" LOC = P165;

net "rst" LOC = P167;

net "Sin" LOC = P163;