COM Express Technical Manual
&
Baseboard Design Guide
Version 3.1

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Chapter 1

1. User Information

1.1 About This Document

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Chapter 2

2. Introduction

A Computer-On-Module, or COM, is a Module with all components necessary for a bootable host computer, packaged as a super component. A COM requires a Baseboard to bring out I/O and to power up. COMs are used to build single board computer solutions and offer OEMs fast time-to-market with reduced development cost. Like integrated circuits, they provide OEMs with significant freedom in meeting form-fit-function requirements. For all these reasons the COM methodology has gained much popularity with OEMs in the embedded industry.

COM Express® is an open industry standard for Computer-On-Modules. Key features include:

· Rich complement of contemporary high bandwidth serial interfaces, including PCI Express, Serial ATA, USB, and Gigabit Ethernet

· Extended power-management capabilities

· Robust thermal and mechanical concept

· Cost-effective design

· Legacy-free design (no Super I/O, PS2 keyboard or mouse)

· Small Module size with multiple footprint options to satisfy a range of performance requirements

· High-performance mezzanine connector with several pin-out types to satisfy a range of applications

· Extensive video port support, including VGA, LVDS, DP, DVI and HDMI termination drivers plus x16 PEG port to Baseboard graphics controller

The COM Express® specification has been created to appeal to a range of vertical embedded markets. It has also been formulated to be applicable to a broad range of form factors, from floor-installed to bench-top to handheld. Markets and applications include but are not limited to:

· Healthcare - clinical diagnostic imaging systems, patient bedside monitors, etc.

· Retail & advertising - electronic shopping carts, billboards, kiosks, POS systems, etc.

· Test & measurement - scientific and industrial test and measurement instruments

· Gaming & entertainment - simulators, slot machines, etc.

· Industrial automation - industrial robots, vision systems, etc.

· Security - digital CCTV, luggage scanners, intrusion detectors, etc.

· Defense & government - unmanned vehicles, rugged laptops, wearable computers, etc.

Systems based on the COM Express® Specification require the implementation of an application-specific Baseboard that accepts the Module. User-specific features such as external connector choices and locations and peripheral circuits can be tailored to suit the application. The OEM can focus on application-specific features rather than CPU board design. The OEM also benefits from a wide choice of Modules providing a scalable range of price and performance upgrade options.

2.1 COM Express® Specification and COM Express Design Guide

The COM Express® Specification defines requirements for highly integrated compact modules with standard I/O interfaces and connections, which allows interoperability between multi-sourced modules.

Key capabilities defined in the COM Express® Specification include support for:

- PCI Express Bus
- PCI Express Graphics (PEG)
- Serial ATA
- USB 2.0/3.0
- Gigabit Ethernet
- DDI interface

The COM Express® Specification defines four form factors:

- Mini (84mm x 55mm) Module
- Compact (95mm x 95mm) Module
- Basic (125mm x 95mm) Module
- Extended (155mm x 110mm) Module

The Mini Module targets the next generation of mobile applications that require energy saving processors, high-end graphics combined with longer battery life.

The mechanical envelope for the Basic Module is defined for low-profile, space-constrained applications.

Compact/Basic Modules usually use a single (or two stacked) horizontal mount SO-DIMM

Extended Modules target applications that require more memory and high-performance CPUs and chipsets. Two full-size DIMMs fit on an Extended Module.

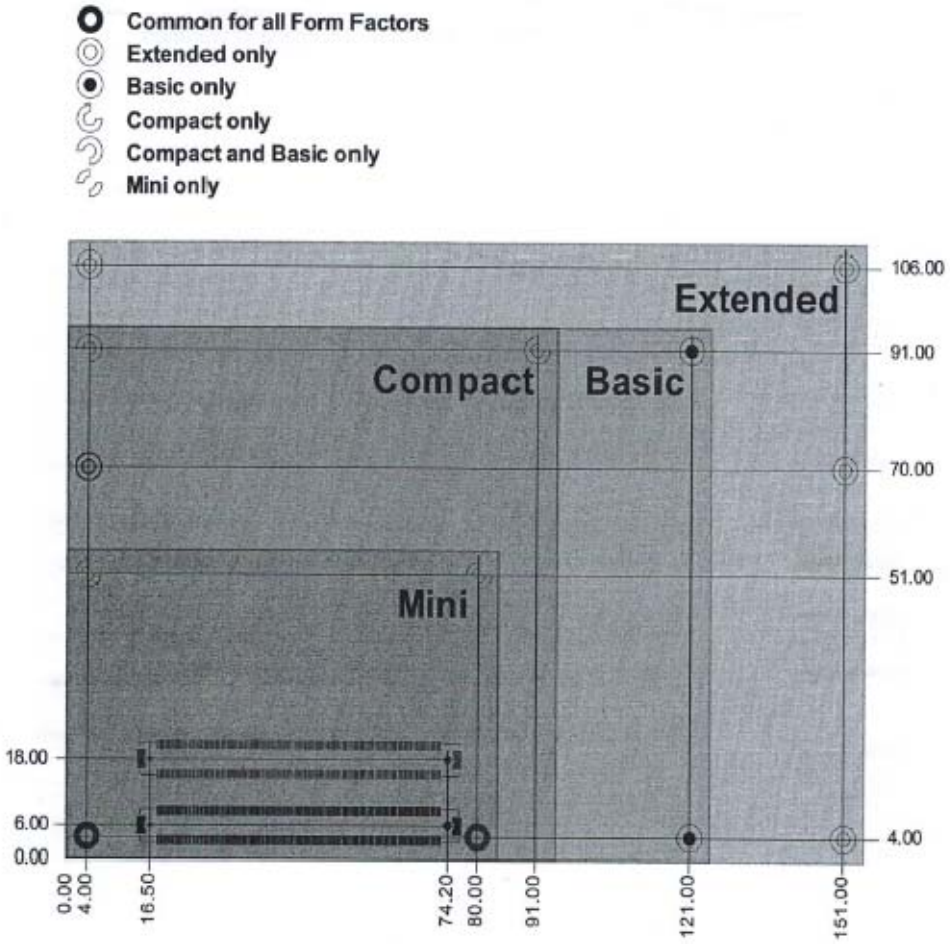
Module Pin-out Type Definitions:

- Module Types 6 supports two connectors with four rows of pins (440 pins total).
- Module Type 10 supports a single connector with two rows of pins (220 pins total).

Connector placement and most mounting holes have transparency between Form Factors.

The mounting positions and connector location for Baseboard is shown in figure 2-1 below.

Figure 2-1 Mounting positions and connector location for Baseboard



The differences among the Module Type 6 & Type 10 are summarized in Table 2-1.

Table 2-1 Module Type Summary Features

Types	Connector Rows	PCI Express Lanes	PEG	SATA Ports	LAN Ports	USB2.0/ SuperSpeed USB	Display Interfaces
Type 6	A-B C-D	Up to 24	1	4	1	8/4	VGA, LVDS, PEG, 3xDDI
Type 10	A-B	Up to 4	NA	2	1	8/2	LVDS, 1xDDI

COM Express Type 6 & Type 10 Required and Optional features are summarized in Table 2-2 & Table 2-3.

Table 2-2 Module Pin-out Required and Optional Features A-B Connecter

Connector	Feature	Type 6 Min/Max	Type 10 Min/Max
A-B	System I/O		
A-B	PCI Express Lanes	1/6	1/4
A-B	LVDS Channel A	0/1	0/1
A-B	LVDS Channel B	0/1	N/A
A-B	VGA Port	0/1	N/A
A-B	DDI	0/3	0/1
A-B	Serial Ports 1-2	0/2	0/2
A-B	SATA Ports	1/4	1/2
A-B	AC'97 / HAD Digital Interface	0/1	0/1
A-B	USB2.0 Ports	4/8	4/8
A-B	USB3.0 Ports	0/4	0/2
A-B	LAN Port0	1/1	1/1
A-B	Express Card Support	1/2	0/2
A-B	LPC Bus	1/1	1/1
A-B	SPI	1/2	1/2
A-B	System Management		
A-B	General Purpose I/O	8/8	8/8
A-B	SMBus	1/1	1/1
A-B	Watchdog Timer	0/1	0/1
A-B	Speaker Out	1/1	1/1
A-B	External BIOS ROM Support	0/2	0/2
A-B	Reset Functions	1/1	1/1
A-B	Power Management		
A-B	Thermal Protection	0/1	0/1
A-B	Battery Low Alarm	0/1	0/1
A-B	Suspend/Wake Signals	0/3	0/3
A-B	Power Button Support	1/1	1/1
A-B	Power Good	1/1	1/1
A-B	VCC_5V_SBY Contacts	4/4	4/4
A-B	Sleep Input	0/1	0/1
A-B	Lid Input	0/1	0/1
A-B	Fan Control Signals	0/2	0/2
A-B	Trusted Platform Modules	0/1	0/1
A-B	Power		
A-B	VCC_12V Contacts	12/12	12/12

Table 2-3 Module Pin-out Required and Optional Features C-D Connecter

Connector	Feature	Type 6 Min/Max	Type 10 Min/Max
C-D	System I/O		
C-D	PCI Express Lanes 16-31	0/16	N/A
	PCI Express Graphics(PEG)	0/1	N/A
C-D	PCI Express Lanes	0/2	N/A
C-D	DDIs 1-3	0/3	N/A
C-D	USB 3.0 Ports	0/4	N/A
C-D	Power		
C-D	VCC_12V Contacts	12/12	N/A

The Axiomtek Design Guide for COM Express Baseboards serves as a general guide for Baseboard designs. The Design Guide focuses on maximum flexibility to accommodate a range of COM Express Modules. The Axiomtek COM Express Design Guide explores the requirements of the COM Express® Specification and provides recommendations on how to design COM Express Baseboards to support features of Axiomtek COM Express Modules.

The Baseboard Design Guide provides schematic examples and information on standard I/O interfaces, connections, and routing. The guide also offers ideas to maximize the design potential of COM Express Baseboards to accommodate all Axiomtek COM Express Modules.

COM Express Module User Guides document specifications and features of an individual COM Express Module. You can find all user guides for COM Express Modules on the Axiomtek Technical Portal (ATP) Website.

Axiomtek ATP website at http://atp.axiomtek.com.tw/atp/

2.2 Acronyms / Definitions

Acronyms and terms used in this document are defined in the table below.

Table 2-4 Terms and Definitions

Term	Definition
AC '97	Audio CODEC (Coder-Decoder)
ACPI	Advanced Configuration Power Interface – standard to implement power saving modes in PC-AT systems
Basic Module	COM Express® 125mm x 95mm Module form factor.
BIOS	Basic Input Output System – firmware in PC-AT system that is used to initialize system components before handing control over to the operating system.
Baseboard	An application specific circuit board that accepts a COM Express® Module.
CCTV	Closed Circuit Television
Compact Module	COM Express® 95x95 Module form factor
DDC	Display Data Control – VESA (Video Electronics Standards Association) standard to allow identification of the capabilities of a VGA monitor
DDI	Digital Display Interface – containing DisplayPort, HDMI/DVI and SDVO
DIMM	Dual In-line Memory Module
DisplayPort	DisplayPort is a digital display interface standard put forth by the Video Electronics Standards Association (VESA). It defines a new license free, royalty free, digital audio/video interconnect, intended to be used primarily between a computer and its display monitor.
DRAM	Dynamic Random Access Memory
DVI	Digital Visual Interface - a Digital Display Working Group (DDWG) standard that defines a standard video interface supporting both digital and analog video signals. The digital signals use TMDS.
EEPROM	Electrically Erasable Programmable Read-Only Memory
Extended Module	COM Express® 155mm x 110mm Module form factor.
Gb	Gigabit
GBE	Gigabit Ethernet
GPI	General Purpose Input
GPIO	General Purpose Input Output
GPO	General Purpose Output
HDA	Intel High Definition Audio (HD Audio) refers to the specification released by Intel in 2004 for delivering high definition audio that is capable of playing back more channels at higher quality than AC97.
HDMI	High Definition Multimedia Interface
I2C	Inter Integrated Circuit – 2 wire (clock and data) signaling scheme allowing communication between integrated circuits, primarily used to read and load register values.

Term	Definition
Legacy Device	Relics from the PC-AT computer that are not in use in contemporary PC systems: primarily the ISA bus, UART-based serial ports, parallel printer ports, PS-2 keyboards, and mice. Definitions vary as to what constitutes a legacy device. Some definitions include IDE as a legacy device
LAN	Local Area Network
LPC	Low Pin-Count Interface: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy-device support into a single IC.
LVDS	Low Voltage Differential Signaling – widely used as a physical interface for TFT flat panels. LVDS can be used for many high-speed signaling applications. In this document, it refers only to TFT flat-panel applications.
Mini Module	COM Express® 84mm x 55mm Module form factor.
NA	Not Available
NC	No Connect
NI-	No Install. Used in the schematics.
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board
PCI Express PCIE	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
PEG	PCI Express Graphics
Pin-out Type	A reference to one of seven COM Express® definitions for the signals that appear on the COM Express® Module connector pins.
PS2 PS2 Keyboard PS2 Mouse	"Personal System 2" - an IBM trademark term used to refer to Intel x86 based personal computers in the 1990s. The term survives as a reference to the style of mouse and keyboard interface that were introduced with the PS2 system.
RTC	Real Time Clock – battery backed circuit in PC-AT systems that keeps system time and date as well as certain system setup parameters
SPD	Serial Presence Detect – refers to serial EEPROM on DRAMs that has DRAM Module configuration information
SPI	Serial Peripheral Interface
SO-DIMM	Small Outline Dual In-line Memory Module
SATA	Serial AT Attachment: serial-interface standard for hard disks
SMBus	System Management Bus
Super I/O	An integrated circuit, typically interfaced via the LPC bus that provides legacy PC I/O functions including PS2 keyboard and mouse ports, serial and parallel port(s) and a floppy interface.
TMDS	Transition Minimized Differential Signaling - a digital signaling protocol between the graphics subsystem and display. TMDS is used for the DVI digital signals.
TPM	Trusted Platform Module, chip to enhance the security features of a computer system.
USB	Universal Serial Bus
VGA	Video Graphics Adapter – PC-AT graphics adapter standard defined by IBM.
WDT	Watch Dog Timer.

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Chapter 3

3. COM Express Baseboard PCB/Layout Design

3.1 PCB Design Rules

The COM Express® Specification provides a rich set of modern, high-speed differential serial interfaces.

Designing COM Express Baseboards is not difficult, but certain design rules must be followed.

The most important design rule is: route high-speed serial interfaces as differential pairs. The two lines in the pair must be length-matched and should have uniform edge-to-edge spacing. They should have a minimum of layer changes. If they do change layers, both lines in the pair should change. The preferred reference plane for the high-speed pairs is a single, continuous GND plane.

3.2 Trace-Impedance Considerations

Most high-speed interfaces used in a COM Express design for a Baseboard are differential pairs that need a well-defined and consistent differential and single-ended impedance. The differential pairs should be edge-coupled (i.e. the two lines in the pair are on the same PCB layer, at a consistent spacing to each other). Broadside coupling (in which the two lines in the pair track each other on different layers) is not recommended for mainstream commercial PCB fabrication.

There are two basic structures used for high-speed differential and single-ended signals. The first is known as a "microstrip", in which a trace or trace pair is referenced to a single ground plane.

The outer layers of multi-layer PCBs are microstrips. A diagram of a microstrip cross section is shown in Figure 3-1 below.

The second structure is the "strip-line" in which a trace or pair of traces is sandwiched between two reference planes, as shown in Figure 3-2 below. If the traces are exactly halfway between the reference planes, then the strip-line is said to be symmetric or balanced. Usually the traces are a lot closer to one of the planes than the other (often because there is another, orthogonal, trace layer, which is not shown in Figure 3-2). In this case, the strip-lines are said to be asymmetric or un-balanced. Inner layer traces on multi-layer PCBs are usually asymmetric strip-lines.

Before proceeding with a Baseboard layout, designers should decide on a PCB stack-up and on trace parameters, primarily the trace-width and differential-pair spacing. It is quite a bit harder to change the differential impedance of a trace pair after layout work is done than it is to change the impedance of a single-ended signal. That is because (with reference to Figures 3-1, and Table 3-1 below) the geometric factors that have the biggest impact on the impedance of a single-ended trace are H1 and W1.Both H1 and W1 can be manipulated slightly by the PCB vendor. The differential impedance of a trace pair depends primarily on H1, W1 and the pair pitch. A PCB vendor can easily manipulate H1 and W1 but changing the pair pitch cannot generally be done at fabrication time. It is more important for the PCB designer and the Project Engineer to determine the routing parameters for differential pairs ahead of time.

Work with a PCB vendor on a suitable board stack-up and do your own homework using a PCB-impedance calculator. An easy to use and comprehensive calculator is available from Polar Instruments (www.polarinstruments.com). Many PCB vendors use software from Polar Instruments for their calculations. Polar Instruments offers an impedance calculator on a low-cost, per-use basis. To find this, search the Web for a "Polar Instruments subscription". Alternatively, impedance calculators are included in many PCB layout packages, although these are often incomplete when it comes to differential-pair impedances. There also are quite a few free impedance calculators available on the Web. Most are very basic, but they can be useful.

Figure 3-1 Microstrip Cross Section

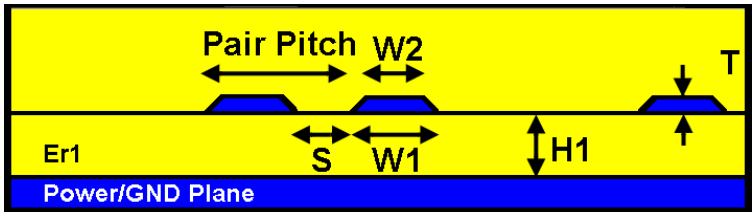

Figure 3-2 Asymmetric Strapline Cross Section

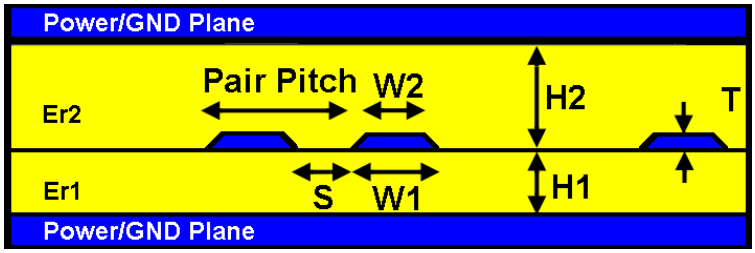

Table 3-1 Microstrip and strapline Definitions

Symbol	Definition
Er1	Dielectric constant of material between the trace and the reference plane. Increasing Er1 results in a lower trace impedance.
Er2	Dielectric constant of the material between the 2nd reference plane (strapline case only). Usually Er1 and Er2 are the same. Increasing Er2 results in a lower trace impedance. Distance between the trace lower surface and the closer reference plane. Increasing H1 raises the trace impedance (assuming that H1 is less than H2).
H1	
H2	Distance between the trace lower surface and the more distant reference plane (strapline case only). Usually H2 is significantly greater than H1. When this is true, the lower plane shown in the figure is the primary reference plane. Increasing H2 raises the trace impedance.
Pair Pitch	The center-to-center spacing between two traces in a differential pair. Increasing the pair pitch raises the differential trace impedance.
S	The spacing or gap between two traces in a differential pair. The pair pitch is the sum of S and W1. Increasing S raises the differential trace impedance.
T	The thickness of the trace. The thickness of a ½ oz. inner layer trace is about 0.0007 inches. The thickness of a 1 oz. inner layer trace is about 0.0014 inches. Outer layer traces using a given copper weight are thicker, due to plating that is usually done on outer layers. Increasing the trace thickness lowers trace impedance.
W1、W2	W1 is the base thickness of the trace. W2 is the thickness at the top of the trace. The relation between W1 and W2 is called the “etch factor” in the PCB trade. For rough calculations, it can be assumed that W1 = W2. The etch factor is process dependent. W2 is often about 0.001 inches less than W1 for ½ Oz inner layer traces For example, a 5 mil (0.005 inch) nominal trace will be 5-mil wide at the bottom and 4-mil wide at the top. Increasing the trace-width lowers trace impedance.

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Chapter 4

4. COM Express Baseboard Connectors

4.1 Connector Descriptions

Descriptions, part numbers, and land patterns for COM Express Connectors are provided in the COM Express® Specification. The discussion below augments the description given in the Specification.

COM Express Baseboards that implement Pin-out Type 6 use a pair of 220-pin, 0.5mm-pitch, surface-mount connectors for a total of 440 pins. Each connector has two rows of 110 pins. For the full 440-pin implementation, there are four rows of 110 pins each. The four rows are labeled A, B, C and D in the COM Express® Specification. The two 220-pin connectors are referred to as the 'A-B' connector and the 'C-D' connector. Only Type 10 Module uses a single 220-pin connector, the 'A-B' connector.

4.2 Connector Land Patterns and Alignment

It is extremely important that the designers of Baseboards ensure that the COM Express connectors have the proper land patterns and that the connectors are aligned correctly. Connector alignment is ensured if the peg location holes in the PCB connector pattern are in the correct positions and if the holes are drilled to the proper size and tolerance by the PCB fabricator.

4.3 Connector and Module CAD Symbol Recommendations

The 440-pin COM Express® Type 6 connector should be shown in the Baseboard CAD system as a single schematic symbol and a single PCB symbol, rather than as a pair of 220-pin symbols. This ensures that the relative position of the two 220-pin connectors' remains correct as PCB placement for the Baseboard is done.

It also is very advantageous to extend this concept to include the COM Express Module outline and the Module mounting holes in the same PCB land pattern. This allows PCB designers to easily move the entire module around to try placement options without losing the relative positions and orientations of the Module connectors, mounting holes, and Module outline.

4.4 Connector Schematics

The following schematics show available signals for the COM Express connector pins for Connector Rows A, B, C and D as defined in the COM Express® Specification for Type 6 and Type 10 pin-outs. The schematics show available and unused signals. The schematics of Type 6 pin-out with connector row A-B and row C-D can be seen in figure 4-1 and figure 4-2. In figure 4-3 is the schematic of Type 10 pin-out with connector row A-B.

Figure 4-1COM Express® Connector Row A-B Schematic(Type 6 Pin-Out)

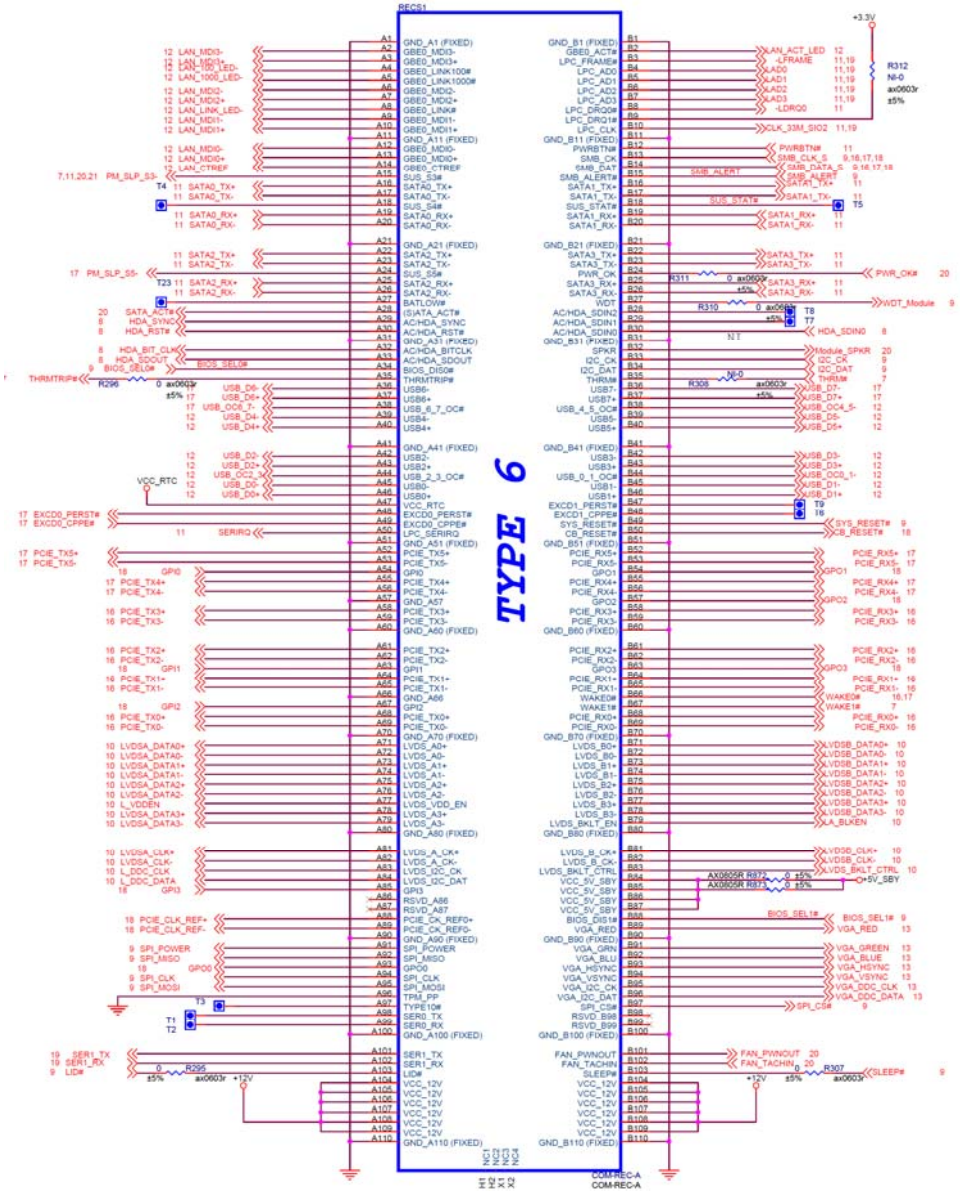


Figure 4-2 COM Express® Connector Row C-D Schematic(Type 6 Pin-Out)

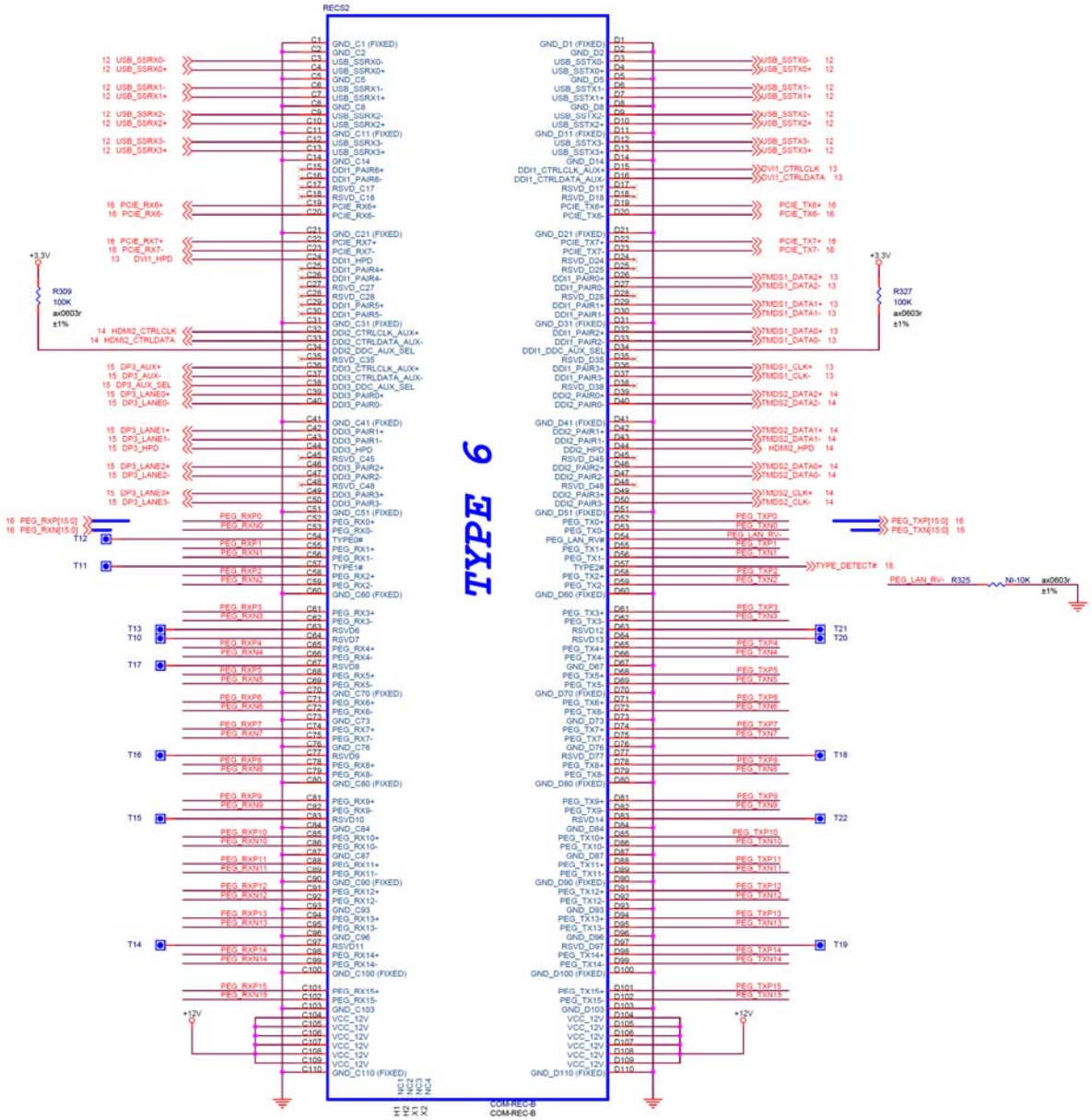
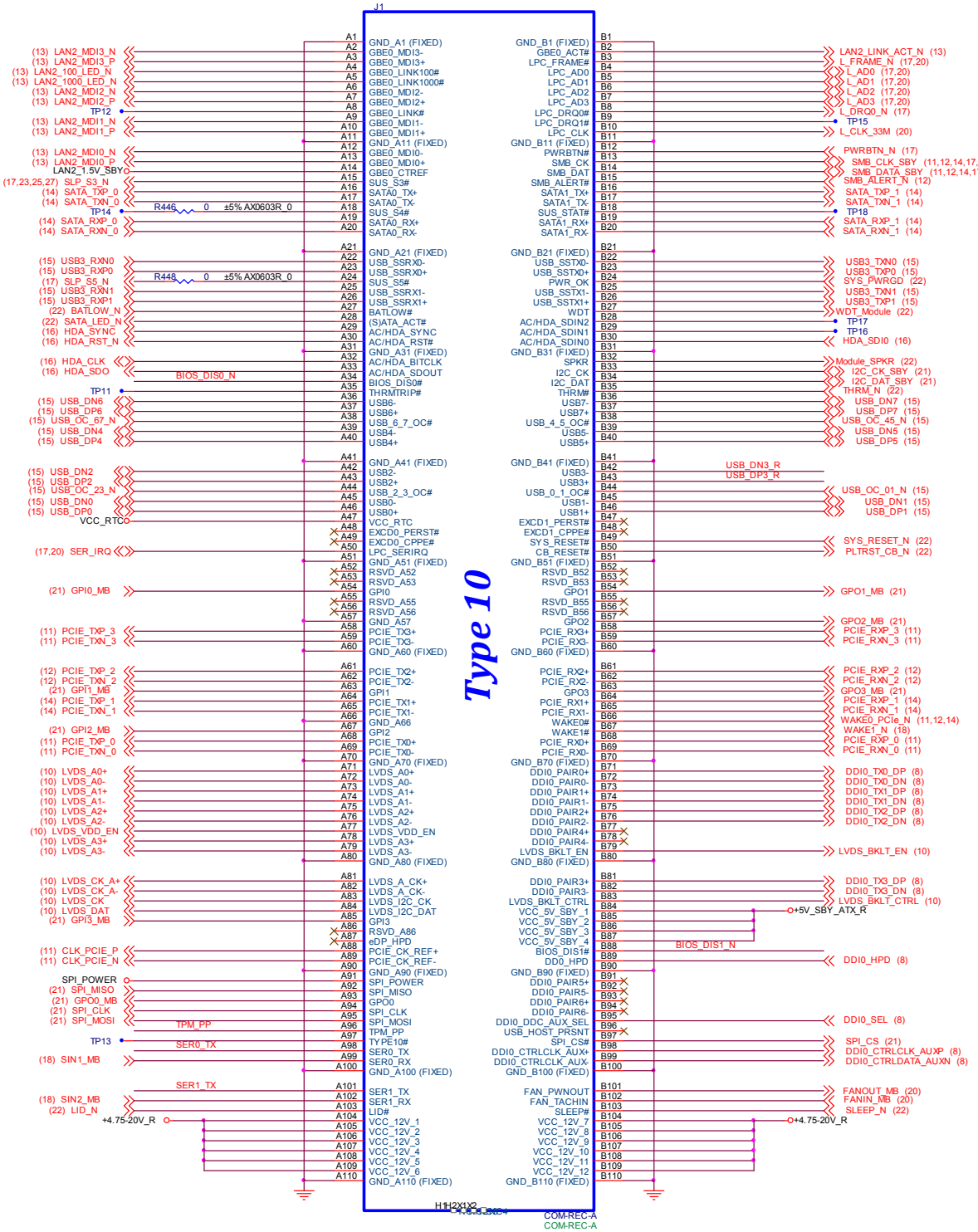


Figure 4-3 COM Express® Connector Row A-B Schematic(Type 10 Pin-Out)



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Chapter 5

5. PCIe Lanes

5.1 PCIe Lanes – Signal Definitions

The COM Express® Specification defines PCI Express™ (PCIe™) lanes on the A-D Connector. The manner in which lanes are grouped can vary with each Module. A lane "fill order" is described in the COM Express® Specification.

Table 5-1 Axiomtek PCIe Lanes Pin-outs

	Type 6		Type 10	
Pin	**Row A**	**Row B**	**Row A**	**Row B**
51				
52	PCIE_TX5+	PCIE_RX5+		
53	PCIE_TX5-	PCIE_RX5-		
54				
55	PCIE_TX4+	PCIE_RX4+		
56	PCIE_TX4-	PCIE_RX4-		
57				
58	PCIE_TX3+	PCIE_RX3+	PCIE_TX3+	PCIE_RX3+
59	PCIE_TX3-	PCIE_RX3-	PCIE_TX3-	PCIE_RX3-
60				
61	PCIE_TX2+	PCIE_RX2+	PCIE_TX2+	PCIE_RX2+
62	PCIE_TX2-	PCIE_RX2-	PCIE_TX2-	PCIE_RX2-
63				
64	PCIE_TX1+	PCIE_RX1+	PCIE_TX1+	PCIE_RX1+
65	PCIE_TX1-	PCIE_RX1-	PCIE_TX1-	PCIE_RX1-
66				
67				
68	PCIE_TX0+	PCIE_RX0+	PCIE_TX0+	PCIE_RX0+
69	PCIE_TX0-	PCIE_RX0-	PCIE_TX0-	PCIE_RX0-
70				

	Type 6	
Pin	**Row C**	**Row D**
18		
19	PCIE_RX6+	PCIE_TX6+
20	PCIE_RX6-	PCIE_TX6-
21		
22	PCIE_RX7+	PCIE_TX7+
23	PCIE_RX7-	PCIE_TX7-

5.2 PCIe Lanes – Routing Considerations

PCI Express (PCIe) signals are high-speed differential pairs with a nominal 85Ω differential impedance. Route them as differential pairs, preferably referenced to a continuous GND plane with a minimum of via transitions.

PCIe pairs need to be length-matched within a given pair ("intra-pair"), but the different pairs do not need to be matched ("inter-pair").

PCB design rules for these signals are summarized in Appendix A.

The transmit pairs are designated as PCIE_TX0+ and PCIE_TX0- thru PCIE_TX7+ and PCIE_TX7-. Transmit in this context means that the signals are transmitted out of the Module. No coupling capacitors are needed on Baseboard PCIe transmit lines. The coupling caps are located on the Module.

The receive pairs are designated PCIE_RX0+ and PCIE_RX0- thru PCIE_RX7+ and PCIE_RX7-. Receive in this context means that the signals are received by the Module. Coupling capacitors are needed on the Baseboard on these lines if the PCIe target device is "down" on the Baseboard. Locate the coupling capacitors near the transmit pins of the Baseboard's PCIe target device. If the PCIe target device is on a slot card (device "up"), no coupling caps are needed on the lines on the Baseboard because the coupling caps will be on the slot card.

Parameter	Trace Louting
Differential Impedance	85 Ω ±15%
Single-End Impedance	50 Ω ±10%
Signal length	9.0 inches (Gen2) 4.0 inches (Gen3)
Spacing between RX and TX pairs (inter-pair)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between reference clock differential pairs REFCLK+ and REFCLK-	Max. 5mils
Reference plane	GND
Via Usage	Gen2: Max. 2 vias per TX trace Max. 4 vias per RX trace Gen3: Max. 2 vias / TX Max. 4 vias / RX (to device) Max. 2 vias / RX (to slot)

5.2.1 PCIe Polarity Inversion

Per the PCI Express Card Electromechanical Specification, all PCIe devices must support polarity inversion on each PCIe lane, independently of the other lanes. This means that, for example, you can route the Module PCIE_TX1+ signal to the corresponding '-,N' pin on the slot or target device, and the PCIE_TX1- signal to the corresponding '+,P' pin. If this makes the layout cleaner, with fewer layer transitions and better differential pairs, then take advantage of this PCIe feature.

5.2.2 PCIe Lane Reversal

Per the PCI Express Card Electromechanical Specification, all PCIe Cards optionally support lane reversal. Lane reversal means that, for example, in a x4 PCIe link, the '1' pair can route to the target device '4' pins; the '2' pair to the target '3' pins, the '3' to the target '2' pins, and the '4' pair to the target '1' pins. If this is done, it must be done with both the transmit and receive pairs.

The COM Express® Specification does not require lane-reversal support and PCIe lane groups except for the PCI Express Graphics (PEG) group. This group is described in Section 6 below.

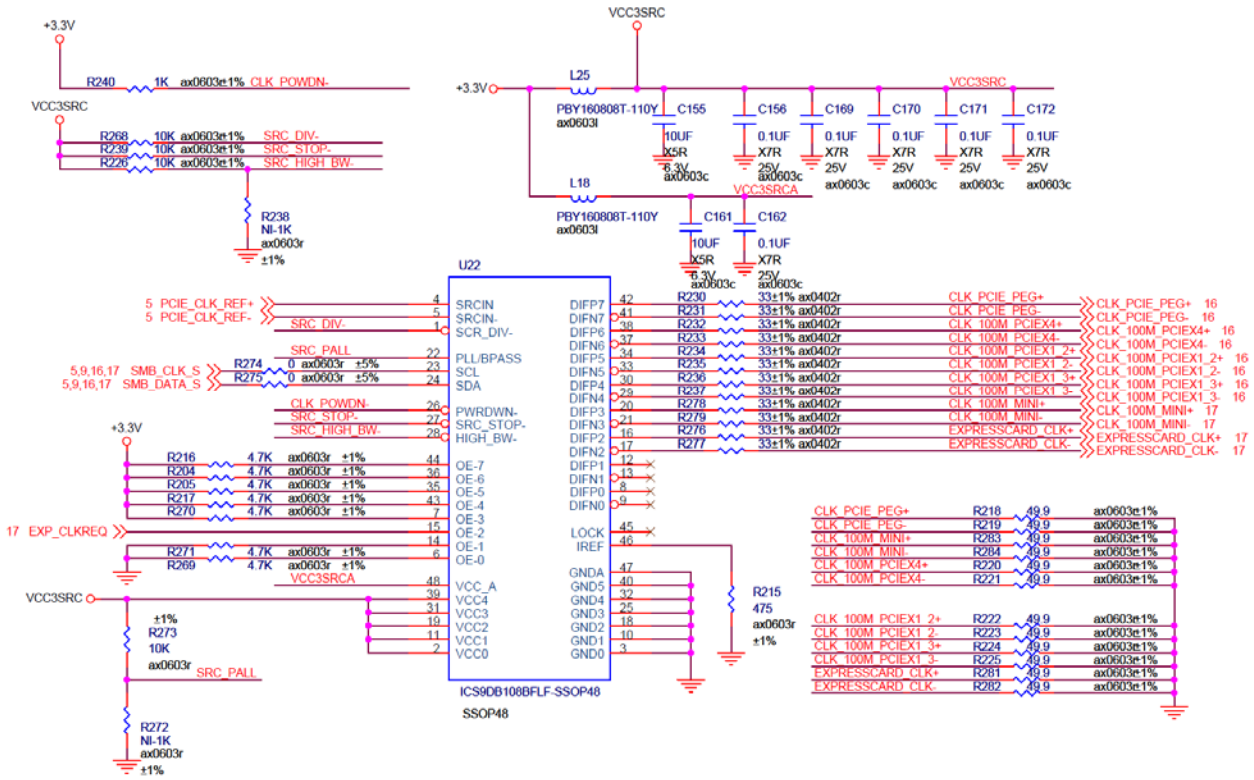
5.2.3 PCIe Reference Clock Buffer Example

The COM Express® Specification calls for one copy of the PCIe reference clock pair to be brought out of the Module. This clock is a 100MHz differential pair and is sometimes known as a "hint" clock. The clock allows the PLL in the target PCIe device to lock faster onto the embedded clock in the PCIe bit stream.

If the Baseboard implements only one PCIe device or slot, then the PCIe reference clock pair from the Module may be routed directly to that device or slot. However, if there are two or more PCIe devices or slots on the Baseboard, then the Module PCIe reference clock should be buffered using a PLL based "zero-delay" buffer. Such devices are available from ICS (Integrated Circuits Systems), Cypress Semiconductor, and others.

The ICS9DB403, ICS9DB108 have four and eight differential output replicas of the input clock, respectively. Each target device (PCIe "device down" chip, slot, Express Card slot, PEG slot) should get an individual copy of the reference clock.

Figure 5-1 PCIe Reference Clock Buffer Schematic



The following notes apply to Figure 5-1 above.

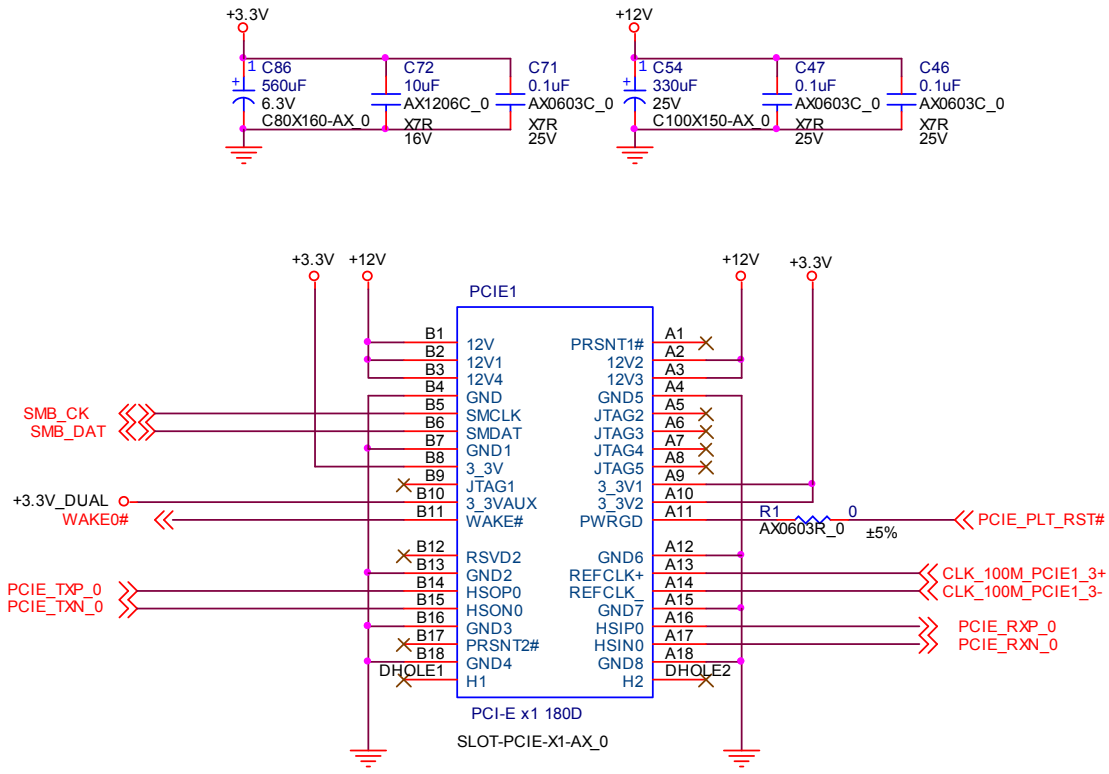
- Nets PCIE_CLK_REF+ and PCIE_CLK_REF- are sourced from COM Express Module pins A88 and A89 respectively.
- Each clock pair is routed point to point to each connector or end device using differential signal routing rules.
- Each clock output pair from the ICS buffer are terminated close to the ICS buffer pins with a series resistor (shown as 33Ω) and a termination to GND (shown as 49.9Ω).
- SM Bus nets SMB_CLK_S and SMB_DATD_S are sourced from COM Express Module pins B13 and B14 respectively.

- SM Bus software can control the PLL bandwidth or bypass the PLL for board tests.
- SM Bus software can enable or disable clock-buffer outputs. Disable unused outputs to reduce emissions.
- ICS chip pins OE0~7 are pulled high to enable ICS outputs DIFN0~DIFN7 and DIFP0~DIFP7 ('P' and 'N' stand for 'Passive' and 'Native' in the ICS names) in hardware, rather than by software.
- The ICS chip IREF pin (pin 46) is pulled low thru the 475Ω fixed precision resistor to establish the reference current for differential current-mode output pairs.
- The ICS chip PLL_BW pin (pin 28) is pulled high to enable a high bandwidth option on the PLL.

5.2.4 PCIe x1 Slot Example

An example of an x1 PCIe slot is shown in Figure 5-2 below. A PCIe x1 slot is commonly used for GBE slot cards. The source specification for slot implementations is the PCI-SIG "PCI Express Card Electromechanical Specification™."

Figure 5-2 PCIe x1 Slot Schematic



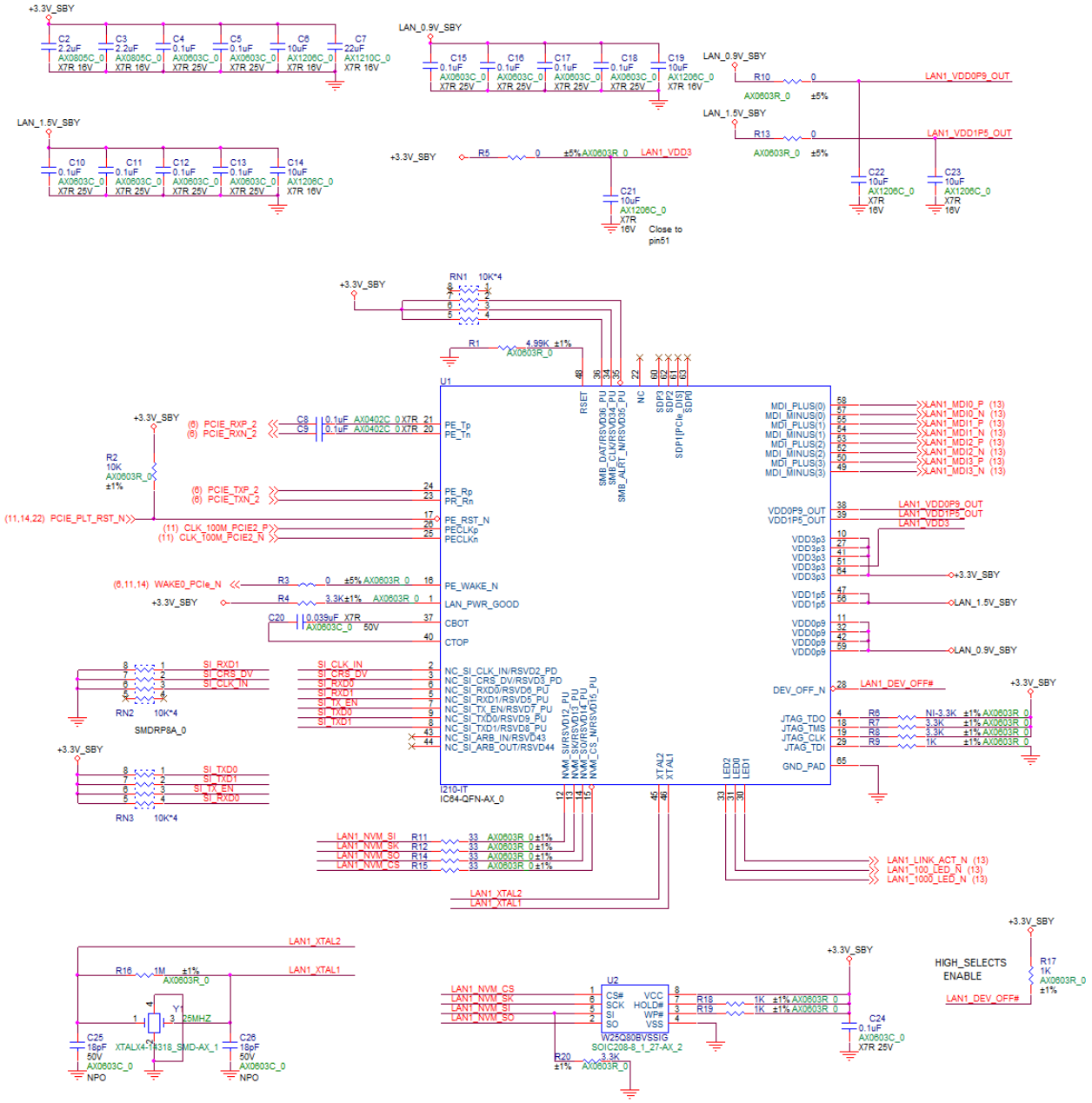
- The Pin PWRGD (A11) of PCIe x1 slot may alternatively be driven by CB_RESET# (COM Exprss Module pin B50). This is a must for COM Express modules.
- Slot signals CLK_100M_PCIE1_3+ and CLK_100M_PCIE1_3- (pins A13 and A14) are driven by the Clock Buffer, which is shown in Figure 5-1. Plug-in cards can optionally use this clock source.
- The pins HSOP0 (B14) and HSON0 (B15) of PCIe x1 slot are sourced from one pair of PCIe TX signals (TX+,TX-) on COM Express Module(ex. module pins A68 and A69). These nets drive the RX load on the slot card. These nets have coupled on the module. No coupling capacitors are needed on the Baseboard.
- Connect the pins HSIP0 (A16) and HSIN0 (A17) of PCIe x1 slot to one pair of PCIe RX signals (RX+,RX-) which are corresponding to the same PCIe TX lanes on COM Express Module(ex. module pins B68 and B69). These nets are driven by the TX source on the slot card. No coupling capacitors are needed on the Baseboard.
- Nets SMB_CK and SMB_DAT are sourced from COM Express Module pins B13 and B14 respectively.
- The SMBus supports plug-in, card-management functions and provides Manufacturer information, a model number, and a part number.
- SMBus software can save the state of the slot-car device before a suspend event, report errors, accept control parameters, and return status.
- Support for the SM Bus is optional on the slot card.
- WAKE0# is asserted by the slot card to cause COM Express Module wake-up at Module pin B66. This is an open-drain signal. It is an input to the Module and is pulled up on the Module. Other WAKE0# sources may pull this line low; it is a shared line.
- Slot JTAG pins on A5-A8 are not used.

5.2.5 PCIe x1 LAN Chip Example

PCI Express ports can used to connect the expansion devices, it can also route to a PCI Express device down on baseboard, like x1 PCIe LAN chip for Ethernet application.

The Intel® Ethernet Controller I210 (I210) is a single port, compact, low power component that supports GbE designs. The I210 supports PCI Express* [PCIe v2.1 (2.5GT/s)].

Figure 5-3 PCIe x1 LAN Chip Schematic



- The PCIe interface pins PE_Tn (20) and PE_Tp (21) should connect to RX signals on COM Express Module and should be AC coupled with capacitors (0.1 µF) near the PCIe transmitter.

- The pins PE_Rn (23) and PE_Rp (24) are sourced form TX signals on COM Express Module. These

pins don't need AC coupling capacitors on baseboard.

- Connect PECLKn (25) and PECLKp (26) to the 100 MHz PCIe system clock.
- Connect PE_RST_N (17) to PERST# on an upstream PCIe device or Pull-up PE_RST_N (17) with a 100 KΩ resistor to 3.3 V.
- Connect PE_WAKE_N (16) to WAKE_N on an upstream PCIe device.
- Pull-up DEV_OFF_N (28) with a 3.3 KΩ resistor to 3.3 V.
- Pull-up LAN_PWR_GOOD(1) to with a 3.3 KΩ resistor to the 3.3 V.
- Pull-down RSET (48), with a 4.99 KΩ + 1% resistor.
- Use a 25 MHz + 30 ppm accuracy @ 25 °C crystal to XTAL2 (45) and XTAL1 (46). Avoid components that introduce jitter. Parallel resonant crystals are required. The calibration load should be 18 pF.
- In I210 16Mbit Flash is required if iSCSI boot, FCoE boot, PXE, EFI drivers are not integrated into the BIOS and must be included with an I210 add in card. On the I210 if the iSCSI boot, FCoE boot, PXE, and EFI drivers are integrated with the BIOS then an 8 Mbit flash can be used.
  - Use 0.1 µF decoupling capacitor on the power supplies for the flash device.
  - The Flash must be powered from auxiliary power.
  - Connect NVM_SI (12) of I210 to U2 (5) of flash part. A 33 Ω series resistor is connected to NVM_SI (12) of I210. Use a 33 KΩ pull-up resistor to this pin. Connect a 3.3 KΩ pull-down resistor through a jumper to NVM_SI (12) in order to disable NVM security. This may be necessary for testing unsigned firmware.
  - Connect NVM_SO (14) of I210 to U2 (2) of flash part.
  - Connect NVM_SK (13) of I210 to U2 (6) of flash part. A 33 Ω series resistor is connected to NVM_SK (13) of I210.
  - Connect NVM_CS_N (15) of I210 to U2 (1) of flash part. A 33 Ω series resistor is connected to NVM_CS_N (15) of I210.
- For best performance, each I210 should have it's own dedicated SMBus link to the SMBus master device. If SMBus is not used, connect 10KΩ pull-up resistors to SMB_CLK (34), SMB_DATA (36), and SMB_ALRT_N (35).

- Use a 10 KΩ pull-up resistors on the NCSI_TXD0 (9), NCSI_TXD1 (8), NCSI_RXD0(6), and NCSI_TX_EN (7) interfaces.
- Use a 10 KΩ pull-down resistors on the NCSI_CLK_IN (2), NCSI_CRS_DV(3) and NCSI_RXD1(5) interfaces.
- The System Side Center tap should not be connected to a power supply.
- Connect Pins 49, 50, 52, 53, 54, 55, 57, 58 of I210 to the magnetics module.
- Connect 10, 27, 41 and 64 to an external 3.3V power supply derived from AUX power.
- For the I210-AT, I210-IT, and I211-AT Connect 51 to 3.3V.
- Connect Pins 39, 47 and 56 to each other for the 1.5 V supply.
- Connect Pins 11, 32, 42, and 59 together for the 0.9 V power supply.
- Connect Pins 39 and 38 with the zero ohm resistor to 1.5V and 0.9V respectively when dual Hartwell-Springville design is to used.
- Connect CTOP (37) and CBOT (40) to each other through a 0.039 uF capacitor.
- The LEDs use 3.3 Vdc. The default behaviours are:
  - LED0 (31) -> If linked at 100BASE-TX then low. Connect LED0 to cathode of green speed LED and the anode of the orange speed LED.
  - LED1 (30) -> If link up then low. If link down then high. Blink high for activity. Connect LED1 to the cathode of the link/activity LED. Connect the anode of the link/activity LED to Vcc with zero ohm resistor.
  - LED2 (33) -> If linked at 1000BASE-T then low. Connect LED2 to cathode of orange speed LED and the anode of the green speed LED.
- Pins JTAG_CLK(19) and JTAG_TMS(18) should be pulled high with 3.3K Ω resistor value.
- Pin JTAG_TDI(29) should be pulled down with 1K Ω resistor value.
- If pin JTAG_TDO(4) is used then 3.3 KΩ pull-up resistor is used. If pin JTAG_TDO(4) is not used then there is no requirement of pull-up or pull-down resistor.

MEMO:

3.0 update to 3.1

1. Modify Parameters of “Signal length” and “Via Usage”

Chapter 6

6. PEG

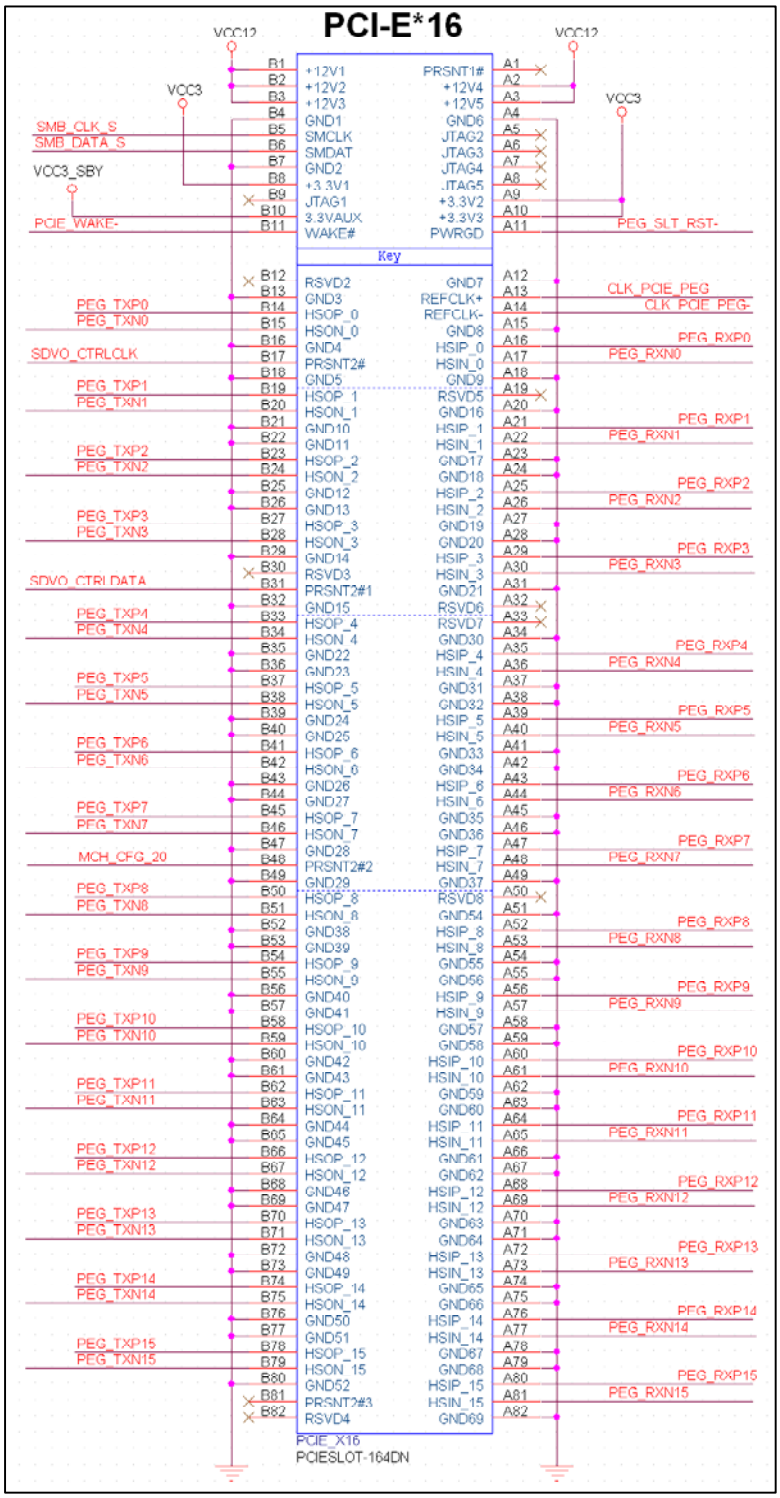
6.1 PEG and – Signal Definitions

A common set of pins on the COM Express Type 6 C-D Connector Rows is shared with PCI Express Graphics (PEG). This pin-out and pin-sharing arrangement is shown in Table 6-1 below.

Table 6-1 PEG x16 Type 6 Rows C and D Pin-outs

Pin	Row C	Row D
51		
52	PEG_RX0+	PEG_TX0+
53	PEG_RX0-	PEG_TX0-
54		PEG_LANE_RV#
55	PEG_RX1+	PEG_TX1+
56	PEG_RX1-	PEG_TX1-
57		
58	PEG_RX2+	PEG_TX2+
59	PEG_RX2-	PEG_TX2-
60		
61	PEG_RX3+	PEG_TX3+
62	PEG_RX3-	PEG_TX3-
63		
64		
65	PEG_RX4+	PEG_TX4+
66	PEG_RX4-	PEG_TX4-
67		
68	PEG_RX5+	PEG_TX5+
69	PEG_RX5-	PEG_TX5-
70		
71	PEG_RX6+	PEG_TX6+
72	PEG_RX6-	PEG_TX6-
73		
74	PEG_RX7+	PEG_TX7+
75	PEG_RX7-	PEG_TX7-
76		
77		
78	PEG_RX8+	PEG_TX8+
79	PEG_RX8-	PEG_TX8-
80		
81	PEG_RX9+	PEG_TX9+
82	PEG_RX9-	PEG_TX9-
83		
84		
85	PEG_RX10+	PEG_TX10+
86	PEG_RX10-	PEG_TX10-
87		
88	PEG_RX11+	PEG_TX11+
89	PEG_RX11-	PEG_TX11-
90		
91	PEG_RX12+	PEG_TX12+
92	PEG_RX12-	PEG_TX12-
93		
94	PEG_RX13+	PEG_TX13+
95	PEG_RX13-	PEG_TX13-
96		
97		PEG_ENABLE#
98	PEG_RX14+	PEG_TX14+
99	PEG_RX14-	PEG_TX14-
100		
101	PEG_RX15+	PEG_TX15+
102	PEG_RX15-	PEG_TX15-

Figure 6-1 PCIe X16 Slot



6.2 PEG – Routing Considerations

6.2.1 PCIe Polarity Inversion

Per the PCI Express Card Electromechanical Specification, all PCIe devices must support polarity inversion on each PCIe lane, independently of the other lanes. For example, you can route the COM Express Module PCIE_TXP0 signal to the corresponding 'N' pin on the slot or target device, and the PCIE_TXN0 signal to the corresponding 'P' pin. If this makes the layout cleaner, with fewer layer transitions and better differential pairs, then take advantage of this PCIe feature.

6.2.2 PEG Lane Reversal

The COM Express® Specification defines an input signal, PEG_LANE_RV-, on Module connector pin D54 to enable PEG lane reversal. Strapping PEG_LANE_RV- low on the Baseboard causes the COM Express Module chipset to reverse the PEG lane order (PEG lane 0 on the chipset becomes PEG lane 15; PEG lane 1 becomes PEG lane 14; etc.)

This can be extremely useful. If you find that the PEG bus is crossed, or has a "bowtie," when placing parts on the Baseboard, you can eliminate the bowtie by invoking PEG-lane reversal.

If Module pin D54 PEG_LANE_RV- is strapped low to untwist a bowtie on the PEGx16 lines to an x16 slot, then an ADD2 card used in this slot must be a reverse pin-out ADD2 card. Reverse pin-out ADD2 cards are designated ADD2-R.

However, there is caveat:

- Lane reversal may not apply if the lines are used for general purpose PCIe use, rather than x16 PEG use. Check the relevant COM Express Module User Guide.

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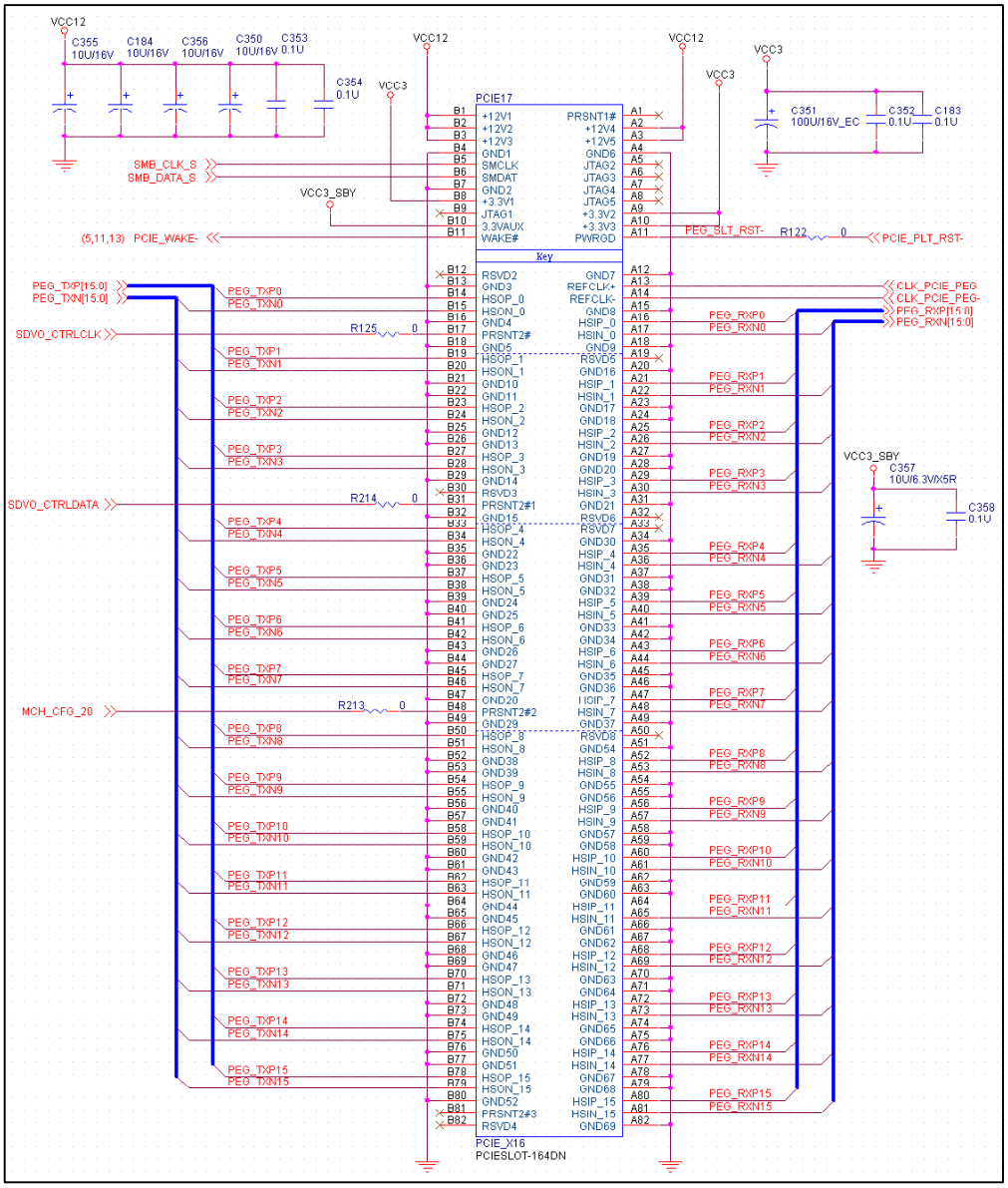
Figure 6-2 PEG X16 Schematic



MEMO:

Chapter 7

7. LAN 1

7.1 LAN 1 – Signal Definitions

The LAN 1 port defines a set of pins on the Type 6 and Type 10 A-B connector to support a 10/100 megabits per second or Gigabit Ethernet LAN (Local Area Network) implementation. All COM Express Modules must support at least 10/100/1000 megabits per second operation on LAN1. The COM Express® Specification specifies that LAN magnetics must reside on the Baseboard, not on the Module. The LAN interface consists of four differential pair signals, designated as LAN1_MDI0+,- thru LAN1_MDI3+,-. Additionally, there are four single-ended signals that provide link-status information, along with a reference voltage for the magnetics center tap.

Table 7-1 LAN 1 Pin-outs

Pin	Row A	Row B
1	GND	GND
2	GBE0_MDI3-	GBE0_ACT#
3	GBE0_MDI3+	
4	GBE0_LINK100#	
5	GBE0_LINK1000#	
6	GBE0_MDI2-	
7	GBE0_MDI2+	
8	GBE0_LINK#	
9	GBE0_MDI1-	
10	GBE0_MDI1+	
11	GND	
12	GBE0_MDI0-	
13	GBE0_MDI0+	
14	GBE0_CTREF	

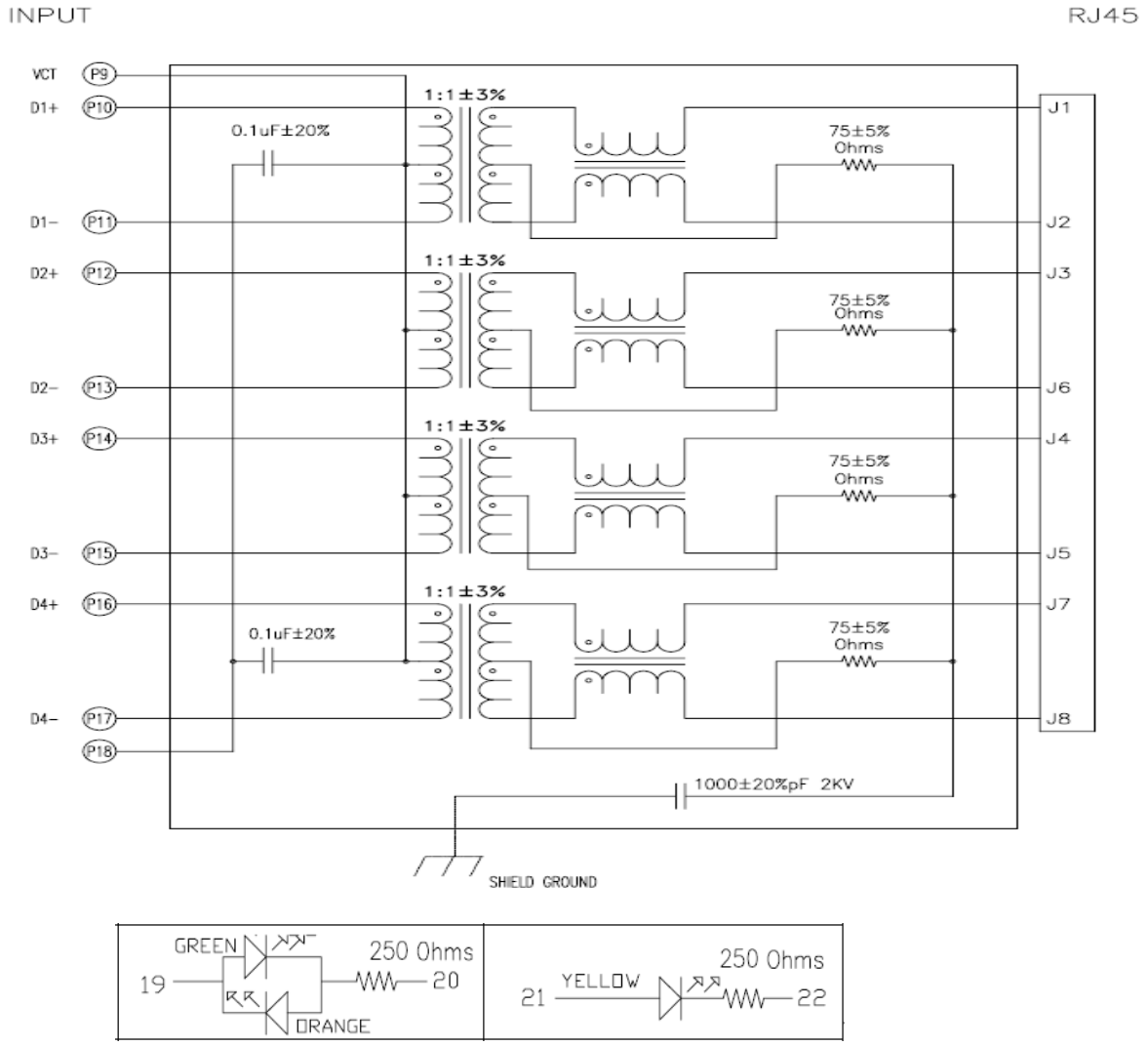
7.2 LAN 1 – Routing Considerations

The four differential pairs for LAN 1 are:

- LAN1_MDI0+ and LAN1_MDIO-
- LAN1_MDI1+ and LAN1_MDI1-
- LAN1_MDI2+ and LAN1_MDI2-
- LAN1_MDI3+ and LAN1_MDI3-
- Keep LAN connections as short as possible.
- Terminate all unused connections on the RJ45 cable and the magnetics module to chassis ground.
- For the magnetics module, separate the digital ground on the primary side and the chassis ground on the secondary side.
- The use of RJ45 jacks with integrated magnetics is strongly recommended.

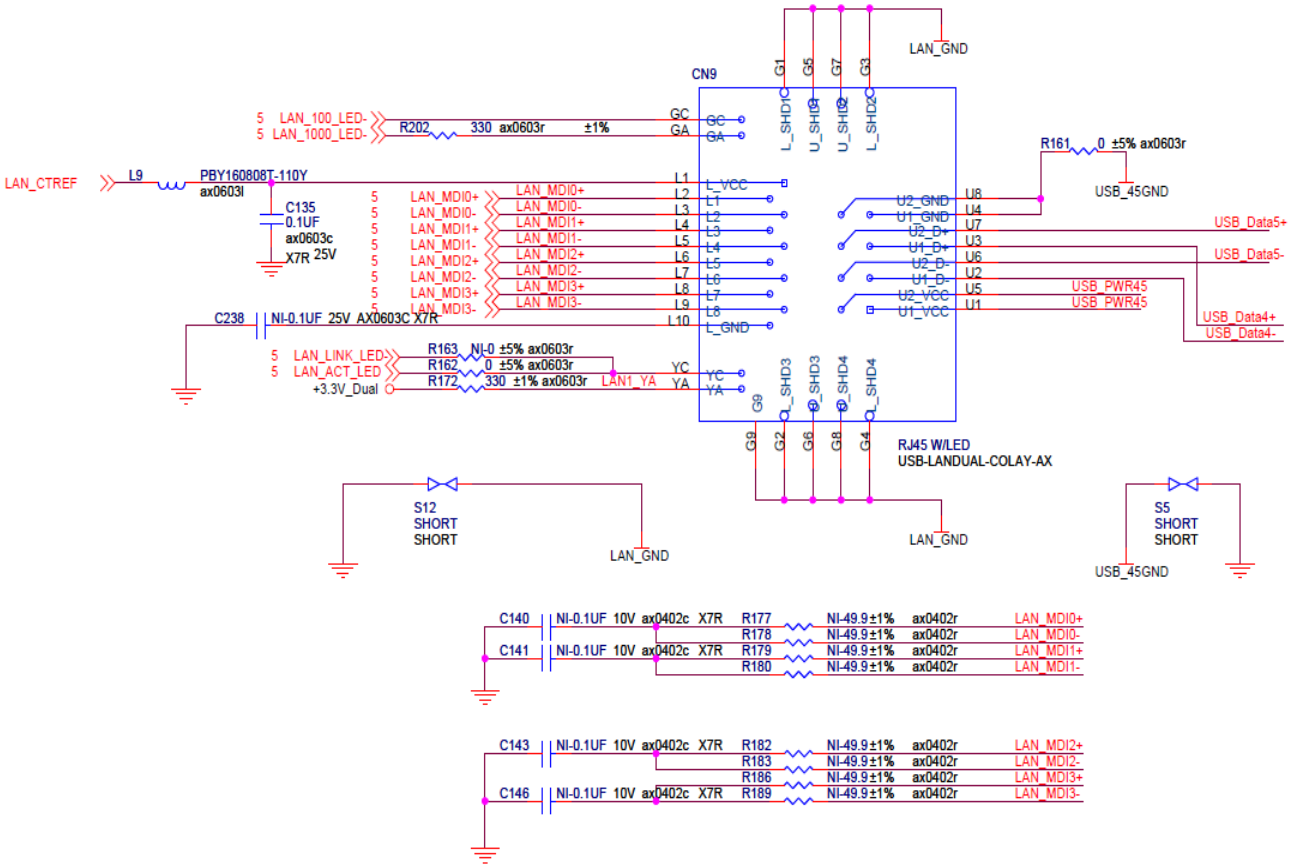
Parameter	Trace Louting
Differential Impedance	95 Ω ±15%
Single-End Impedance	50 Ω ±10%
Signal length	5.0 inches
Maximum signal length between isolation magnetics Module and RJ45 connector on the Carrier Board	1.0 inch
Spacing between differential pairs (inter-pair)	Min. 50mils
Spacing between differential pairs and high-speed periodic signals	Min. 300mils
Spacing between differential pairs and low-speed non periodic signals	Min. 100mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between differential pairs (inter-pair)	Max. 30mils
Reference plane	GND
Via Usage	2 vias per segment (Lan Device to magnetics or magnetics to RJ45)

Figure 7-1 LAN 1 Magnetics Connections



7.3 LAN 1 – Reference Schematic

Figure 7-2 Ethernet Schematic



MEMO:

3.0 update to 3.1

1. Modify Parameters of “Signal length” and “Maximum signal length between isolation magnetics Module and RJ45 connector on the Carrier Board”

Chapter 8

8. USB

8.1 USB – Signal Definitions

A COM Express Module must support a minimum of 4 USB Ports and can support up to 8 USB Ports. All of the USB Ports must be USB2.0 compliant. There are 4 over-current signals shared by the 8 USB Ports. A Baseboard must current limit the USB power source to minimize disruption of the Baseboard in the event that a short or over-current condition exists on one of the USB Ports.

A Module must fill the USB Ports starting at Port 0. The USB SuperSpeed ports 0, 1, 2 and 3, if used, are to be paired with USB 2.0 ports 0, 1, 2 and 3 in the same order. The USB SuperSpeed ports use the same over current signaling mechanism as the USB 2.0 ports, but USB 3.0 allows up to 0.9A current per port instead of 500mA allowed in USB 2.0.

A USB Port can be powered from the Baseboard Main Power or from the Baseboard Suspend Power. Main Power is used for USB devices that are accessed when the system is powered on. Suspend Power (VCC_5V_SBY) is used for devices that need to be powered when the Module is in Sleep-State S3. This would typically be for USB devices that support Wake-on-USB. The amount of current available on VCC_5V_SBY is limited so it should be used sparingly.

All eight ports appear on the COM Express A-B-C-D connector as shown in Table 8-1 below.

Table 8-1 USB Pin-outs

	Type 6		Type 10	
Pin	**Row A**	**Row B**	**Row A**	**Row B**
22			USB_SSRX0-	USB_SSTX0-
23			USB_SSRX0+	USB_SSTX0+
24				
25			USB_SSRX1-	USB_SSTX1-
26			USB_SSRX1+	USB_SSTX1+
36	USB6-	USB7-	USB6-	USB7-
37	USB6+	USB7+	USB6+	USB7+
38	USB_6_7_OC#	USB_4_5_OC#	USB_6_7_OC#	USB_4_5_OC#
39	USB4-	USB5-	USB4-	USB5-
40	USB4+	USB5+	USB4+	USB5+
41	GND	GND	GND	GND
42	USB2-	USB3-	USB2-	USB3-
43	USB2+	USB3+	USB2+	USB3+
44	USB_2_3_OC#	USB_0_1_OC#	USB_2_3_OC#	USB_0_1_OC#
45	USB0-	USB1-	USB0-	USB1-
46	USB0+	USB1+	USB0+	USB1+

	Type 6	
Pin	**Row C**	**Row D**
3	USB_SSRX0-	USB_SSTX0-
4	USB_SSRX0+	USB_SSTX0+
5	GND	GND
6	USB_SSRX1-	USB_SSTX1-
7	USB_SSRX1+	USB_SSTX1+
8	GND	GND
9	USB_SSRX2-	USB_SSTX2-
10	USB_SSRX2+	USB_SSTX2+
11	GND	GND
12	USB_SSRX3-	USB_SSTX3-
13	USB_SSRX3+	USB_SSTX3+

8.2 USB Ports – Routing Considerations

USB pairs should not cross plane split. Keep layer transitions to a minimum.

Table 8-2 USB2.0 Layout Guidelines

Parameter	Trace Louting
Differential Impedance	90 Ω ±15%
Single-End Impedance	45 Ω ±10%
Signal length	14.0 inches
Spacing between pairs-to-pairs (inter-pair)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	150mils
Reference plane	GND
Via Usage	Max. 3
USB_PWR	1 Port for 0.5A

Table 8-3 USB3.0 Layout Guidelines

Parameter	Trace Louting
Differential Impedance	85 Ω ±15%
Single-End Impedance	50 Ω ±10%
Signal length	4.5 inches
Spacing between pairs-to-pairs (inter-pair)	Min. 15mils
Spacing between differential pairs and high-speed periodic signals	Min. 15mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Reference plane	GND
Via Usage	Max. 3
USB_PWR	1 Port for 0.9A

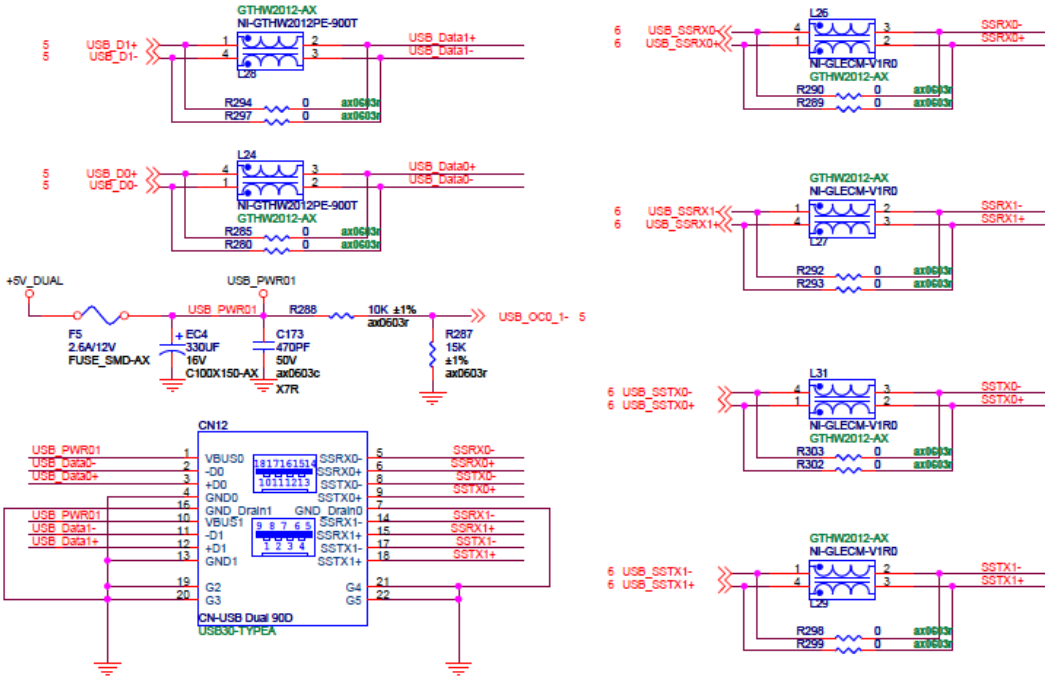
USB_OC# signal routes should be spacing other signal more than **2X** trace width is better.

8.3 USB Ports – Reference Schematic

The following notes apply to Figure 8-1.

- USB_OC_ 0_1-, USB_OC_2_3-, USB_OC_4_5- and USB_OC_6_7- are over-current signals that are inputs to COM Express Module pins B44, A44, B38 and A38 for USB_0_1, USB_2_3, USB_4_5 and USB_6_7 respectively.
- Each signal is driven low by the chip upon detection of overload, short-circuit or thermal trip, which causes the affected switch to turn off. The adjacent switch is not affected.
- Do not pull the OC signals high to 3.3V on the COM Express Baseboard; this is done on the COM Express Module.
- The signal is asserted until the over-current or over-temperature condition is resolved.
- USB0+/- thru USB7+/- from the COM Express Module are routed thru a common mode choke to reduce radiated cable emissions. The common-mode choke should be placed close to the external connector.

Figure 8-1 USB Ports Schematic



MEMO:

3.0 update to 3.1

1. Modify Parameters of “Single-End Impedance” and “Length matching between differential pairs (intra-pair)” for Table 8-2
2. Modify Parameters of “Spacing between pairs-to-pairs (inter-pair) ” and “Spacing between differential pairs and high-speed periodic signals“ for Table 8-3

Chapter 9

9. SATA

9.1 SATA – Signal Definitions

Support for up to four (Type 6) or two (Type 10) SATA ports is defined on the COM Express A-B connector. Support for a minimum of one port is required for all Module Types. The COM Express® Specification allows for both SATA-150 (150 megabits per second; 1st generation of SATA),SATA-300 (300 megabits per second; 2nd generation) implementations. Constraints for SATA-300 implementations are more severe than those for SATA-150. The COM Express® Specification addresses both in the section on insertion losses.

Table 9-1 SATA Pin-outs

	Type 6		Type 10	
Pin	**Row A**	**Row B**	**Row A**	**Row B**
16	SATA0_TX+	SATA1_TX+	SATA0_TX+	SATA1_TX+
17	SATA0_TX-	SATA1_TX-	SATA0_TX-	SATA1_TX-
18				
19	SATA0_RX+	SATA1_RX+	SATA0_RX+	SATA1_RX+
20	SATA0_RX-	SATA1_RX-	SATA0_RX-	SATA1_RX-
21				
22	SATA2_TX+	SATA3_TX+		
23	SATA2_TX-	SATA3_TX-		
24				
25	SATA2_RX+	SATA3_RX+		
26	SATA2_RX-	SATA3_RX-		

9.2 SATA – Routing Considerations

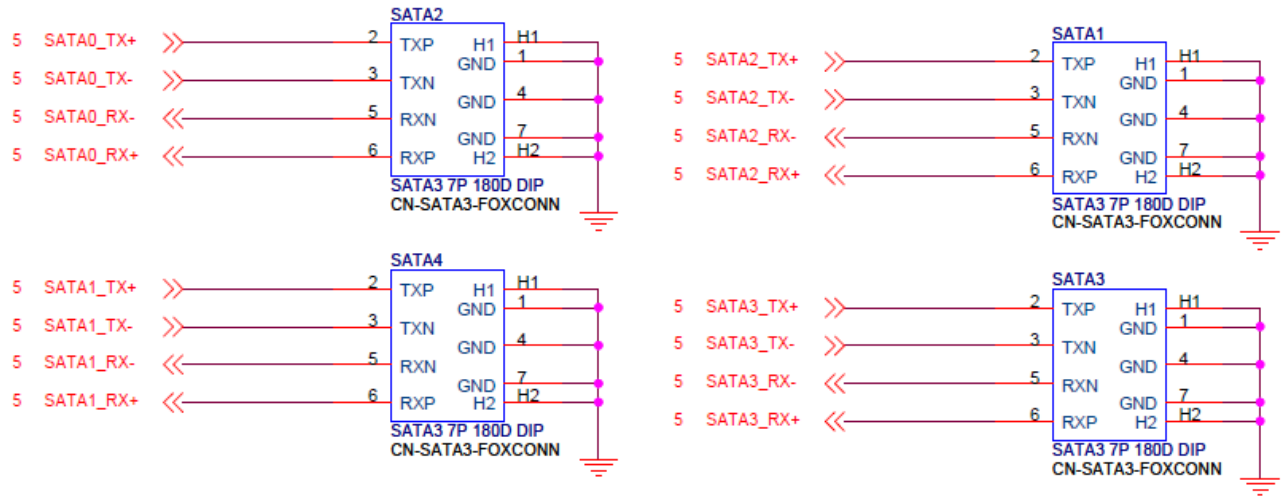
Route SATA signals as differential pairs, and do not cross plane splits. Keep layer transitions to a minimum.

Table 9-2 SATA Layout Guidelines

Parameter	Trace Louting
Differential Impedance	85 Ω ±15%
Single-End Impedance	50 Ω ±10%
Signal length	3.0 inches
Spacing between RX and TX pairs (inter-pair)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Reference plane	GND
Via Usage	A maximum of 2 vias is recommended

9.3 SATA – Reference Schematic

Figure 9-1 SATA Ports Schematic



The following notes apply to Figure 9-1 above.

- This type carries SATA data pairs and the GND reference only. Power for the SATA drive is not included on this connector type. Power for the SATA drive is delivered thru a separate connector from the system ATX power supply.
- Alternate 22-pin connector types are available that deliver power and data to the SATA drive. This may be over a combined power/data cable or in a direct configuration in which the SATA drive mates directly to the 22-pin plug on the Baseboard. Please refer to the SATA specification for pin-out information.
- Nets SATA0_TX+/- thru SATA3_TX +/- are sourced from the COM Express Module SATA TX pins.
- Nets SATA0_RX+/- thru SATA3_RX +/- are sourced from SATA disks and are routed to the COM Express Module SATA RX pins.
- Coupling capacitors are not needed on Baseboard SATA lines. They are present on the COM Express Module.

MEMO:

Chapter 10

10. LVDS

10.1 LVDS – Signal Definitions

The COM Express® Specification provides an optional LVDS interface on the COM Express A-B connector. Type 6 Module defines two LVDS channels and is designated as LVDS_A and LVDS_B. Type 10 Module only defines one LVDS channel that is designated as LVDS_A.

Systems use a single-channel LVDS for most displays. Dual LVDS channels are used for very high-bandwidth displays. Single-channel LVDS means that one complete RGB pixel is transmitted per display input clock (also known as the shift clock - see Table 10-2 below for a summary of LVDS terms). Dual channel LVDS means that two complete RGB pixels are transmitted per display input clock. The two pixels are adjacent along a display line. Dual-channel LVDS does not mean that two LVDS displays can be driven.

Each COM Express LVDS channel consists of four differential data pairs and a differential clock pair for a total of five differential pairs per channel. COM Express Modules and Module chipsets may not use all pairs. For example, with 18-bit TFT displays, only three of the four data pairs on the LVDS_A channel are used, along with the LVDS_A clock. The LVDS_B lines are not used. The manner in which RGB data is packed onto the LVDS pairs (including packing order and color depth) is not specified by the COM Express® Specification. This may be Module-dependent. Further mapping details are given in Section 10.3 below.

There are five single-ended signals included to support the LVDS interface: two lines are used for an I2C interface that may be used to support EDID or other panel information and identification schemes.

Additionally, there are an LVDS power enable (LVDS_VDD_EN) and backlight control and enable lines (LVDS_BKLT_CTRL and LVDS_BKLT_EN).

Table 10-1 LVDS A and B Pin-outs

	Type 6		Type 10	
Pin	**Row A**	**Row B**	**Row A**	**Row B**
71	LVDS_A0+	LVDS_B0+	LVDS_A0+	
72	LVDS_A0-	LVDS_B0-	LVDS_A0-	
73	LVDS_A1+	LVDS_B1+	LVDS_A1+	
74	LVDS_A1-	LVDS_B1-	LVDS_A1-	
75	LVDS_A2+	LVDS_B2+	LVDS_A2+	
76	LVDS_A2-	LVDS_B2-	LVDS_A2-	
77	LVDS_VDD_EN	LVDS_B3+	LVDS_VDD_EN	
78	LVDS_A3+	LVDS_B3-	LVDS_A3+	
79	LVDS_A3-	LVDS_BKLT_EN	LVDS_A3-	LVDS_BKLT_EN
80	GND	GND	GND	GND
81	LVDS_A_CK+	LVDS_B_CK+	LVDS_A_CK+	
82	LVDS_A_CK-	LVDS_B_CK-	LVDS_A_CK-	
83	LVDS_I2C_CK	LVDS_BKLT_CTRL	LVDS_I2C_CK	LVDS_BKLT_CTRL
84	LVDS_I2C_DAT		LVDS_I2C_DAT	

10.2 LVDS – Routing Considerations

Route LVDS signals as differential pairs (excluding the five single-ended support signals), LVDS pairs should not cross plane splits. Keep layer transitions to a minimum.

All LVDS pairs should have the same environment, including the same reference plane and the same number of vias.

Table 10-2 LVDS Layout Guidelines

Parameter	Trace Louting
Differential Impedance	100 Ω ±15%
Single-End Impedance	55 Ω ±10%
Signal length	6.75 inches
Spacing between pairs-to-pairs (inter-pair)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 20mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 20mils
Length matching between clock and data pairs (inter-pair)	Max. 20mils
Length matching between data pairs (inter-pair)	Max. 20mils
Reference plane	GND
Via Usage	Max. of 2 vias per line

10.3 LVDS – Color Mapping and Terms

10.3.1 FPD-Link and Open LDI Color Mapping

An LVDS stream consists of frames that pack seven data bits per LVDS frame. Details can be found in the tables below. The LVDS clock is one seventh of the source-data clock. The order in which panel data bits are packed into the LVDS stream is referred to as the LVDS color-mapping. There are two LVDS color-mappings in common use: FPD-Link and Open LDI. FPD-Link is the older standard but is being eclipsed by Open LDI.

The FPD-Link and Open LDI standards are the same for panels with color depths of 18 bits (6 Red, 6 Green, 6 Blue) or less. The 18 bits of color data and 3 bits of control data, or 21 bits total, are packed into 3 LVDS data streams. The LVDS clock is carried on a separate channel for a total of 4 LVDS pairs – 3 data pairs and a clock pair.

For 24-bit color depths, a 4th LVDS data pair is required (for a total of 5 LVDS pairs – 4 data and 1 clock). FPD-Link and Open LDI differ in this case. FPD-Link keeps the least significant color bits on the original 3 LVDS data pairs and adds the most significant color bits (the dominant or “most important” bits) to the 4th channel. Six bits are added: 2 Red, 2 Green, and 2 Blue (the seventh available bit slot in the 4th LVDS stream is not used).

A 24-bit, Open LDI implementation shifts the color bits on the original 3 LVDS data pairs up by two, such that the most significant color bits for both 18- and 24-bit panels occupy the same LVDS slots. For example, the most significant Red color bit is R5 for 18-bit panels and R7 for 24-bit panels. The 18-bit R5 and the 24-bit R7 occupy the same LVDS bit slot in Open LDI. The 4th LVDS data stream in Open LDI carries the least significant bits of a 24-bit panel – R0, R1, G0, G1, B0, and B1.

The advantage of Open LDI is that it provides an easier upgrade and downgrade path than FPD-Link does. An 18-bit panel can be used with an Open LDI 24-bit data stream by simply connecting the 1st three LVDS data pairs to the panel, and leaving the 4th LVDS data pair unused. This does not work with FPD-Link because the mapping for the 24-bit case is not compatible with the 18-bit case – the most significant data bits are on the 4th LVDS data stream.

If you design LVDS de-sterilizers, work around the Module color-mapping by picking off the de-serialized outputs in the order needed. If you use a flat panel with an integrated LVDS receiver, it is important that the display’s color-mapping matches the Module’s color-mapping.

10.4 Notes on Industry Terms

Some terms in this document that describe LVDS displays may vary from other documents (such as display data sheets from vendors, IC data sheets for graphics controllers and LVDS transmitters and receivers, the Open LDI specification, and COM Express Module documentation).

Examples of terms that may vary include:

- For dual-channel displays, terms are needed to describe the adjacent pixels.

Various documents will reference for the same pair of pixels:

- Odd and Even pixels (column count starts at 1)
- Even and Odd pixels (column count starts at 0)
- R10 and R20 for adjacent least significant Red bits
- R00 and R10 for adjacent least significant Red bits
- Terms used to describe the clocks vary:
- The Open LDI specification uses the term “pixel clock” differently from most other documents. In the Open LDI specification, the “pixel clock” period is seven pixel periods long. Most other documents refer to this concept as the “LVDS clock.”
- Transmit Bit Order
- In this document, the seven bits in an LVDS frame are numbered 1 – 7, with Bit 1 being placed into the stream before Bit 2.

Display terms used in this document are defined in Table 10-3 below.

Table 10-3 LVDS Display Terms and Definitions

Term	Definition
Color-Mapping	Color-mapping refers to the order in which display color bits and control bits are placed into the serial LVDS stream. Each LVDS data frame can accept seven bits. The way in which the bits are serialized into the stream is arbitrary, as long as they are de-serialized in a corresponding way. Two main color-mapping schemes are FPD-Link and Open LDI. They are the same for 18-bit panels but differ for 24-bit panels.
DE	Display Enable – a control signal that asserts during an active display line.
Dual Channel	In a dual-channel bit stream, two complete RGB pixels are transmitted with each shift clock. The shift clock is one half the pixel frequency in this case. Dual channel LVDS streams are either 8 differential pairs (6 data pairs, 2 clock pairs, for dual 18 bit streams) or 10 differential pairs (8 data pairs, 2 clock pairs, for dual 24-bit streams).
Even Pixel	A pixel from an even column number, counting from 1. For example, on an 800x600 display, the even pixels along a row are in columns 2,4 ... 800. The odd pixels are in columns 1,3,5 ... 799.
FPD-Link	Flat Panel Display Link – an LVDS color-mapping scheme popularized by National Semiconductor. FPD Link color-mapping is the same as open LDI color-mapping for 18-bit displays but is different for 24-bit displays. FPD color-mapping puts the most significant bits of a 24-bit display onto the 4th LVDS channel.
HSYNC	Horizontal Sync – a control signal that occurs once per horizontal display line.
LCLK	LVDS clock – the low voltage differential clock that accompanies the serialized LVDS data stream. For a single-channel LVDS stream, the LVDS clock is 1/7th the pixel clock, which means there is one LVDS clock period for every 7 pixel clock periods. For a dual-channel LVDS data stream, the LVDS clock is 1/14th the pixel clock, which means there is one LVDS clock period for every 14-pixel clock periods.
Odd Pixel	A pixel from an odd column number, counting from 1. For example, on an 800x600 display, the odd pixels along a row are in columns 1,3,5, ... 799. The even pixels are in columns 2,4 ...800.
Open LDI	Open LVDS Display Interface – a formalization by National Semiconductor of de facto LVDS standards. See Appendix G for a reference to the standard. Open LDI color-mapping is the same as FPD-Link color-mapping for 18-bit displays, but is different for 24-bit displays. Open LDI color-mapping puts the least significant bits of a 24-bit display onto the 4th LVDS channel. Doing so means that an 18-bit display can operate on a 24-bit Open LDI link by using the first 3 LVDS data channels.
PCLK	Pixel clock – the clock associated with a single display pixel. For example, on a 640x480 display, there are 640 pixel clocks during the active display line period (and additional pixel clocks during the blanking periods). For a single-channel TFT display, the pixel clock is the same as the shift clock. For a dual-channel TFT display, the pixel clock is twice the frequency of the shift clock.
SCLK	Shift clock – the clock that shifts either a single pixel or a group of pixels into the display, depending on the display type. For a single-channel TFT display, the shift clock is the same as the pixel clock. For a dual-channel TFT display, the shift clock period is twice the pixel clock. For some display types, such as passive STN displays, the shift clock may be four- or eight-pixel clocks.
Single Channel	In a single-channel bit stream, a single RGB pixel is transmitted with each shift clock. The shift clock and the pixel clock are the same in this case. Single-channel LVDS streams are either 4 differential pairs (3 data pairs, 1 clock pair, for a single 18 bit stream) or 5 differential pairs (4 data pairs, 1 clock pair, for a single 24-bit stream).
Transmit Bit Order	The order, in time, in which bits are placed into the seven bit slots per LVDS frame. Bit 1 is earlier in time than bit 2, etc.
Unbalanced	Unbalanced means that the LVDS serializing hardware does not insert or manipulate bits to achieve a DC balance – i.e. an equal number of 0 and 1 bits, when averaged over multiple frames.
VSYNC	Vertical Sync – a control signal that occurs once per display frame.
Xmit Bit Order	See Transmit Bit Order.

10.4.1 LVDS Display Color Mapping Tables

LVDS display color-mappings for single- and dual-channel displays are shown in Tables 10-4 and 10-5 below.

For single-channel displays, COM Express Module LVDS B pairs are not used and may be left open. For single-channel, 18-bit displays, the LVDS_A3± channel is not used and may be left open.

For 18-bit, single-channel and 36-bit, dual-channel displays, the FPD-Link and Open LDI color-mappings are the same. For 24-bit, single-channel and 48-bit, dual-channel displays, mappings differ and care must be taken that the Module and display LVDS color-mappings agree.

Table 10-4 LVDS Display: Single Channel, Unbalanced Color-Mapping

	Xmit Bit Order	LVDS Clock	Open LDI 18 bit Single Ch	Open LDI 24 bit Single Ch	FPD Link 18 bit Single Ch	FPD Link 24 bit Single Ch
LVDS_A0±	1	1	G0	G2	G0	G0
	2	1	R5	R7	R5	R5
	3	0	R4	R6	R4	R4
	4	0	R3	R5	R3	R3
	5	0	R2	R4	R2	R2
	6	1	R1	R3	R1	R1
	7	1	R0	R2	R0	R0
LVDS_A1±	1	1	B1	B3	B1	B1
	2	1	B0	B2	B0	B0
	3	0	G5	G7	G5	G5
	4	0	G4	G6	G4	G4
	5	0	G3	G5	G3	G3
	6	1	G2	G4	G2	G2
	7	1	G1	G3	G1	G1
LVDS_A2±	1	1	DE	DE	DE	DE
	2	1	VSYNC	VSYNC	VSYNC	VSYNC
	3	0	HSYNC	HSYNC	HSYNC	HSYNC
	4	0	B5	B7	B5	B5
	5	0	B4	B6	B4	B4
	6	1	B3	B5	B3	B3
	7	1	B2	B4	B2	B2
LVDS_A3±	1	1				
	2	1		B1		B7
	3	0		B0		B6
	4	0		G1		G7
	5	0		G0		G6
	6	1		R1		R7
	7	1		R0		R6
LVDS_A_CK±			LCLK = PCLK / 7 SCLK = PCLK	LCLK= PCLK / 7 SCLK = PCLK	LCLK = PCLK / 7 SCLK = PCLK	LCLK = PCLK / 7 SCLK = PCLK

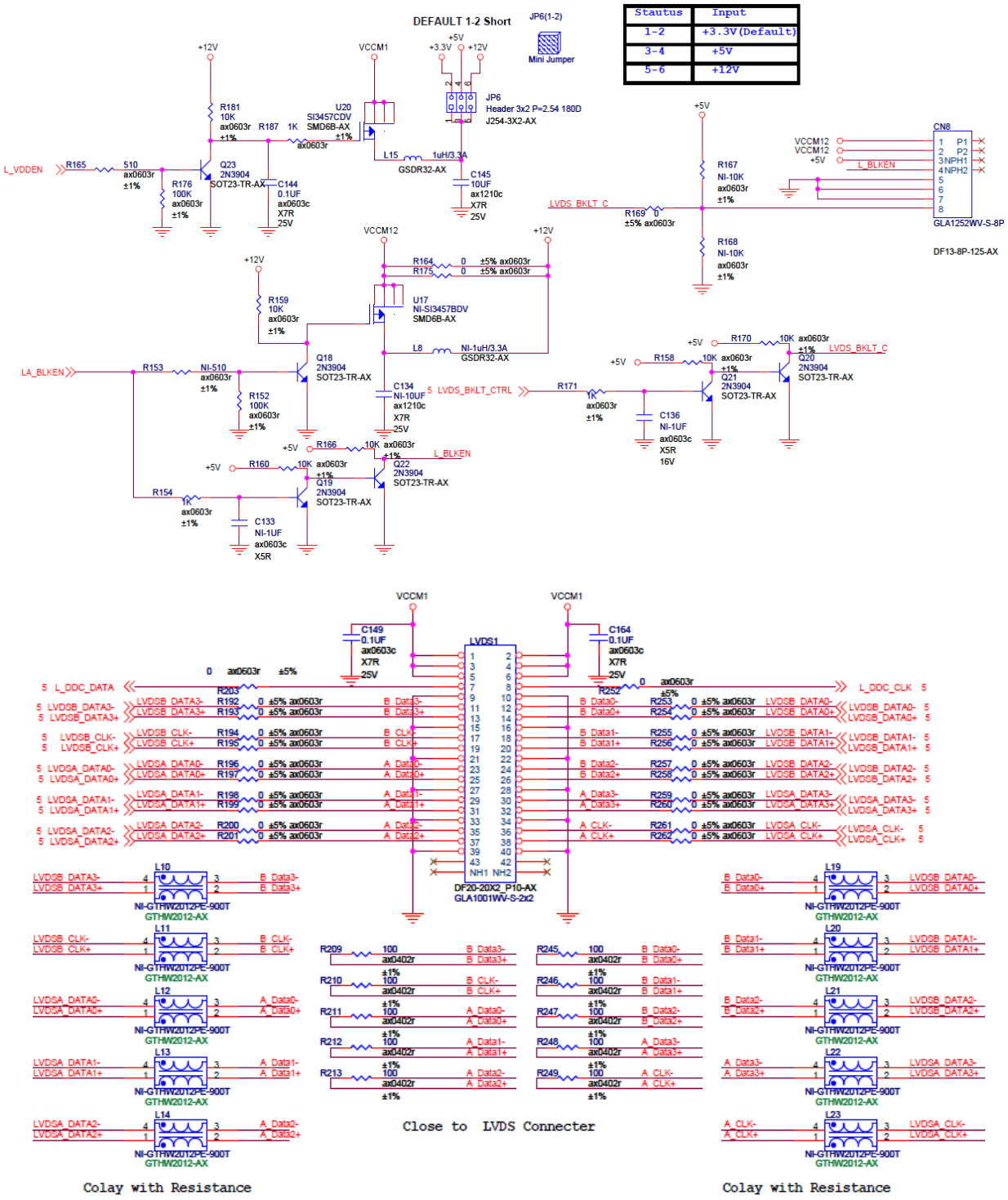
Table 10-5 LVDS Display: Dual Channel, Unbalanced Color-Mapping

	Xmit Bit Order	LVDS Clock	Open LDI 18 bit (36 bit) Dual Ch	Open LDI 24 bit (48 bit) Dual Ch	FPD Link 18 bit (36 bit) Dual Ch	FPD Link 24 bit (48 bit) Dual Ch
LVDS_A0±	1	1	Odd Pixel G0	Odd Pixel G2	Odd Pixel G0	Odd Pixel G0
	2	1	Odd Pixel R5	Odd Pixel R7	Odd Pixel R5	Odd Pixel R5
	3	0	Odd Pixel R4	Odd Pixel R6	Odd Pixel R4	Odd Pixel R4
	4	0	Odd Pixel R3	Odd Pixel R5	Odd Pixel R3	Odd Pixel R3
	5	0	Odd Pixel R2	Odd Pixel R4	Odd Pixel R2	Odd Pixel R2
	6	1	Odd Pixel R1	Odd Pixel R3	Odd Pixel R1	Odd Pixel R1
	7	1	Odd Pixel R0	Odd Pixel R2	Odd Pixel R0	Odd Pixel R0
LVDS_A1±	1	1	Odd Pixel B1	Odd Pixel B3	Odd Pixel B1	Odd Pixel B1
	2	1	Odd Pixel B0	Odd Pixel B2	Odd Pixel B0	Odd Pixel B0
	3	0	Odd Pixel G5	Odd Pixel G7	Odd Pixel G5	Odd Pixel G5
	4	0	Odd Pixel G4	Odd Pixel G6	Odd Pixel G4	Odd Pixel G4
	5	0	Odd Pixel G3	Odd Pixel G5	Odd Pixel G3	Odd Pixel G3
	6	1	Odd Pixel G2	Odd Pixel G4	Odd Pixel G2	Odd Pixel G2
	7	1	Odd Pixel G1	Odd Pixel G3	Odd Pixel G1	Odd Pixel G1
LVDS_A2±	1	1	DE	DE	DE	DE
	2	1	VSYNC	VSYNC	VSYNC	VSYNC
	3	0	HSYNC	HSYNC	HSYNC	HSYNC
	4	0	Odd Pixel B5	Odd Pixel B7	Odd Pixel B5	Odd Pixel B5
	5	0	Odd Pixel B4	Odd Pixel B6	Odd Pixel B4	Odd Pixel B4
	6	1	Odd Pixel B3	Odd Pixel B5	Odd Pixel B3	Odd Pixel B3
	7	1	Odd Pixel B2	Odd Pixel B4	Odd Pixel B2	Odd Pixel B2
LVDS_A3±	1	1				
	2	1		Odd Pixel B1		Odd Pixel B7
	3	0		Odd Pixel B0		Odd Pixel B6
	4	0		Odd Pixel G1		Odd Pixel G7
	5	0		Odd Pixel G0		Odd Pixel G6
	6	1		Odd Pixel R1		Odd Pixel R7
	7	1		Odd Pixel R0		Odd Pixel R6
LVDS_A_CK±			LCLK= PCLK / 14 SCLK = PCLK / 2	LCLK = PCLK / 14 SCLK = PCLK / 2	LCLK= PCLK / 14 SCLK = PCLK / 2	LCLK = PCLK / 14 SCLK = PCLK / 2
LVDS_B0±	1	1	Even Pixel G0	Even Pixel G2	Even Pixel G0	Even Pixel G0
	2	1	Even Pixel R5	Even Pixel R7	Even Pixel R5	Even Pixel R5
	3	0	Even Pixel R4	Even Pixel R6	Even Pixel R4	Even Pixel R4
	4	0	Even Pixel R3	Even Pixel R5	Even Pixel R3	Even Pixel R3
	5	0	Even Pixel R2	Even Pixel R4	Even Pixel R2	Even Pixel R2
	6	1	Even Pixel R1	Even Pixel R3	Even Pixel R1	Even Pixel R1
	7	1	Even Pixel R0	Even Pixel R2	Even Pixel R0	Even Pixel R0
LVDS_B1±	1	1	Even Pixel B1	Even Pixel B3	Even Pixel B1	Even Pixel B1
	2	1	Even Pixel B0	Even Pixel B2	Even Pixel B0	Even Pixel B0
	3	0	Even Pixel G5	Even Pixel G7	Even Pixel G5	Even Pixel G5
	4	0	Even Pixel G4	Even Pixel G6	Even Pixel G4	Even Pixel G4
	5	0	Even Pixel G3	Even Pixel G5	Even Pixel G3	Even Pixel G3
	6	1	Even Pixel G2	Even Pixel G4	Even Pixel G2	Even Pixel G2
	7	1	Even Pixel G1	Even Pixel G3	Even Pixel G1	Even Pixel G1
LVDS_B2±	1	1				
	2	1				
	3	0				
	4	0	Even Pixel B5	Even Pixel B7	Even Pixel B5	Even Pixel B5
	5	0	Even Pixel B4	Even Pixel B6	Even Pixel B4	Even Pixel B4
	6	1	Even Pixel B3	Even Pixel B5	Even Pixel B3	Even Pixel B3
	7	1	Even Pixel B2	Even Pixel B4	Even Pixel B2	Even Pixel B2
LVDS_B3±	1	1				
	2	1		Even Pixel B1		Even Pixel B7
	3	0		Even Pixel B0		Even Pixel B6
	4	0		Even Pixel G1		Even Pixel G7

	Xmit Bit Order	LVDS Clock	Open LDI 18 bit (36 bit) Dual Ch	Open LDI 24 bit (48 bit) Dual Ch	FPD Link 18 bit (36 bit) Dual Ch	FPD Link 24 bit (48 bit) Dual Ch
	5	0		Even Pixel G0		Even Pixel G6
	6	1		Even Pixel R1		Even Pixel R7
	7	1		Even Pixel R0		Even Pixel R6
LVDS_B_CK±			LCLK= PCLK / 14 SCLK = PCLK / 2	LCLK = PCLK / 14 SCLK = PCLK / 2	LCLK= PCLK / 14 SCLK = PCLK / 2	LCLK = PCLK / 14 SCLK = PCLK / 2

10.5 LVDS – Reference Schematic

Figure 10-1 LVDS LCD Function Module Schematic



MEMO:

3.0 update to 3.1

1. Modify Parameters of “Single-End Impedance”

Chapter 11

11. VGA

11.1 VGA – Signal Definitions

Pins for an analog VGA interface are defined in the COM Express® Specification for all Module Types. Implementation of the VGA interface is optional. The VGA interface consists of three analog color signals (Red, Green, and Blue); digital Horizontal and Vertical Sync signals, and I2C for DDC (Display Data Control) implementation.

Note: The Type 10 module doesn't define VGA signals.

Table 11-1 VGA Pin-outs

Pin	Row A	Row B
89		VGA_RED
90		GND(FIXED)
91		VGA_GRN
92		VGA_BLU
93		VGA_HSYNC
94		VGA_VSYNC
95		VGA_I2C_CK
96		VGA_I2C_DAT

11.2 VGA– Routing Considerations

Route the three analog VGA signals (VGA_RED, VGA_GRN, and VGA_BLU) and the two sync signals (VGA_HSYNC and VGA_VSYNC) as single-ended signals with a trace impedance of 75Ω.

The three analog color signals should be back-terminated on the Baseboard to ground thru 150 ohms. The signals should be given generous spacing to each other and to other signal groups. Shorter routes are preferred, although longer routes can work if carefully done. Reference the signals to a continuous, low-noise ground plane. These signals are also terminated on the Module through 150 ohms to ground, resulting in a combined Module / Baseboard side termination of 75 ohms. The VGA monitor will also have a 75 ohm termination. The Module electronics are designed to drive the net VGA termination of 37.5 ohms.

A schematic example is given in Section 11.3 below. Place the shown termination resistors, ESD- and EMI-suppression components, close to the external DB15 connector.

11.3 VGA – Reference Schematics

A schematic example of a VGA connector implementation is shown in Figure 11-2 below.

All signals along the left edge of Figure 11-2 are sourced directly from the COM Express® Module. No additional pull-ups or terminations beyond what is shown in the figure are required.

Analog signals VGA_RED, VGA_GRN, VGA_BLU are back-terminated through 150Ω resistors to ground.

Analog signals VGA_RED, VGA _GRN, VGA_BLU are connected to the DB15 VGA connector thru ferrite beads to suppress radiated noise.

- The VGA_HSYNC and VGA_VSYNC signals also are connected to the DB15 connector thru ferrite beads to suppress radiated noise.
- VGA_(R,G,B) signals route should be spacing other signal more than **4x** trace width is better.
- VGA_(HSY,VSY) signals route should be spacing other signal more than **2X** trace width is better.

Table 11-2 VGA Layout Guidelines

Data Pair	Signal Matching
VGA_RED、VGA_GREEN、VGA_BLUE	±100 mils

Figure 11-1 Analog VGA Connector Schematic

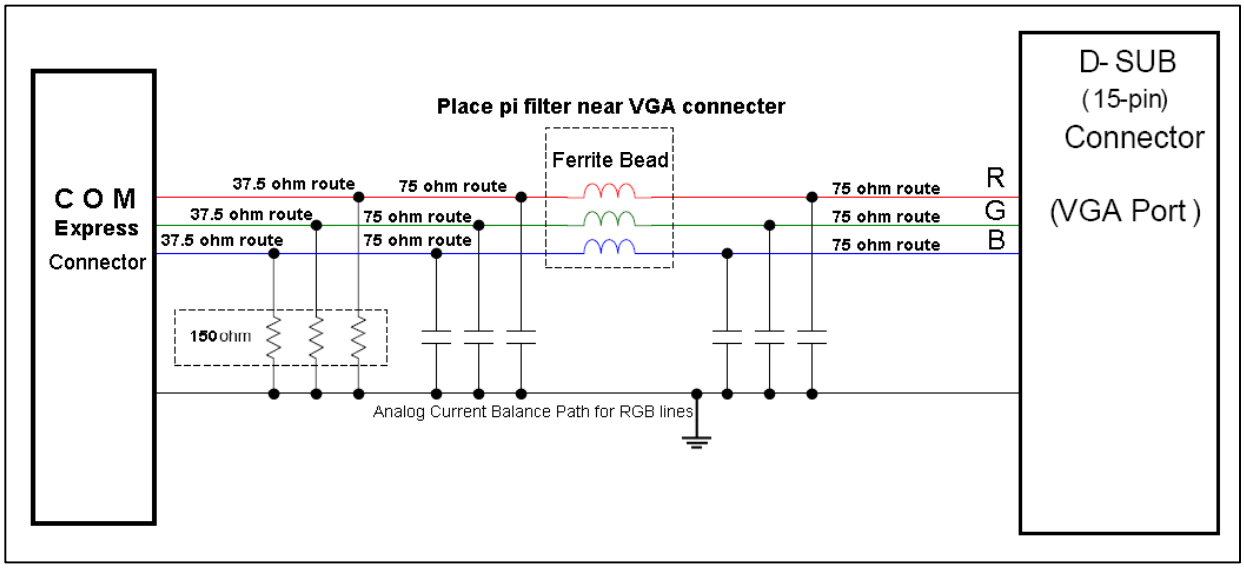
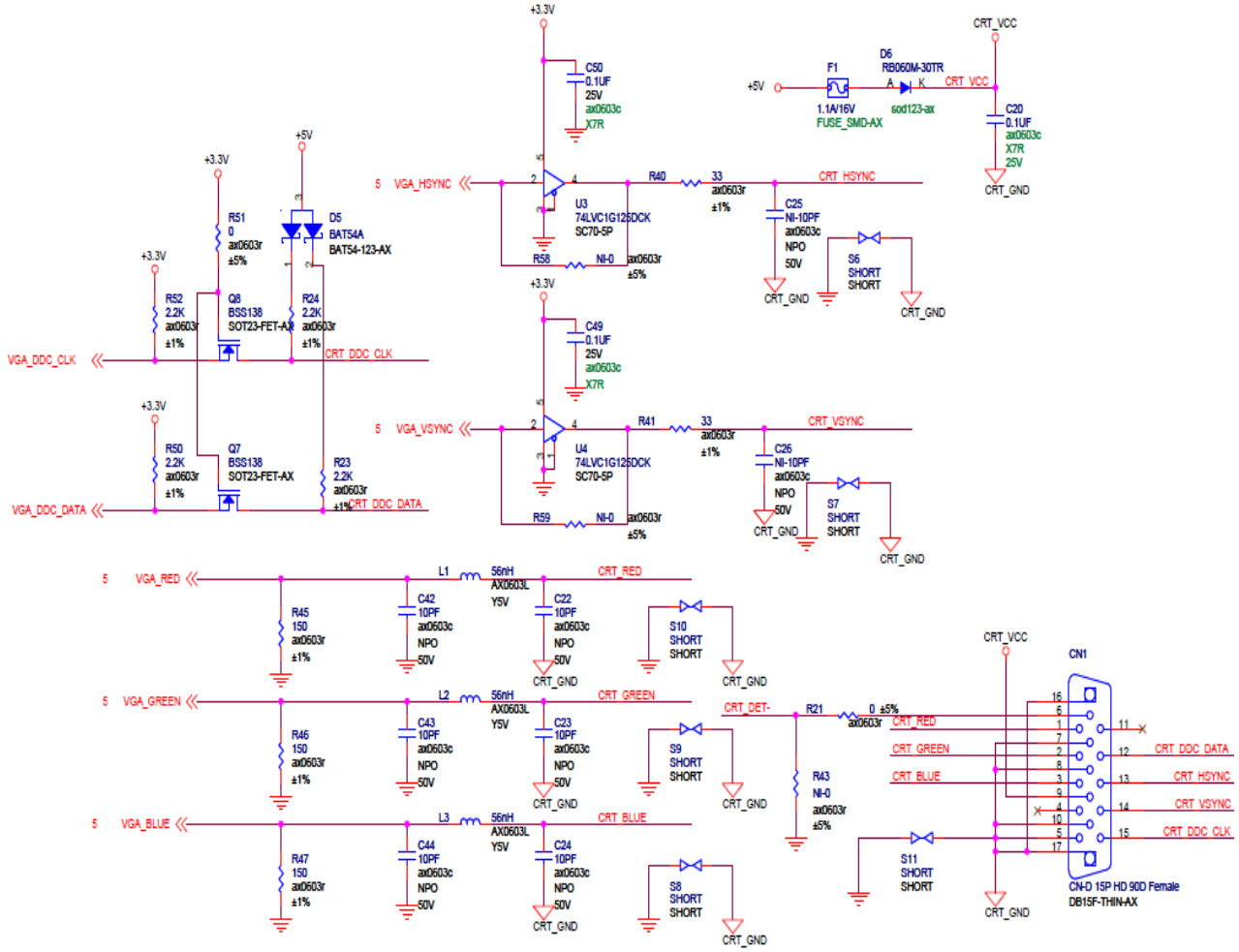


Figure 11-2 Analog VGA Schematic



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Chapter 12

12. Digital Audio Interface: AC'97 and HD Audio

12.1 AC'97 and HD Audio – Signal Definitions

The COM Express® Specification allocates seven pins on the A-B connector to support digital AC'97 and HD interfaces to audio CODEC on the Baseboard. The pins are available on all Module types. High-definition (HD) audio uses the same digital-signal interface as AC '97 audio. CODEC for AC '97 and HD Audio are different.

Table 12-1 Audio Pin-outs

Pin	Row A	Row B
26		
27		
28		AC/HDA_SDIN2
29	AC/HDA_SYNC	AC/HDA_SDIN1
30	AC/HDA_RST#	AC/HDA_SDIN0
31		
32	AC/HDA_BITCLK	
33	AC/HDA_SDOUT	

12.2 HDA/AC'97 – Routing Considerations

The AC_ signal set is comprised of single-ended signals that have a nominal trace impedance of 50Ω.

- Route AC_ signals in a point-to-point fashion above a continuously quiet reference plane.
- Create separate Analog and Digital Ground Planes and split them across the CODEC.

  Tie the Analog Ground to Digital Ground at a single point.
- Partition the design to group Analog parts as one group and Digital parts as another group.
- Route Analog and Digital signals as far apart as possible.

- Keep the Clock as far away as possible from analog input and voltage-reference pins.
- Use metal film resistors.
- Fill the region between the Analog signals with copper and tie it to Analog Ground.
- Fill the region between the Digital signals with copper and tie it to Digital Ground.
- Locate the Crystal or Oscillator close to Codec.
- Place the Codec in the quietest part of the Baseboard – away from significant current paths or ground bounce.
- See application notes from the Codec vendor for other useful information.

Figure 12-1 AUDIO ALC662Schematic (1)

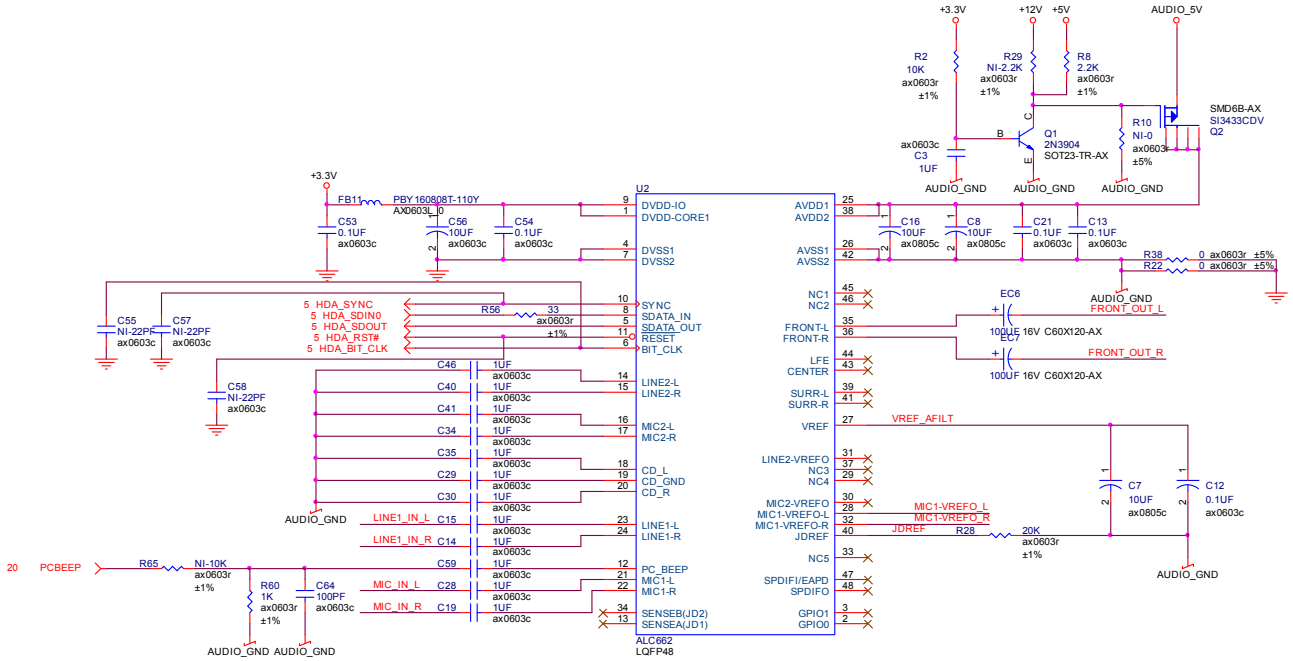
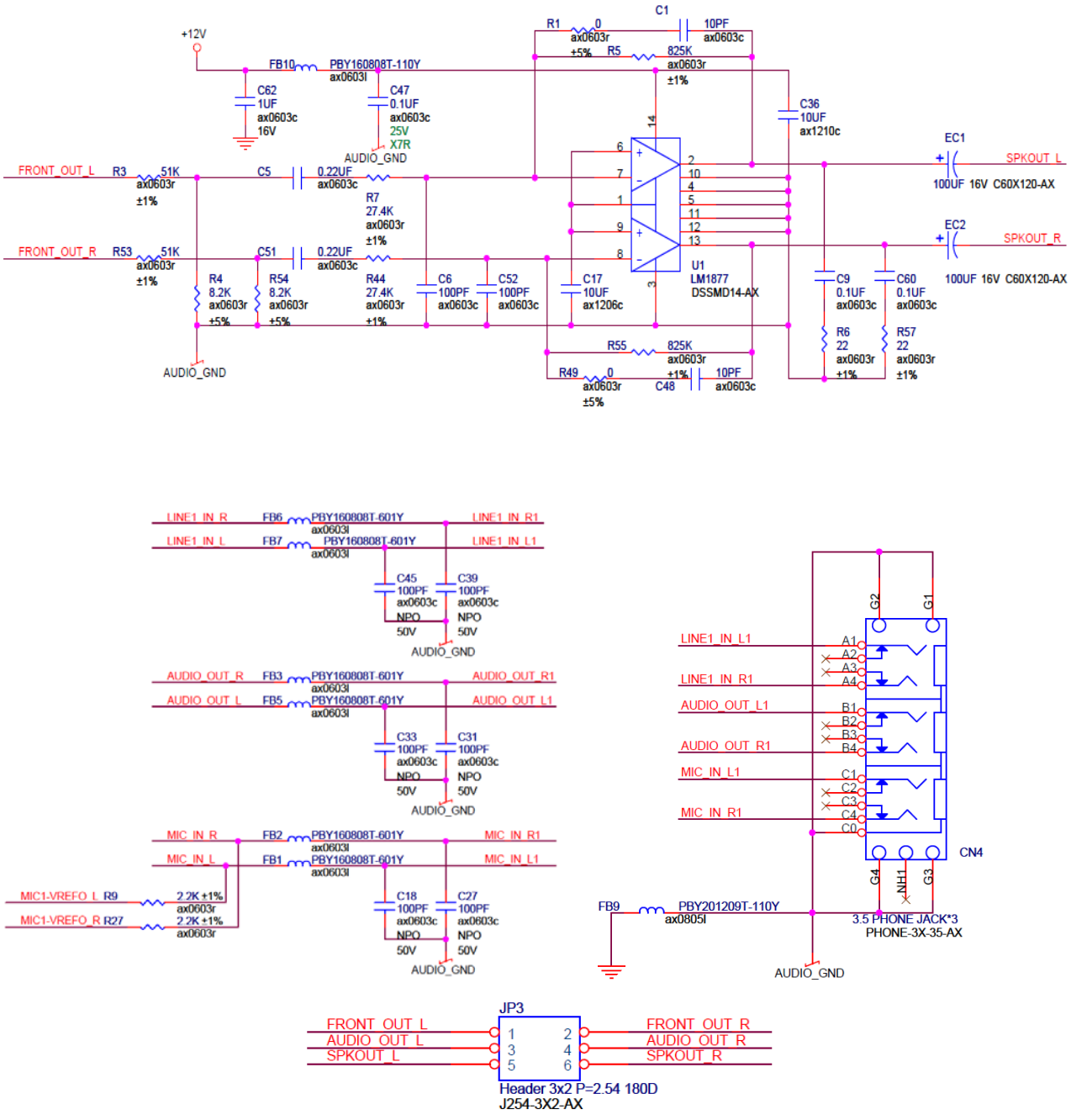


Figure 12-2 AUDIO ALC662 Schematic (2)



DEFAULT 1-3,2-4 Short

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Chapter 13

13. Digital Display Interface(DDI)

13.1 DDI – Signal Definitions

Up to three (Type 6) or one (Type 10) Digital Display Interfaces are added. These ports can be used to support DisplayPort or HDMI/DVI interfaces. Note that level shifters and back-power FETs might be required. The pin map uses a generic name for the Digital Display Interface pins. Table 13-1 below, details the mapping between the Digital Display Interface pins and the different types of video interfaces supported.

When implementing DisplayPort on the Baseboard, the DP_HP signal shall include a blocking FET to prevent back-drive current damage. The DP_HP signal shall be pulled-down to GND with a 100kΩ resistor.

When implementing HDMI level shifters shall be used on the TMDS signals. Bi-directional level shifters shall be used between the 3.3V and 5V CTRLCLK and CTRLDATA signals. The CTRLCLK signal with 2.2 kΩ pull up to 3.3V and 5V. The CTRLDATA signal with 10 kΩ pull up to 3.3V and 5V.

Table 13-1 Digital Display Interface

	Pin Name	Type 6 Pin Number	Type 10 Pin Number	DisplayPort	HDMI/DVI (TMDS Signaling)
DDI 1	DDI1_PAIR0+	D26	B71	DP1_LANE0+	TMDS1_DATA2+
	DDI1_PAIR0-	D27	B72	DP1_LANE0-	TMDS1_DATA2-
	DDI1_PAIR1+	D29	B73	DP1_LANE1+	TMDS1_DATA1+
	DDI1_PAIR1-	D30	B74	DP1_LANE1-	TMDS1_DATA1-
	DDI1_PAIR2+	D32	B75	DP1_LANE2+	TMDS1_DATA0+
	DDI1_PAIR2-	D33	B76	DP1_LANE2-	TMDS1_DATA0-
	DDI1_PAIR3+	D36	B81	DP1_LANE3+	TMDS1_CLK+
	DDI1_PAIR3-	D37	B82	DP1_LANE3-	TMDS1_CLK-
	DDI1_HPD	C24	B89	DP1_HPD	HDMI1_HPD
	DDI1_AUX+	D15(1)	B98(1)	DP1_AUX+	
	DDI1_AUX-	D16(1)	B99(1)	DP1_AUX-	
	DDI1_CTRLCLK	D15(1)	B98(1)		HDMI1_CTRLCLK
	DDI1_CTRLDATA	D16(1)	B99(1)		HDMI1_CTRLDATA
	DDI1_DDC_AUX_SEL	D34(1)	B95(1)	Low(1)	High(1)
DDI 2	DDI2_PAIR0+	D39		DP2_LANE0+	TMDS2_DATA2+
	DDI2_PAIR0-	D40		DP2_LANE0-	TMDS2_DATA2-
	DDI2_PAIR1+	D42		DP2_LANE1+	TMDS2_DATA1+
	DDI2_PAIR1-	D43		DP2_LANE1-	TMDS2_DATA1-
	DDI2_PAIR2+	D46		DP2_LANE2+	TMDS2_DATA0+
	DDI2_PAIR2-	D47		DP2_LANE2-	TMDS2_DATA0-
	DDI2_PAIR3+	D49		DP2_LANE3+	TMDS2_CLK+
	DDI2_PAIR3-	D50		DP2_LANE3-	TMDS2_CLK-
	DDI2_HPD	D44		DP2_HPD	HDMI2_HPD
	DDI2_AUX+	C32(1)		DP2_AUX+	
	DDI2_AUX-	C33(1)		DP2_AUX-	
	DDI2_CTRLCLK	C32(1)			HDMI2_CTRLCLK
	DDI2_CTRLDATA	C33(1)			HDMI2_CTRLDATA
	DDI2_DDC_AUX_SEL	C34(1)		Low(1)	High(1)
DDI 3	DDI3_PAIR0+	C39		DP3_LANE0+	TMDS3_DATA2+
	DDI3_PAIR0-	C40		DP3_LANE0-	TMDS3_DATA2-
	DDI3_PAIR1+	C42		DP3_LANE1+	TMDS3_DATA1+
	DDI3_PAIR1-	C43		DP3_LANE1-	TMDS3_DATA1-
	DDI3_PAIR2+	C46		DP3_LANE2+	TMDS3_DATA0+
	DDI3_PAIR2-	C47		DP3_LANE2-	TMDS3_DATA0-
	DDI3_PAIR3+	C49		DP3_LANE3+	TMDS3_CLK+
	DDI3_PAIR3-	C50		DP3_LANE3-	TMDS3_CLK-
	DDI3_HPD	C44		DP3_HPD	HDMI3_HPD
	DDI3_AUX+	C36(1)		DP3_AUX+	
	DDI3_AUX-	C37(1)		DP3_AUX-	
	DDI3_CTRLCLK	C36(1)			HDMI3_CTRLCLK
	DDI3_CTRLDATA	C37(1)			HDMI3_CTRLDATA
	DDI3_DDC_AUX_SEL	C38(1)		Low(1)	High(1)

Note:

1. DDI[1:3]_DDC_AUX_SEL are the signals that select the function of DDI[1:3]_AUX+/ DDI[1:3]_CTRLCLK and DDI[1:3]_AUX-/ DDI[1:3]_CTRLDATA. These pins have 1M pull down to ground on module. If the DDI_DDC_AUX_SEL pin is floating on baseboard, the AUX pair is used for the DP_AUX+/- signals. For HDMI/DVI application, the DDI_DDC_AUX_SEL pin must pull up 100K to +3.3V.

13.2 DDI – Routing Considerations

Table 13-2 DDI Layout Guidelines

Parameter	Trace Louting
Differential Impedance	85 Ω ±15%
Single-End Impedance	50 Ω ±10%
Signal length	3.2 inches
Spacing between pairs-to-pairs (inter-pair)	Min. 15mils
Spacing between differential pairs and high-speed periodic signals	Min. 15mils
Spacing between differential pairs and low-speed non periodic signals	Min. 15mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between differential pairs (inter-pair)	Max. 1 inch
Reference plane	GND
Via Usage	Max. 2
AC coupling capacitors	100nF

13.3 DDI – Reference Schematics

13.3.1 DVI/HDMI/DisplayPort Example

Figure 13-1 DVI Schematic (1)

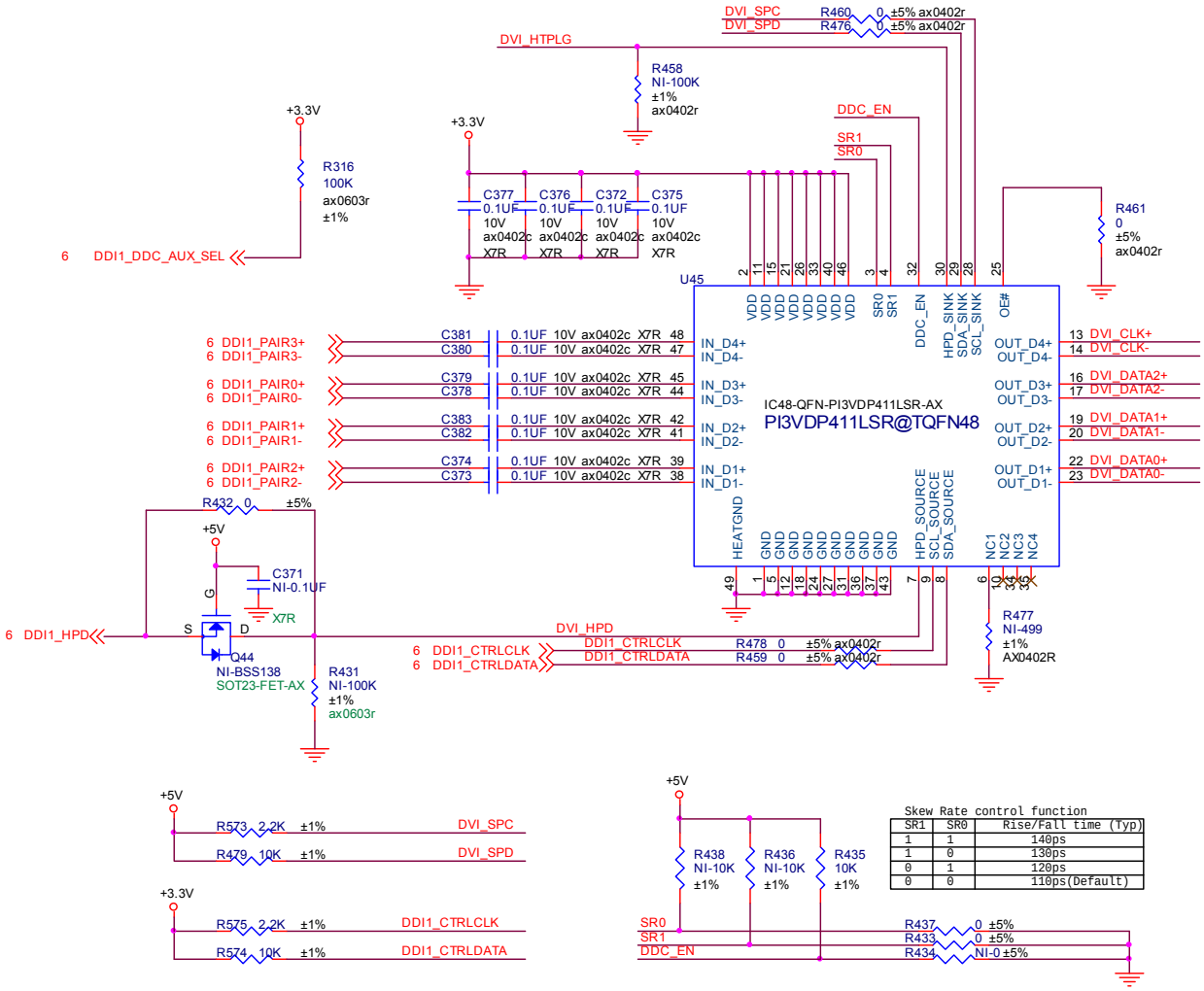


Figure 13-1 DVI Schematic (2)

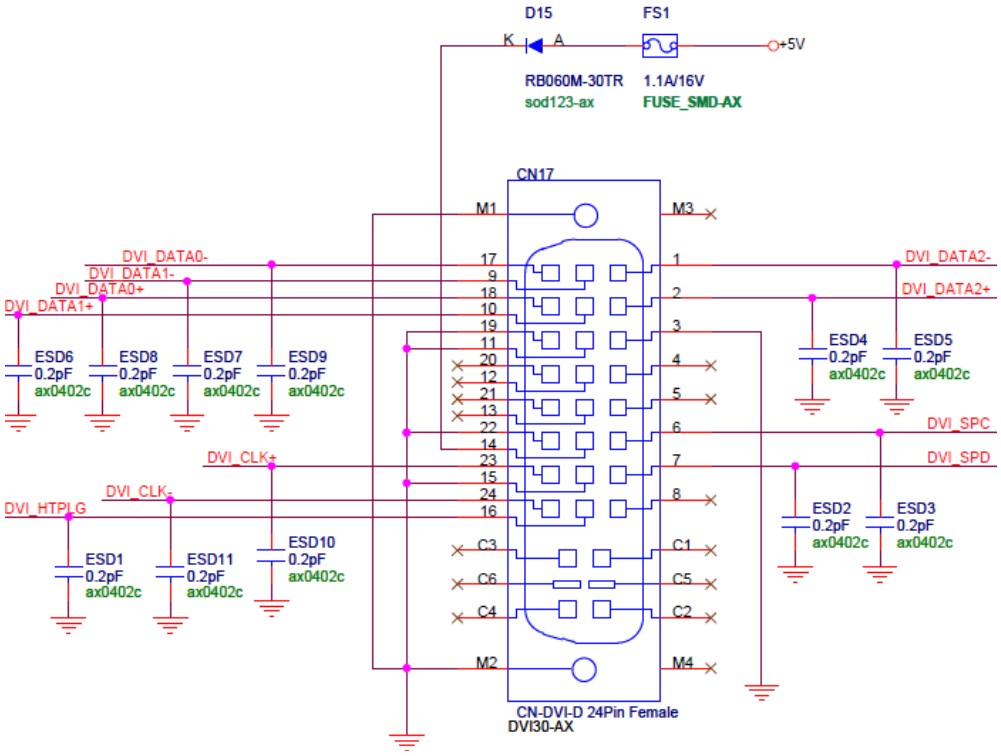


Figure 13-2HDMI Schematic

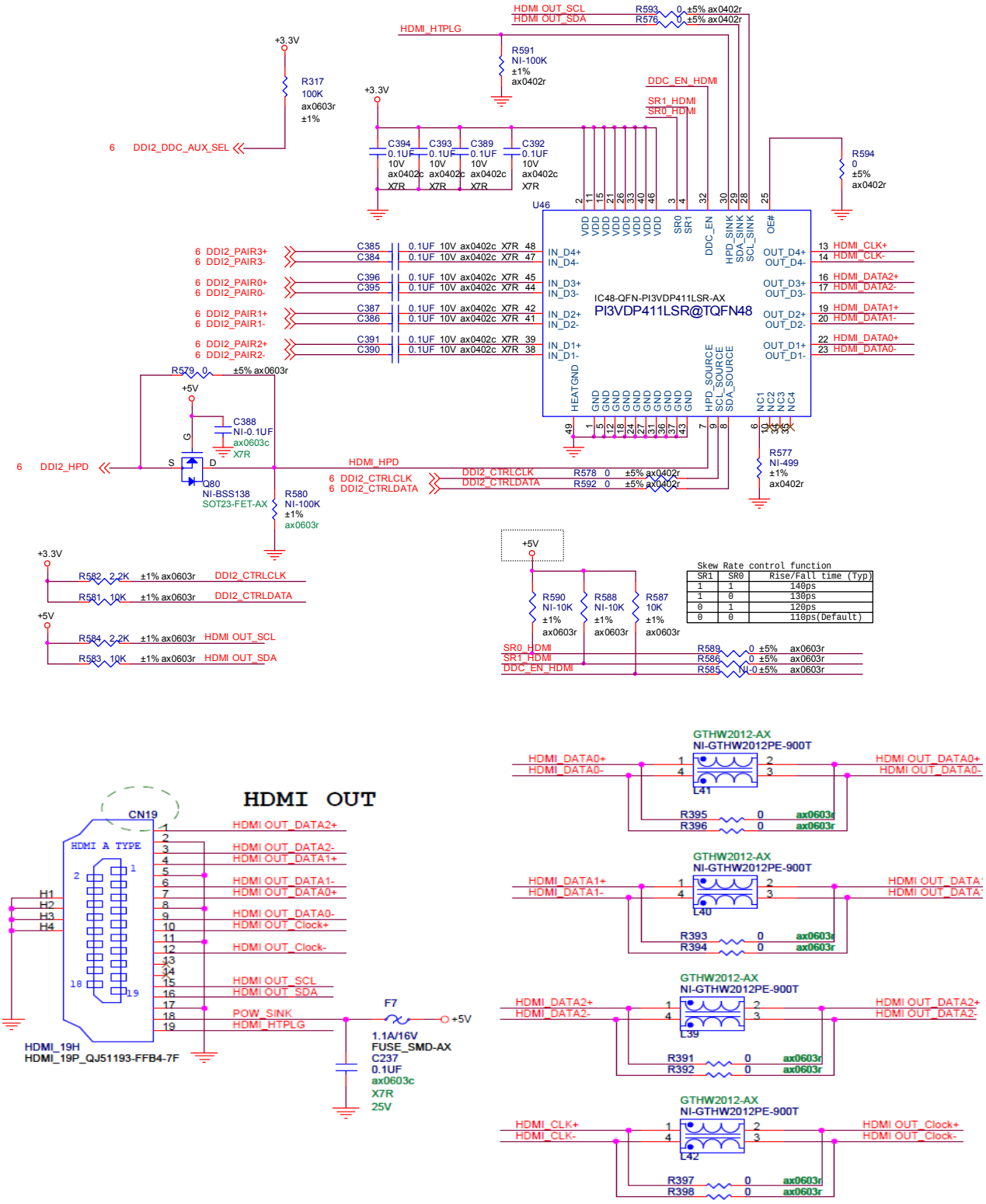
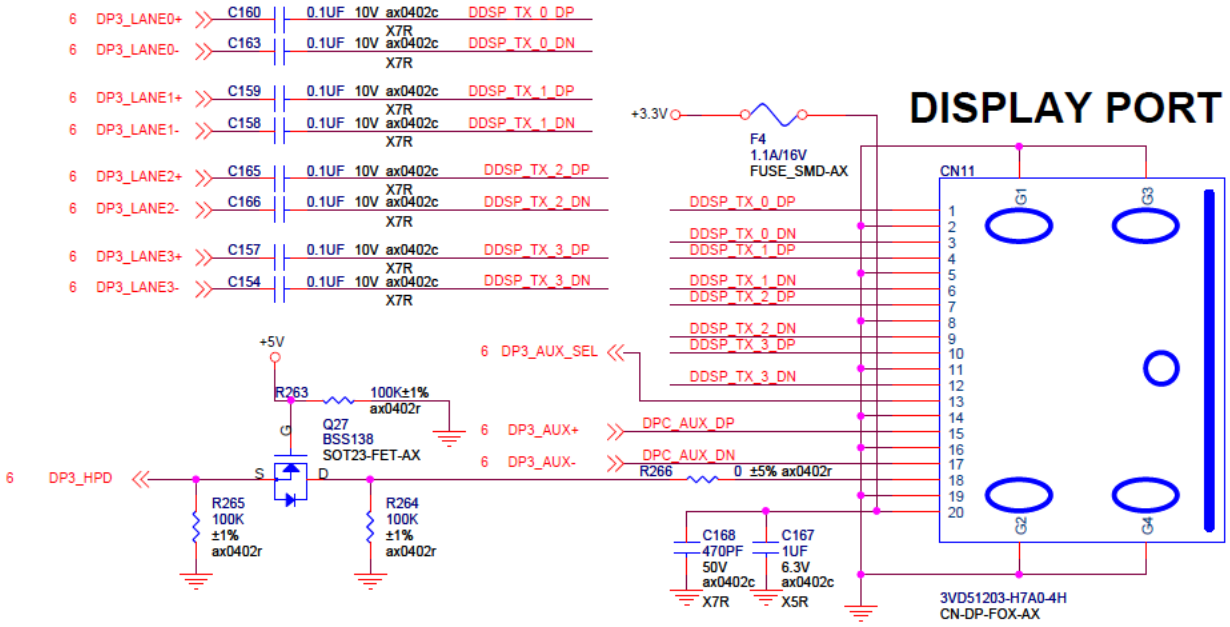


Figure 13-3 DisplayPort Schematic

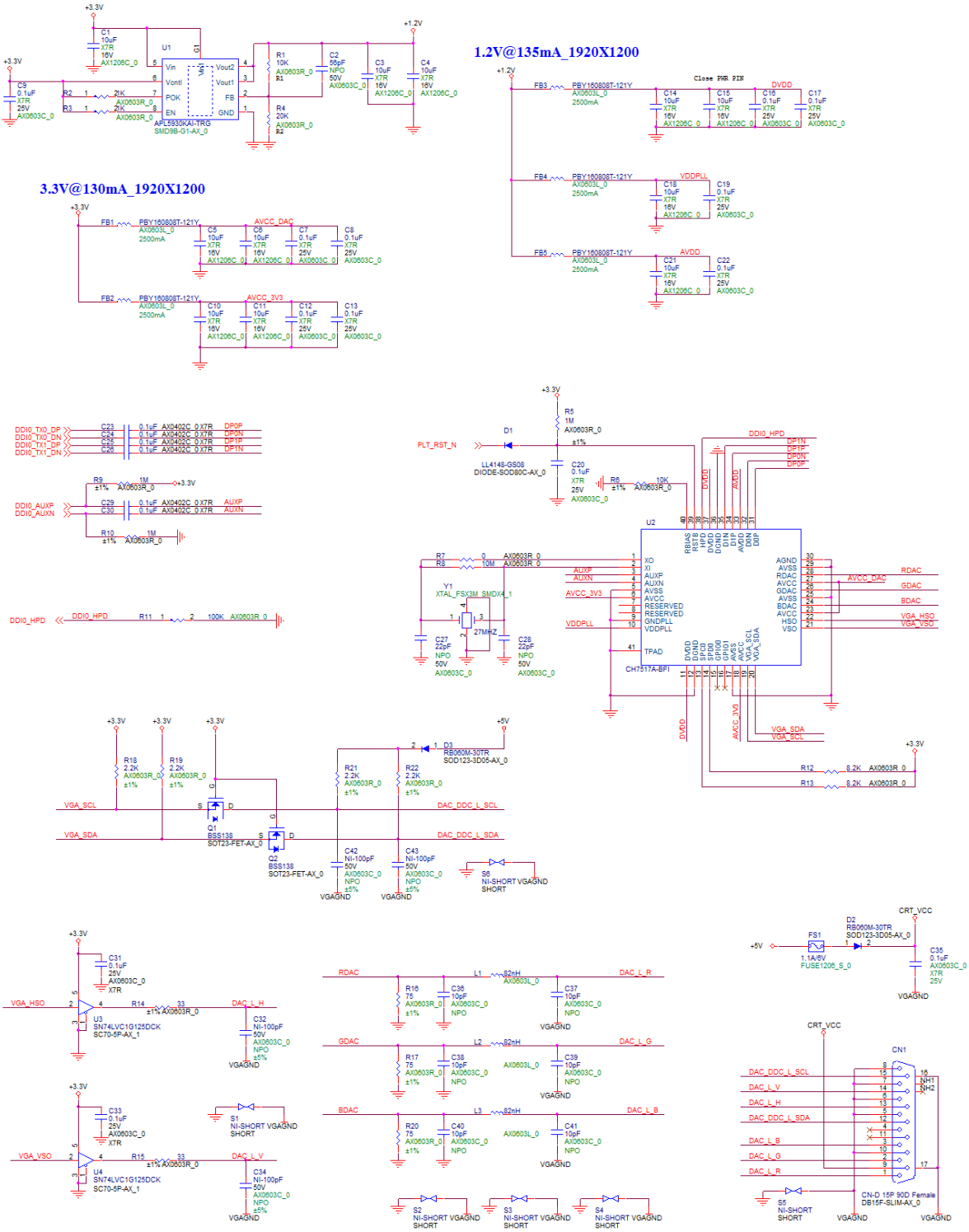


13.3.2 DisplayPort to VGA Example

DisplayPort signals through a DisplayPort to VGA Adapter IC can translate to VGA signals. The IC integrates a DisplayPort receiver and a digital-to analog converter.

The CH7517A is compliant with DisplayPort specification version 1.2 and Embedded DisplayPort (eDP) specification version 1.3. With internal HDCP key Integrated, the device support HDCP 1.3 specifications. In the device's receiver block, which supports two DisplayPort Main Link Lanes input with data rate running at either 1.62Gb/s or 2.7Gb/s, can accept RGB digital formats in either 18-bit 6:6:6 or 24-bit 8:8:8, and converted the input signal to VGA output up to 1920x1200@60Hz.

Figure 13-4 DisplayPort to VGA Schematic



- Power Supply Decoupling

Table as below is the CH7517A power supply pin assignments.

Pin Assignment	Type	Symbol	Description
11,37	Power	DVDD	Digital supply voltage (1.2V)
33	Power	AVDD	Analog supply voltage (1.2V)
10	Power	VDD_PLL	PLL supply voltage (1.2V)
6,18	Power	AVCC	Analog supply voltage (3.3V)
23,27	Power	AVCC_DAC	DAC supply voltage (3.3V)
12,36	Ground	DGND	Digital supply ground
30	Ground	AGND	Analog supply ground
9	Ground	GNDPLL	PLL supply ground
5,17,25,29	Ground	AVSS	Analog supply ground

The optimum power supply decoupling is accomplished by placing a 0.1μF ceramic capacitor to each of the power supply pins. These capacitors should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance.

- The RBIAS (40) sets the Band-gap Bias Voltage. A 10 K-Ohm, 1% tolerance resistor should be connected between RBIAS and GND.

- The RSTB (39) is the chip reset pin for CH7517. RSTB pin, which is internally pulled-up, places the device in the power on reset condition when this pin is low.
  There are two reset methods. One is RC reset. The power supply should be valid and stable for at least 9ms before RSTB becomes invalid as shown in Figure 13-4-1. A 1 M_ and 0.1uF RC reset circuit is recommended.

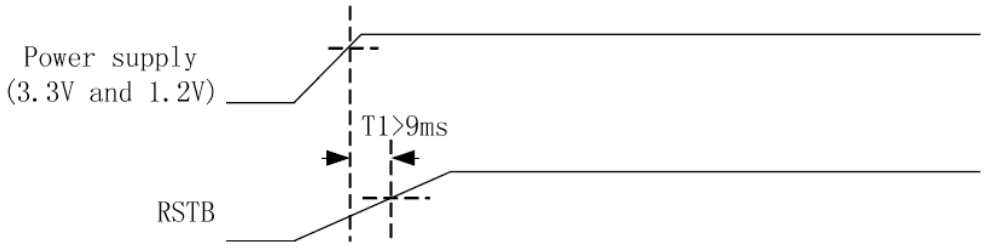
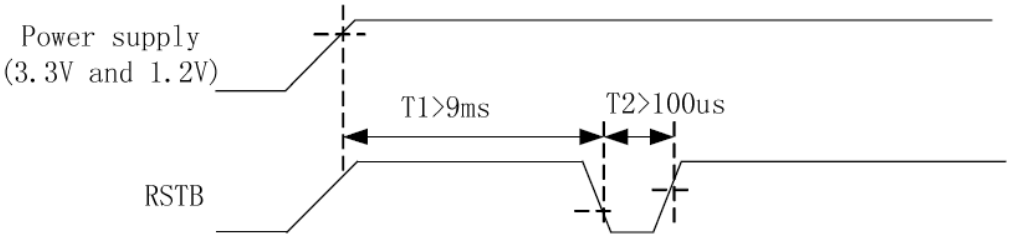


Figure 13-4-1: Power on and reset timing of RC

Another method is using an external reset signal. In this case, the power supply should be valid and stable for at least 9ms before the reset signal is valid. The pulse width of valid reset signal should be at least 100us. The timing is shown in Figure 13-4-2.

Figure 13-4-2: Power on and reset timing of external reset



- 27MHz crystal can be connected to these pins of XI (2), XO (1) as the CH7517 optional reference clock input. In PCB design, 27MHz crystal must be placed as close as possible to the XI and XO pins, with traces connected from point to point, overlaying the ground plane.

- SPC0 (13) and SPD0 (14) function as a serial interface where SPD0 is bi-directional data and SPC0 is an input only serial clock. In the reference design, SPD0 and SPC0 pins are pulled up to +3.3V with 8.2kΩ resistors.

- VGA_SCL (19) and VGA_SDA (20) are used to interface with the DDC of VGA monitor. This DDC pair needs to be pulled up to 5V through 2.2KΩ resistors. A low instantaneous forward voltage diode is used to avoid back drive current from VGA monitor.

- The DP0P/N (31) (32), DP1P/N (34) (35) pins accept two AC-coupled differential pair signals from DisplayPort transmitter.

  Since the digital serial data of the CH7517 may be toggled at speeds up to 2.7 GHz, it is strongly recommended that the connection of these video signals between the graphics controller and the CH7517 should be kept as short as possible and be isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals. It is recommended that 5 mils traces should be used in routing these signals. There should be 7 mils spacing between each intra pair.

  The length for a pair of intra differential signals should be matched within 5 mils. The length for inter pairs should be matched within 2 inches..

- The AUXP (3) and AUXN (4) two pins are DisplayPort AUX channel control that accepts a half-duplex, bi-directional AC-coupled differential signal. They must have the AC-coupling capacitors, and 100nF capacitors are recommended in this document.

- The HPD (38) pin indicates whether this device is active or not. It also generates interrupt pulse as defined by DisplayPort standard. Output voltage is 3.3V. A resistor more than 100K-Ohm should be connected between this pin and ground.

- The RDAC (28), GDAC (26), BDAC (24) three on-chip 8-bit high speed DACs provide RGB output. If the DACs require a double termination, a 75 Ω resistor should be placed between each DAC pin and the ground.
- The HSO (22) and VSO (21) are COMS output pins, the voltage level is the same with AVCC.

MEMO:

3.0 update to 3.1

1. Modify Parameters of “Spacing between differential pairs and high-speed periodic signals”

Chapter 14

14 LPC Bus Implementation

14.1 LPC Bus – Signal Definitions

The LPC (Low Pin Count) bus is a versatile, easy-to-use bus than can support low-bandwidth peripherals such as serial ports, firmware memory, legacy peripherals and general-purpose inputs and outputs. The LPC bus uses four data bits and a 33MHz clock, yielding a maximum bandwidth of approximately 16 megabytes per second – about double the bandwidth of the legacy ISA bus. It is straightforward to develop PLDs or FPGAs that interface to the LPC bus.

The LPC bus is implemented on the COM Express A-B connector per Table 14-1 below.

Table 14-1 LPC Signals

Pin	Row A	Row B
1		
2		
3		LPC_FRAME#
4		LPC_AD0
5		LPC_AD1
6		LPC_AD2
7		LPC_AD3
8		LPC_DRQ0#
9		LPC_DRQ1#
10		LPC_CLK
18		SUS_STAT#
50	LPC_SERIRQ	CB_RESET#

Signal SUS_STAT- is a Module output that may be used to notify LPC devices of an imminent suspend operation.

14.2 LPC Bus – Routing Considerations

14.2.1 LPC Bus Routing – General Signals

Parameter	Trace Louting
Transfer Rate @ 33MHz	16 MBit/s
Single-End Impedance	55 Ω ±10%
Maximum data and control signal length	15.0 inches
Maximum clock signal length	8.88 inches
Length matching between single ended signals	Max. 200mils
Length matching between clock signals	Max. 200mils
Reference plane	GND
Via Usage	Try to minimize number of vias

See the LPC bus section in Appendix B for a summary of trace-routing parameters and guidelines.

14.2.2 LPC Bus Clock Routing

The LPC bus clock is similar to the PCI bus clock and should be treated similarly. The COM Express® Specification allows 1.6 ns +/- 0.1ns for the propagation delay of the LPC clock from the Module pin to the LPC device destination pin. Using a typical propagation delay value of 180 ps / inch, this works out to 8.88 inches of Baseboard trace for a device-down application. For device-up situations, 2.5 inches of clock trace are assumed to be on the LPC slot card (by analogy to the PCI specification). This is deducted from the 8.88 inches, yielding 6.38 inches.

On a Baseboard with a small form factor, serpentine clock traces may be required to meet the clock-length requirement.

Route the LPC clock as a single-ended, 50-ohm trace with generous clearance to other traces and to itself. A continuous ground-plane reference is recommended. Routing the clock on a single ground references internal layer is preferred to reduce EMI.

The COM Express® Specification brings a single LPC clock out of the Module. If there are multiple LPC targets on the Baseboard design, then a zero delay clock buffer is recommended. This provides a separate copy of the LPC clock to each target. The overall delay from the Module LPC clock pin to the target LPC device clock pin should be 1.6 ns.

MEMO:

3.0 update to 3.1

1. Modify Parameters of “Transfer Rate @ 33MHz” and “Single-End Impedance”

Chapter 15

15. I²C BUS

15.1 I²C Bus – Signal Definitions

The I²C (Inter-Integrated Circuit) bus is a two-wire serial bus originally defined by Philips. The bus is used for low-speed (400kbps) communication between system ICs. The bus is often used to access small serial EEPROM memories and to set up IC registers.

A reference to the I²C source specification can be found in Appendix B.

There are four types of I²C bus that are brought to the Module connector that use the I²C format and protocol. These I²C buses are summarized in Table 15-1 below.

Table 15-1 I²C Signal Groups

I²C Bus Function	Clock	Data
System Management Bus	SMB_CK	SMB_DAT
LVDS display parameters	LVDS_I2C_CK	LVDS_I2C_DAT
VGA display parameters	VGA_I2C_CK	VGA_I2C_DAT
DDI display parameters	DDI[1:3]_CTRLCLK	DDI[1:3]_CTRLDATA

All of the I²C buses are special-purpose buses. Baseboard designers should take special cares when connecting to the special-purpose buses. The System Management Bus (SMB) is used on the Module to collect information and controls many important Module subsystems, including DRAM SPD, system hardware monitors, and clock synthesizers and buffers. A fault introduced on the SMB could prevent the Module from functioning.

MEMO:

Chapter 16

16. Electrical Specification

16.1 Input Power – General Considerations

The Basic and Compact Modules shall use a single main power rail with a nominal value of +12V.
The Mini Module shall support a wide range power supply of 4.75V to 20.0V.
Two additional rails are specified: a +5V standby power rail and a +3V battery input to power the Module Real-time Clock (RTC) circuit in the absence of other power sources.
The +5V standby rail may be left unconnected on the Baseboard if the standby functions are not required by the application. Likewise, the +3V battery input may be left open if the application does not require the RTC to keep time in the absence of the main and standby sources. There may be Module specific concerns regarding storage of system setup parameters that may be affected by the absence of the +5V standby and / or the +3V battery.

The rationale for this power-delivery scheme is:

- Module pins are scarce. It is more pin-efficient to bring power in on a higher voltage rail.
- Single supply operation is attractive to many users.
- Contemporary chipsets have no power requirements for +5V other than to provide a reference voltage for +5V tolerant inputs. No COM Express® Module pins are allocated to accept +5V except for the +5V standby pins. In the case of an ATX supply, the switched (non standby) +5V line would not be used for the COM Express® Module, but it might be used elsewhere on the Baseboard.

16.2 Input Power – Current Load

The Module connector pins limit the amount of power that can be brought into the COM Express® Modules. The limit are different for Module Pin-out Type 10 vs. Pin-out Type 6, based on the number of 12V power pins as Pin-out Type 10 has fewer pins available.

Table 16-1 Input Power- Pin-out Type 10 Module(Single Connector,220 pins)

Power Rail	Module Pin Current Capability (Amps)	Normal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (mV)	Max. Module Input Power (derated input) (Watts)	Assumed Conversion Efficiency	Max Load Power (Watts)
VCC_12V	6	12	11.4-12.6	11.4	+/-100	68	85%	58
Wide input (Mini)	6		4.75-20.0	4.75	+/-100	28		
VCC_5V_SBY	2	5	4.75-5.25	4.75	+/-50	9		
VCC_RTC	0.5	3	2.0-3.3		+/-20			

Table 16-2 Input Power- Pin-out Type 6 Module(Dual Connector,440 pins)

Power Rail	Module Pin Current Capability (Amps)	Normal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (mV)	Max. Module Input Power (derated input) (Watts)	Assumed Conversion Efficiency	Max Load Power (Watts)
VCC_12V	12	12	11.4-12.6	11.4	+/-100	137	85%	116
VCC_5V_SBY	2	5	4.75-5.25	4.75	+/-50	9		
VCC_RTC	0.5	3	2.0-3.3		+/-20			

16.3 Input Power – Sequencing

COM Express® input power sequencing requirements are as follows:

VCC_RTC shall come up at the same time or before VCC_5V_SBY comes up.

VCC_5V_SBY shall come up at the same time or before VCC_12V comes up.

PWROK shall be active at the same time or after VCC_12V comes up.

PWROK shall be inactive at the same time or before VCC_12V goes down.

VCC_12V shall go down at the same time or before VCC_5V_SBY goes down.

VCC_5V_SBY shall go down at the same time or before VCC_RTC goes down.

Wide input (Mini) shall follow the power sequencing of the VCC_12V.

Figure 16-1 Power Sequencing

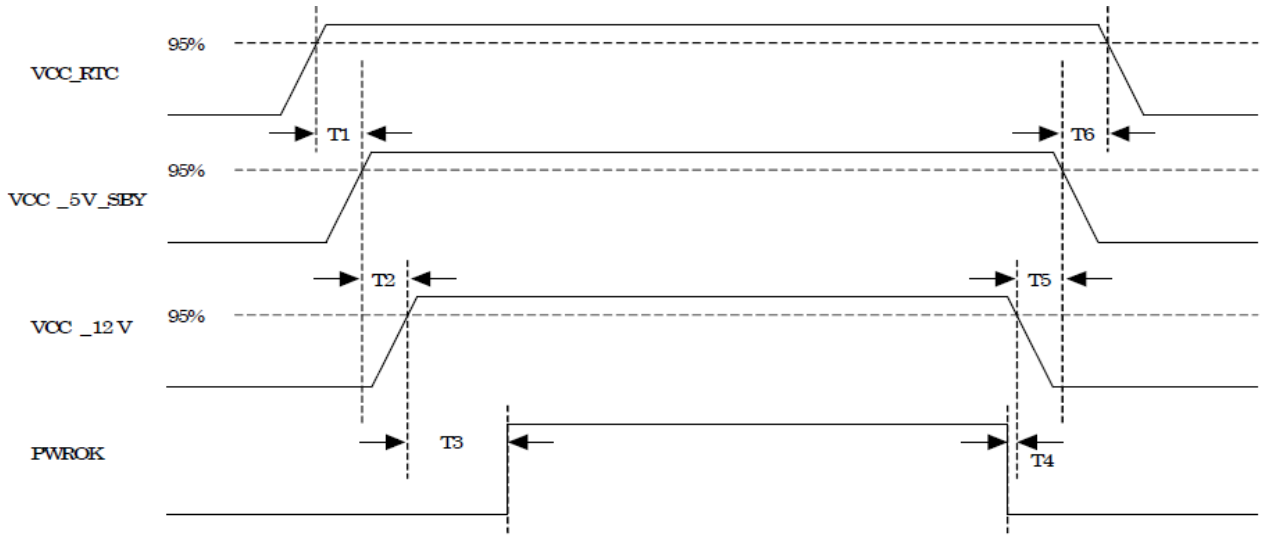


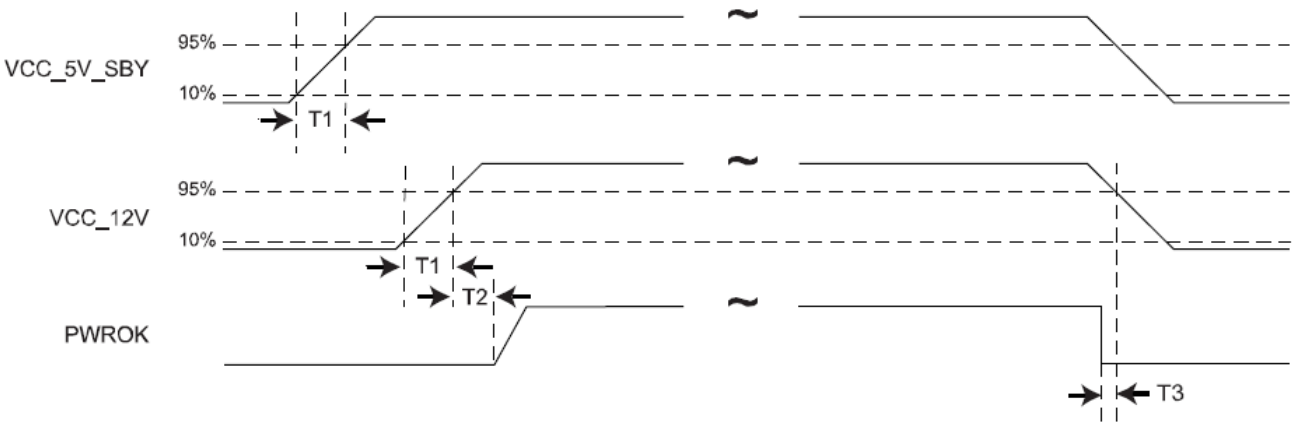
Table 16-3 Power Sequencing

T1	VCC_RTC rise to VCC_5V_SBY rise	≥ 0 ms
T2	VCC_5V_SBY rise to VCC_12V rise	≥ 0 ms
T3	VCC_12V rise to PWROK rise	≥ 0 ms
T4	PWROK fall to VCC_12V fall	≥ 0 ms
T5	VCC_12V fall to VCC_5V_SBY fall	≥ 0 ms
T6	VCC_5V_SBY fall to VCC_RTC fall	≥ 0 ms

16.4 Input Power – Rise Time

The input voltages to the COM Express module VCC_12V, wide input (Mini) and VCC_5V_SBY if used shall rise from ≤10% of nominal to within the regulation ranges within 0.1 ms to 20 ms (0.1 ms ≤ T2 ≤ 20 ms). There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of its final set point within the regulation band. The smooth turn-on requires that, during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive and have a value of between 0 V/ms and [Vout, nominal / 0.1] V/ms. Also, for any 5ms segment of the 10% to 90% rise time waveform, a straight line drawn between the end points of the waveform segment must have a slope ≥ [Vout, nominal / 20] V/ms.

Figure 16-2 Input Power Rise Time



T1,min = 0.1ms

T1,max = 20ms

T2 ≥ 0ms

T3 ≥ 0ms

The values chosen were selected to be compatible and enable use of ATX specification R2.2

MEMO:

Chapter 17

17. BIOS Consideration

17.1 Baseboard Super I/O Support

A Baseboard Super I/O implementation usually requires BIOS customization to support the Super I/O. If the Baseboard uses the same Super I/O as the Axiomtek reference boards, then it may be possible to use the standard legacy BIOS that goes with the particular Module. The Super I/O that on Axiomtek's reference boards of Type 6 is W83627DHG-PT, Type 10 is NCT6106D.

MEMO:

Chapter 18

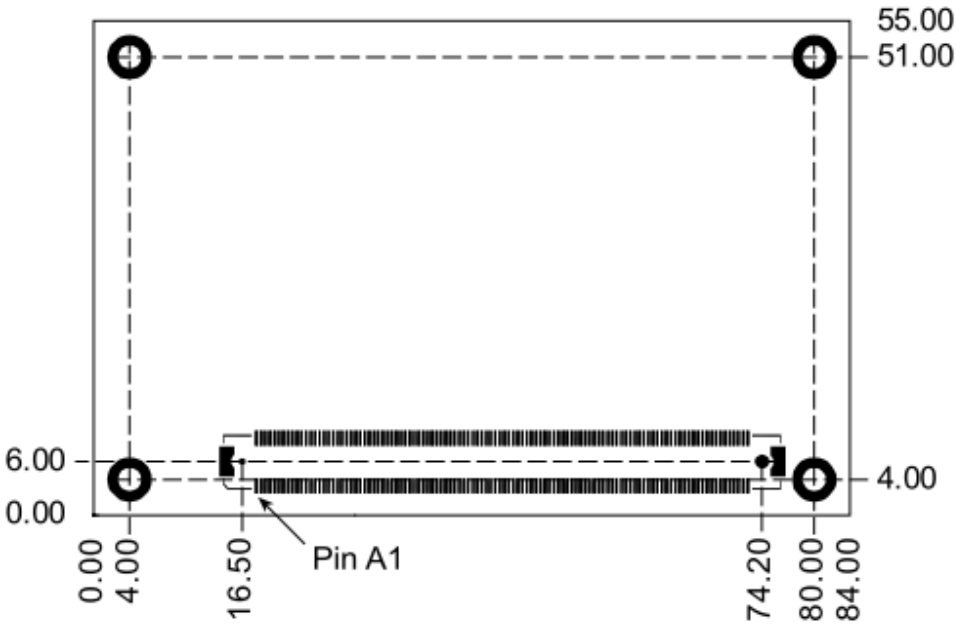
18. Mechanical Specifications

18.1 Module Size — Mini Module

The PCB size for the Mini Module shall be 84mm x 55mm. The PCB thickness shuld be 2mm to allow high layer count stack-ups and facilitate a standard 'z' dimension between the Baseboard and the top of the heat-spreader. (See Section 18.9,"Heat-Spreader").

The holes shown in this drawing are intended for mounting the module / heat-spreader combination to the Baseboard. An independent, implementation specific set of holes and spacers shall be used to attach the heat-spreader to the Module.

Figure 18-1 Mini Module Form Factor



All dimensions are shown in millimeters.

Tolerances shall be ± 0.25mm [±0.010"], unless noted otherwise.

The 220 pin connector pair shall be mounted on the backside of the PCB and is seen "through" the board in this view. The 4 mounting holes shown shall use 6 mm diameter pads and shall have 2.7mm plated holes, for use with 2.5mm hardware. The pads shall be tied to the PCB ground plane.

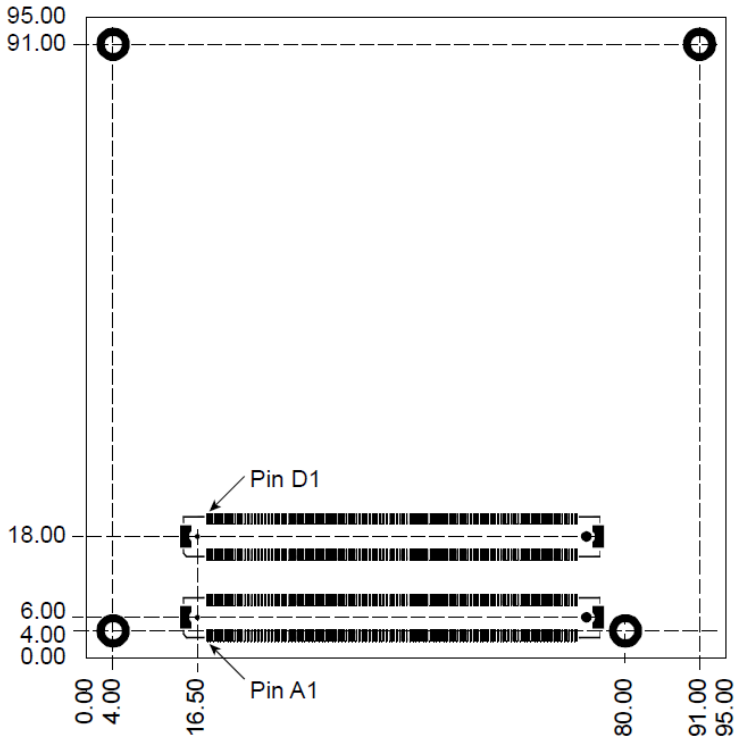
18.2 Module Size — Compact Module

The PCB size for the Compact Module shall be 95mm x 95mm. The PCB thickness may be 2mm to allow high

layer count stack-ups and facilitate a standard 'z' dimension between the Baseboard and the top of the heat-spreader. (See Section 18.9,"Heat-Spreader").

The holes shown in this drawing are intended for mounting the module / heat-spreader combination to the Baseboard. An independent, implementation specific set of holes and spacers shall be used to attach the heat-spreader to the Module.

Figure 18-2 Compact Module Form Factor



All dimensions are shown in millimeters.

Tolerances shall be ± 0.25mm [±0.010"], unless noted otherwise.

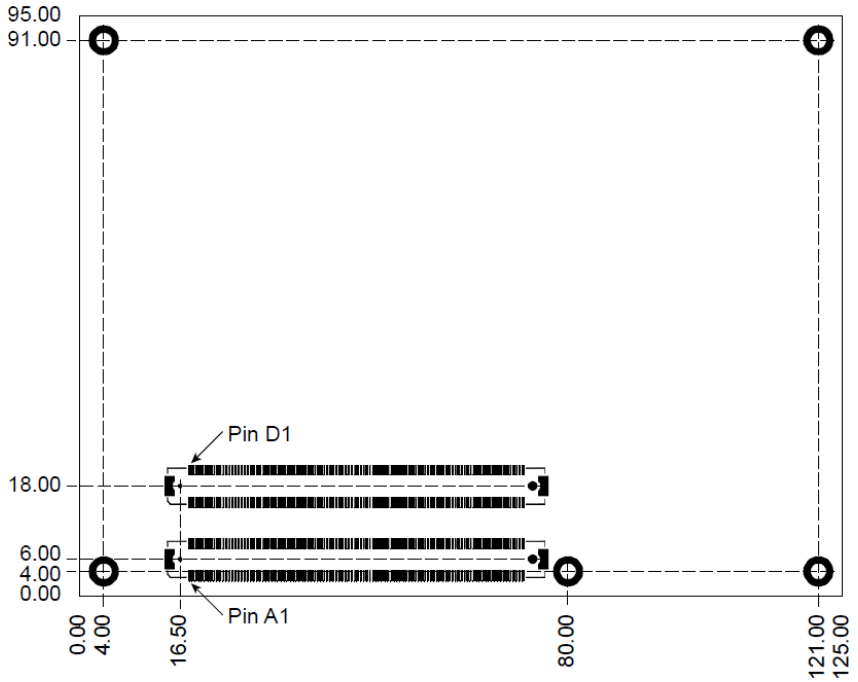
The 440 pin connector pair shall be mounted on the backside of the PCB and is seen "through" the board in this view. The 4 mounting holes shown shall use 6 mm diameter pads and shall have 2.7mm plated holes, for use with 2.5mm hardware. The pads shall be tied to the PCB ground plane.

18.3 Module Size — Basic Module

The PCB size for the Basic Module shall be 125mm x 95mm. The PCB thickness may be 2mm to allow high layer count stack-ups and facilitate a standard 'z' dimension between the Baseboard and the top of the heat-spreader. (See Section 18.9,"Heat-Spreader").

The holes shown in this drawing are intended for mounting the module / heat-spreader combination to the Baseboard. An independent, implementation specific set of holes and spacers shall be used to attach the heat-spreader to the module.

Figure 18-3 Basic Module Form Factor



All dimensions are shown in millimeters.

Tolerances shall be ± 0.25mm [±0.010"], unless noted otherwise.

The 440 pin connector pair shall be mounted on the backside of the PCB and is seen "through" the board in this view. The 5 mounting holes shown shall use 6 mm diameter pads and shall have 2.7mm plated holes, for use with 2.5mm hardware. The pads shall be tied to the PCB ground plane.

18.4 Module Connector

The module connector for Pin-out Types 2 through 6 shall be a 440-pin receptacle that is composed of 2 pieces of a 220-pin, 0.5 mm pitch receptacle. The pair of connectors may be held together by a plastic carrier during assembly to allow handling by automated assembly equipment. Module Pin-out Type 1/10 shall use a single 220-pin, 0.5 mm pitch receptacle. The connectors shall be qualified for LVDS operation up to 6.25GHz, to support PCI Express Generation 2 signaling speeds.

18.5 Baseboard Connector

The Baseboard connector for module Pin-out Types 6 shall be a 440-pin plug that is composed of 2 pieces of a 220-pin, 0.5 mm pitch plug. The pair of connectors may be held together by a plastic carrier during assembly to allow handling by automated assembly equipment. Baseboards intended only for use with Pin-out Type 10 module may use a single 220-pin, 0.5 mm pitch plug. The connectors shall be qualified for LVDS operation up to 6.25GHz, to support PCI Express Generation 2 signaling speeds. The Baseboard plugs are available in a variety of heights. The Baseboard shall use either the 5mm or 8mm heights.

A source for the individual 5 mm stack height 220 pin plug is:

FOXCONN QT002206-2131-3H 0.5 mm pitch Free Height 220 pin 5H Plug or equivalent

A source for the combined 5mm stack height 440-pin plug (composed of 2 pieces of the 220 pin plug held by a carrier) is:

FOXCONN QT002206-2131-3H 0.5 mm pitch Free Height 220 pin 5H Plug or equivalent

A source for the individual 8 mm stack height 220 pin plug is:

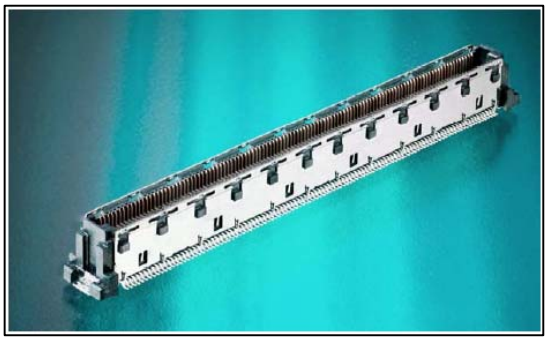
FOXCONN QT002206-4131-3H 0.5 mm pitch Free Height 220 pin 8H Plug or equivalent

A source for the combined 8 mm stack height 440 pin plug (composed of 2 pieces of the 220 pin plug held by a carrier) is:

FOXCONN QT002206-4131-3H 0.5 mm pitch Free Height 220 pin 8H Plug or equivalent

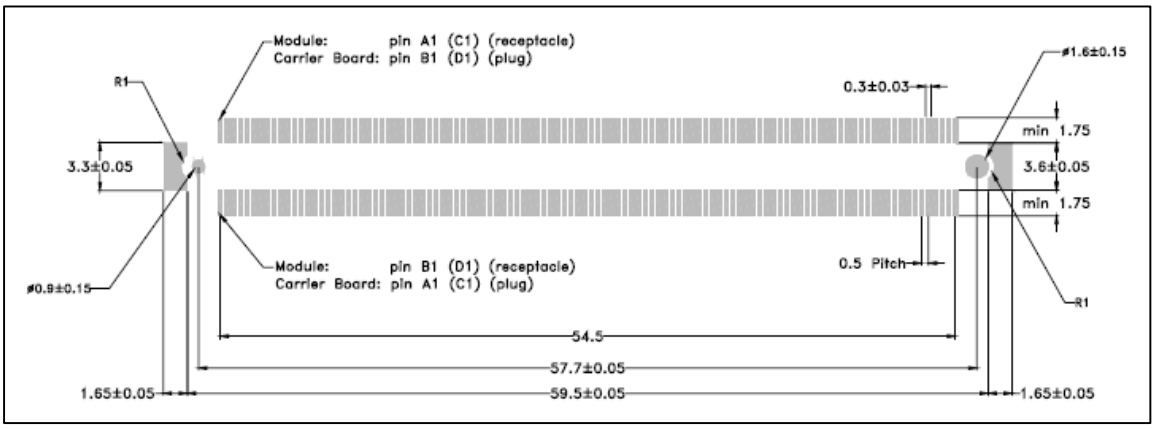
The Baseboard connector is a plug by virtue of the vendor's technical definition of a plug, and to some users it looks like a receptacle.

Figure 18-4Baseboard Plug(8-mm Version)



18.6 Connector PCB Pattern

Figure 18-5Connector PCB Pattern

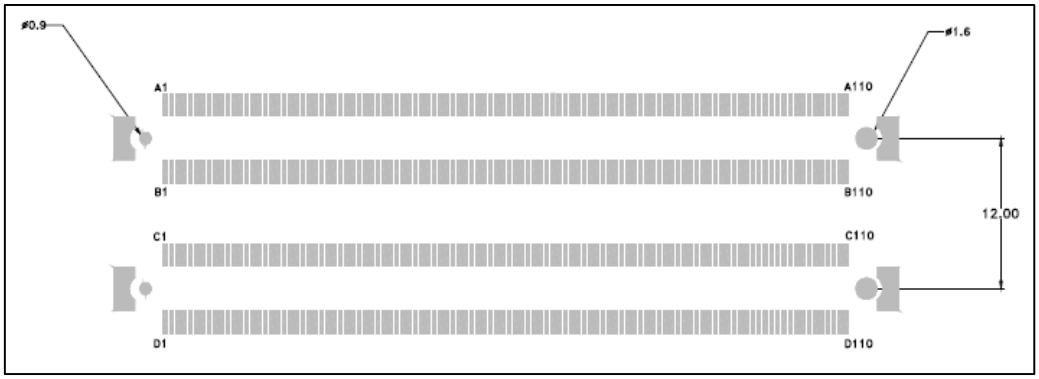


All dimensions in mm.

18.7 Module Connector Pin Numbering

Pin numbering for 440-pin module receptacle shows below. This is a top view of the receptacle, looking into the receptacle, as mounted on the backside of the module.

Figure 18-6 Module Connector Pin Numbering

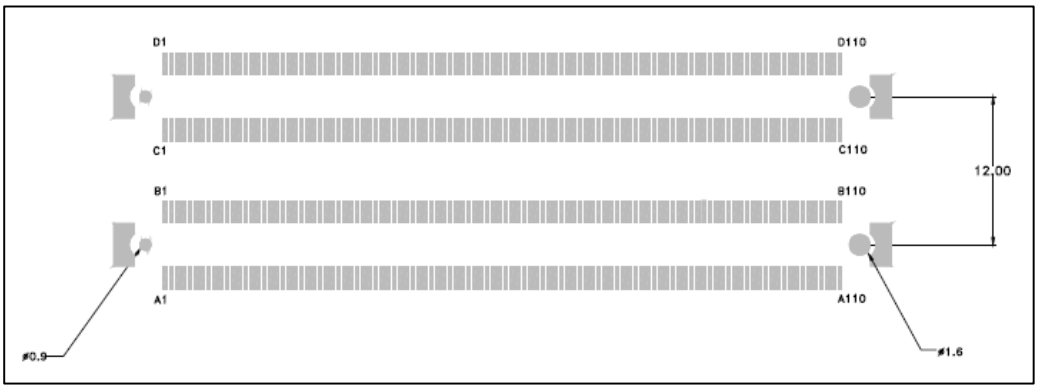


All dimensions in mm.

18.8 Baseboard Connector Pin Numbering

Pin numbering for 440-pin baseboard plug shows below. This is a top view, looking into the plug as mounted on the Baseboard.

Figure 18-7 Baseboard Connector Pin Numbering



All dimensions in mm.

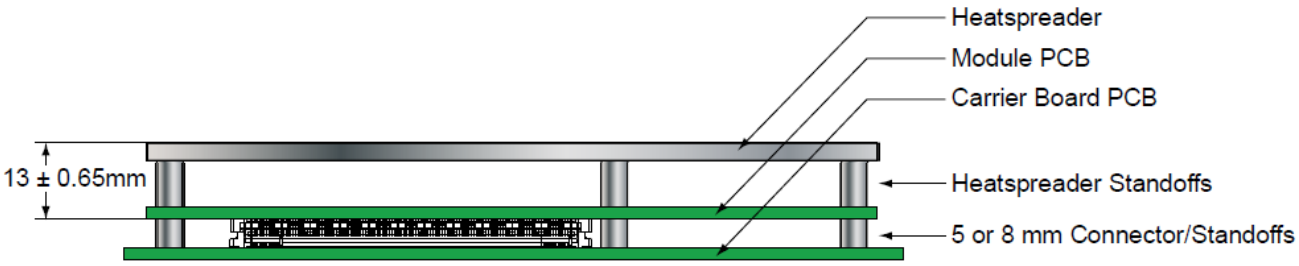
18.9 Heat-Spreader

Modules should be equipped with a heat-spreader. This heat-spreader by it self does not constitute the complete thermal solution for a module but provides a common interface between modules and implementation-specific thermal solutions.

The standoffs shown in Figure 18-8 should be mounted on the Baseboard. The height of the standoff is dependent on the stack height of the Baseboard connector (5mm or 8mm).

The overall module height from the bottom surface of the module board to the heat-spreader top surface shall be 13 mm. The module PCB and heat-spreader plate thickness are vendor implementation specific, however, a 2-mm PCB with a 3-mm heat-spreader may be used which allows use of readily available standoffs.

Figure 18-8 Overall Height for Heat-Spreader in Mini, Compact and Basic Modules



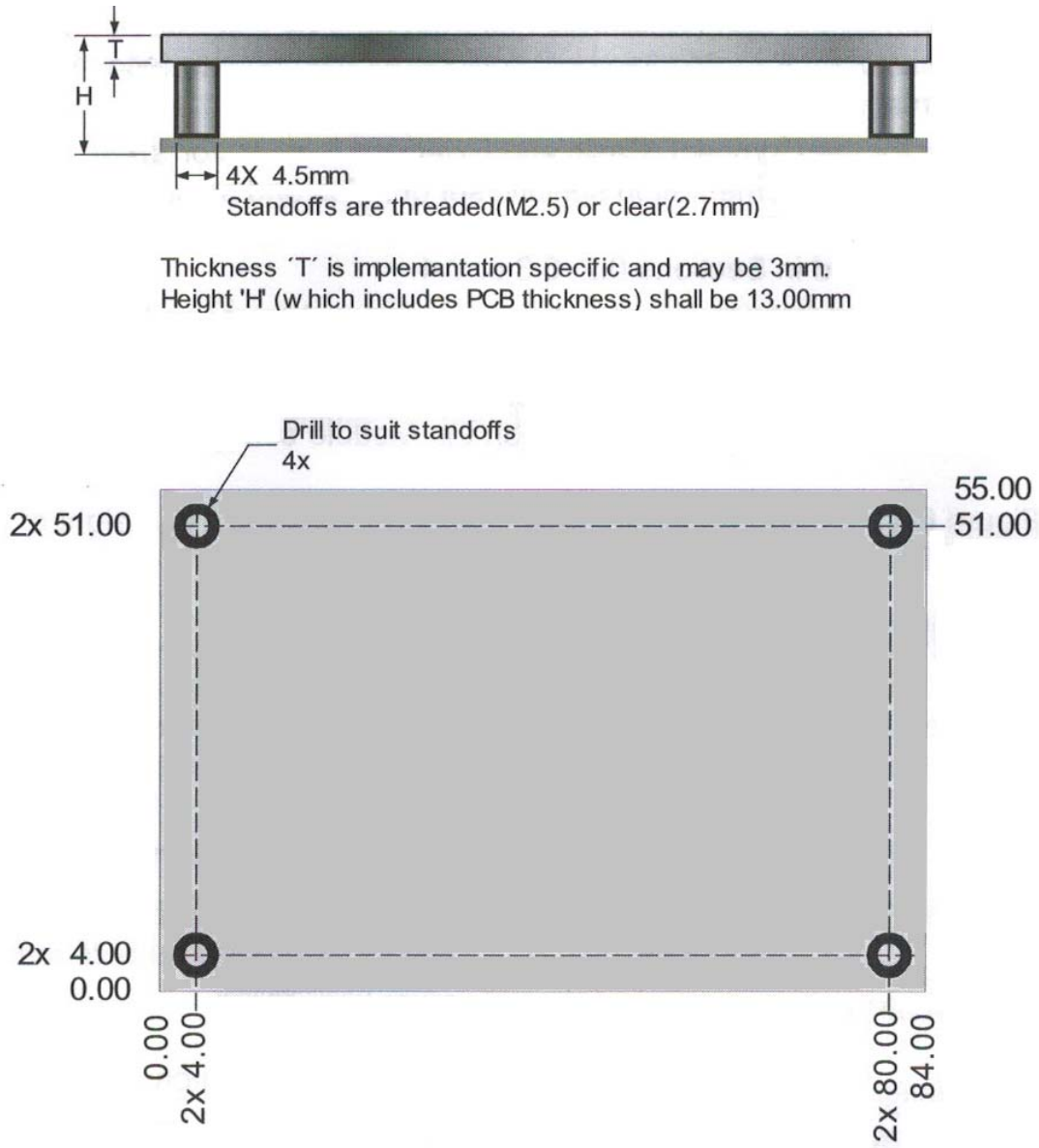
All dimensions in mm.

Tolerances (unless otherwise specified): Z (height) dimensions should be ± 0.8mm [±0.031”] from top of Baseboard to top of heat-spreader. Heat-spreader surface should be flat within 0.2mm [.008"] after assembly. Interface surface finish should have a maximum roughness average (Ra) of 1.6µm [63µin].

The critical dimension in Figure 19-9 is the module PCB bottom side to heat-spreader top side. This dimension shall be 13.00mm ± 0.65mm [±0.026”].

Figure 18-8 shows a cross section of a module and heat-spreader assembled to a Baseboard using the 5mm stack height option. If 8mm Baseboard connectors are used, the overall assembly height increases from 18.00mm to 21.00mm

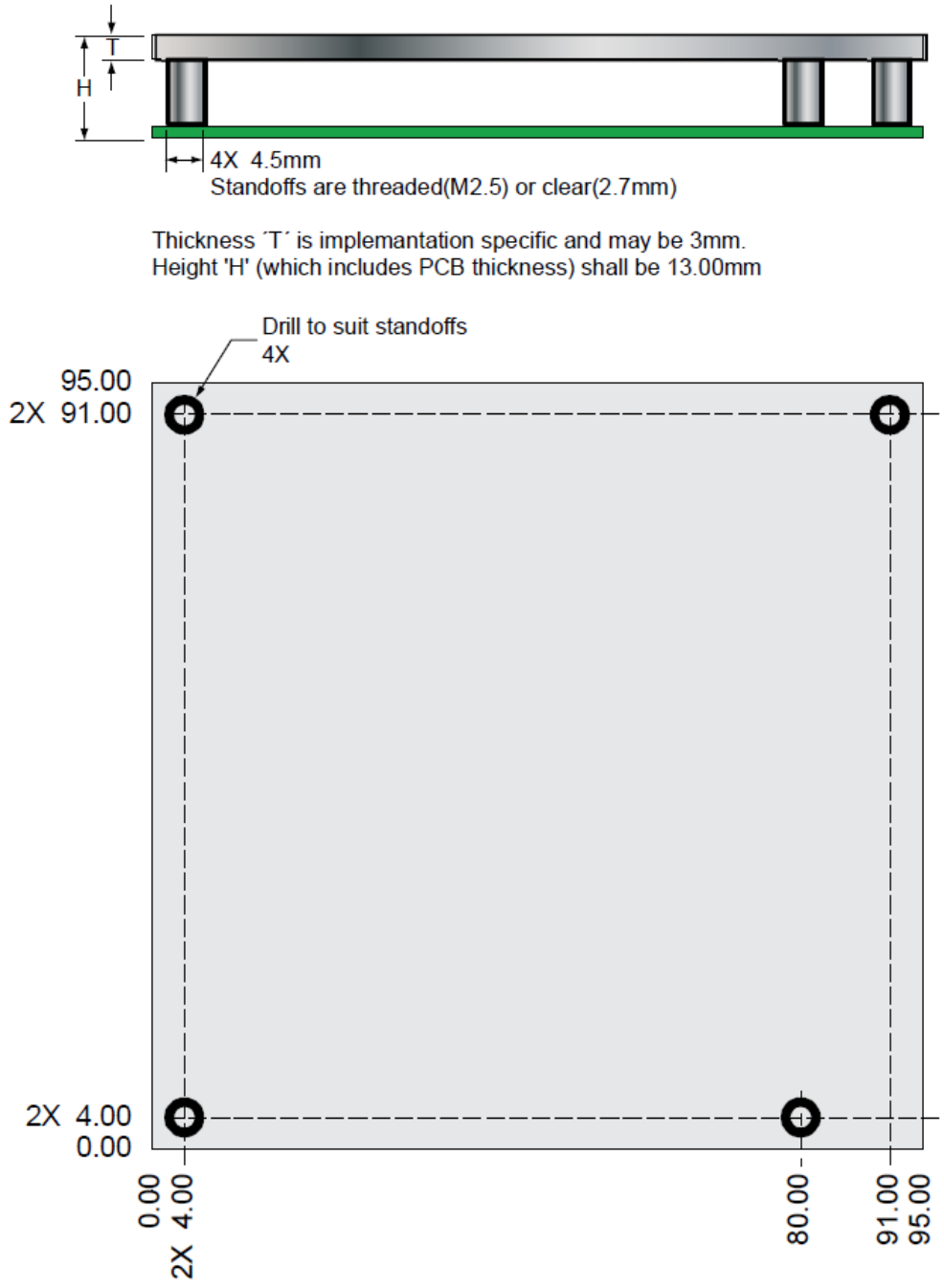
Figure 18-9 Mini Module Heat-Spreader



All dimensions are in mm. X-Y tolerances shall be ± 0.3mm [±0.012"].

If a heat-spreader is supported, it shall provide the attachment points dimensioned in Figure 18-9.

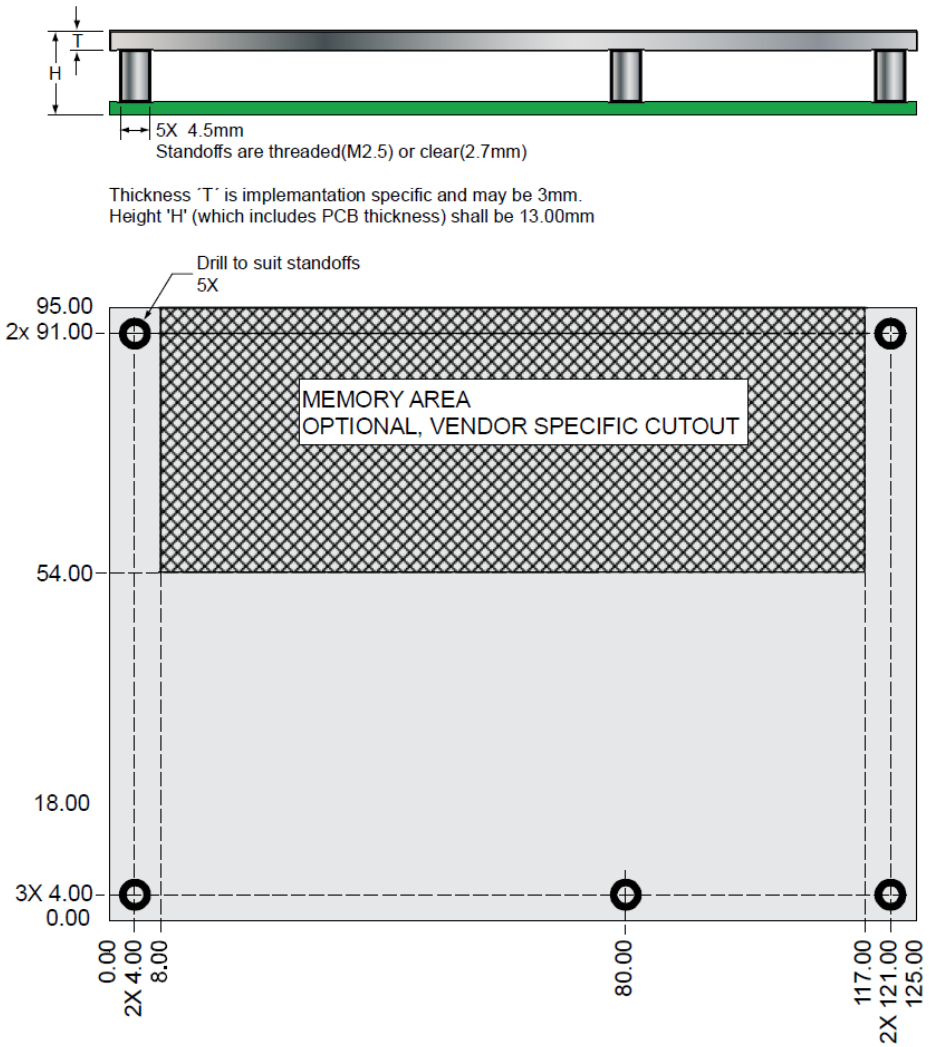
Figure 18-10 Compact Module Heat-Spreader



All dimensions are in mm. X-Y tolerances shall be ± 0.3mm [±0.012"].

If a heat-spreader is supported, it shall provide the attachment points dimensioned in Figure 18-10.

Figure 18-11 Basic Module Heat-Spreader



All dimensions are in mm. X-Y tolerances shall be ± 0.3mm [±0.012"].

If a heat-spreader is supported, it shall provide the attachment points dimensioned in Figure 18-11.

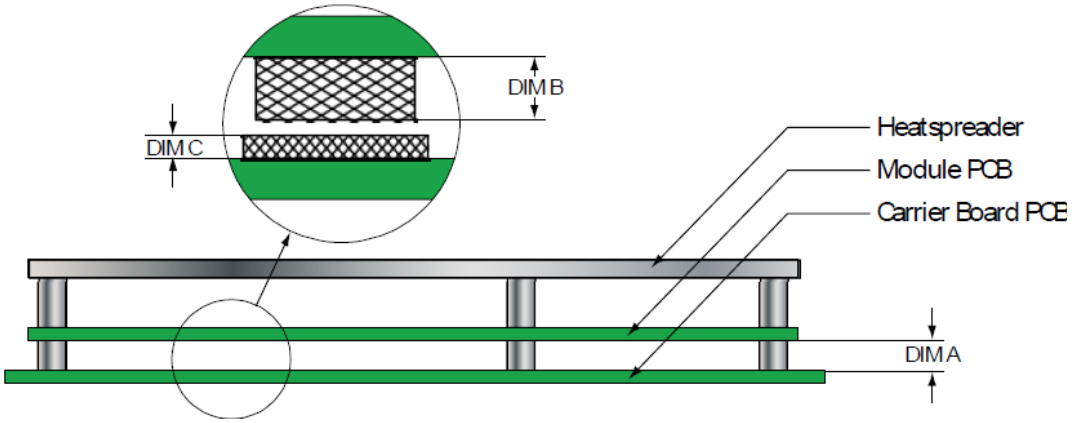
18.10 Component Height — Module Back and Baseboard Top

Parts mounted on the backside of the module (in the space between the bottom surface of the module PCB and the Baseboard) shall have a maximum height of 3.8 mm (dimension 'B' in Figure 18-12).

With the 5 mm stack option, the clearance between the Baseboard and the bottom surface of the module's PCB is 5 mm (dimension 'A' in Figure 18-12). Using the 5 mm stack option, components placed on the Baseboard topside under the module envelope shall be limited to a maximum height of 1 mm (dimension 'C' in Figure 18-12), with the exception of the mating connectors. Using Baseboard topside components up to 1mm allows a gap of 0.2 mm between Baseboard module bottom side components. This may not be sufficient in some situations. In Baseboard applications in which vibration or board flex is a concern, then the Baseboard component height should be restricted to a value less than 1mm that yields a clearance that is sufficient for the application.

If the Baseboard uses the 8 mm stack option (dimension 'A' in Figure 18-12), then the Baseboard topside components within the module envelope shall be limited to a height of 4 mm (dimension 'C' in Figure 18-12), with the exception of the mating connectors. Using Baseboard topside components up to 4mm allows a gap of 0.2 mm between Baseboard topside components and module bottom side components. This may not be sufficient in some situations. In Baseboard applications in which vibration or board flex is a concern, then the Baseboard component height should be restricted to a value less than 4 mm that yields a clearance that is sufficient for the application.

Figure 18-12 Component Clearances Underneath Module



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Chapter 19

19. Appendix A – PCIe Lane Overview

The fundamental PCI Express (PCIe) Link consists of two low-voltage differentially driven pairs of signals such as a transmit pair and a receive pair that are configured as a point to point interconnect between two devices. Clocking information is embedded into the data stream using 8b/10b encoding. The characteristic impedance of the Link is 85Ω differential (nominal), while single-ended DC common mode impedance is 50Ω.

The 10-bit symbol transmission encoding scheme achieves equal number of 1s and 0s over time, which results in DC-balanced transmission and eliminates the 2.5GHz clock signal over the Link. Expanding the 8-bit character into 10-bit symbols degrades transmission performance by 20% but achieves reliable Link operation.

The specified Link speed is 2.5Gtransfers/sec/direction, which results in 250MB/sec/direction raw data throughput that is based on 10-bit symbols incorporating 8-bit data. See Figure 23-1 below.

PCIe Links consist of a varying number of Lanes(x1, x2, x4, x8, x16 and x32) where each numeral represents the number of Lanes resulting in 1, 2, 4, 8, 16 and 32 transmit and receive interfaces per device supporting throughputs of 250, 500, 1000, 2000, 4000 and 8000 MB/sec/direction respectively.

When a Link has more than 1 Lane, Byte Striping is implemented. Each consecutive outbound character in a character stream is multiplexed onto consecutive Lanes.

The PCI Express™ Specification requires polarity inversion to be supported independently by all receivers across the link. The lane performs polarity inversion during initial training sequence if the receiver detects polarity discrepancies. The lane will function correctly even if a positive (TX+) signal from a transmitter is connected to the negative (RX-) signal of a receiver.

Lane Reversal involves reversing the mapping of lanes in an x2 or greater link. The typical interconnect for example in an x4 link is TX0, TX1, and TX2, TX3 connected to RX0, RX1, RX2, and RX3 respectively. In a link that supports lane reversal, mapping can be reversed such that TX0, TX1, TX2, TX3 is connected to RX3, RX2, RX1, RX0 respectively and mapped to RX0, RX1, RX2, RX3 respectively under the control of a hardware signal typically activated via a strapping option. The Lane Reversal feature is an optional feature of the PCI Express™ Specification.

Polarity Inversion or Lane Reversal does not imply direction inversion or reversal. The TX differential pair from an upstream device must still connect to the RX differential pair on the downstream device.

Each device in a link can support multiple lane widths. The two devices negotiate a width that both devices can support during the link-training phase. The PCI Express™ Specification requires that all devices be capable of forming an x1 link as well as their maximum link size.

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Chapter 20

20. Appendix B – Applicable Documents and Standard

The following publications are used in conjunction with this manual. When any of the referenced specifications are superseded by an approved revision, that revision shall apply. All documents may be obtained from their respective organizations.

- Advanced Configuration and Power Interface Specification Revision 4.0, June 16, 2009 Copyright c 1996-2003 Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, Phoenix Technologies Ltd., Toshiba Corporation. All rights reserved.

  http://www.acpi.info/

- ANSI/TIA/EIA-644-A-2001: Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, January 1, 2001. http://www.ansi.org/

- ANSI INCITS 361-2002: AT Attachment with Packet Interface - 6 (ATA/ATAPI-6), November 1, 2002. http://www.ansi.org/

- ANSI INCITS 376-2003: American National Standard for Information Technology – Serial Attached SCSI (SAS), October 30, 2003. http://www.ansi.org/

- Audio Codec '97 Revision 2.3 Revision 1.0, April 2002 Copyright c 2002 Intel Corporation. All rights reserved.

  download.intel.com/support/motherboards/desktop/sb/ac97_r23.pdf

- Display Data Channel Command Interface (DDC/CI) Standard (formerly DDC2Bi) Version 1, August 14, 1998 Copyright c 1998 Video Electronics Standards Association. All rights reserved. http://www.vesa.org

- HDA - High Definition Audio Specification, Revision 1.0, April 15, 2004 Copyright c 2002 Intel Corporation. All rights reserved. http://www.intel.com/standards/hdaudio/

- IEEE 802.3-2005, IEEE Standard for Information technology, Telecommunications and information exchange between systems-Local and metropolitan area networks-Specific requirements – Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications." http://www.ieee.org

- IEEE 802.3ae (Amendment to IEEE 802.3-2005), Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications, Amendment: Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10 Gb/s Operation. http://www.ieee.org
- Intel Low Pin Count (LPC) Interface Specification Revision 1.1, August 2002 Copyright c 2002 Intel Corporation. All rights reserved. http://developer.intel.com/design/chipsets/industry/lpc.htm
- PCI Express Base Specification Revision 2.0, December 20, 2006, Copyright c 2002-2006 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI Express Card Electromechanical Specification Revision 2.0, April 11, 2007, Copyright c 2002-2007 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PICMGR Policies and Procedures for Specification Development, Revision 2.0, September 14, 2004, PCI Industrial Computer Manufacturers Group (PICMGR), 401 Edgewater Place, Suite 500, Wakefield, MA 01880 USA, Tel: 781.224.1100, Fax: 781.224.1239. http://www.picmg.org/
- PICMGR EAPI - Embedded Application Software Interface Specification, Revision 1.0, 2009, PCI Industrial Computer Manufacturers Group (PICMGR), 401 Edgewater Place, Suite 500, Wakefield, MA 01880 USA, Tel: 781.224.1100, Fax: 781.224.1239. http://www.picmg.org/

- SSerial ATA: High Speed Serialized AT Attachment Revision 1.0a January 7, 2003 Copyright c 2000-2003, APT Technologies, Inc., Dell Computer Corporation, Intel Corporation, Maxtor Corporation, Seagate Technology LLC. All rights reserved. http://www.sata-io.org/
- Smart Battery Data Specification Revision 1.1, December 11, 1998. www.sbs-forum.org
- System Management Bus (SMBus) Specification Version 2.0, August 3, 2000 Copyright c 1994, 1995, 1998, 2000 Duracell, Inc., Energizer Power Systems, Inc., Fujitsu, Ltd., Intel Corporation, Linear Technology Inc., Maxim Integrated Products, Mitsubishi Electric Semiconductor Company, PowerSmart, Inc., Toshiba Battery Co. Ltd., Unitrode Corporation, USAR Systems, Inc. All rights reserved. http://www.smbus.org/
- USB 3.0 Specification, Revision 1.0, November 12, 2008, 2000 Copyright c 2007-2008 Hewlett-Packard Company, Intel Corporation, , Microsoft Corporation, NEC Corporation, ST-NXP Wireless and Texas Instruments. All rights reserved. http://www.usb.org/
- SPI, Serial Peripheral Interface Bus. http://elm-chan.org/docs/spi_e.html
- Trusted Platform Module (TPM), Trusted Computing Group Specification 1.2 Revision 103, July 9, 2007, http://www.trustedcomputinggroup.org
- DisplayPort Standard Version 1.1 http://w ww.vesa.org
- High-Definition Multimedia Interface specification version 1.3 http://www.hdmi.org

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Chapter 21

21. Appendix C – Reference Materials

General PC Architecture

- Building the Power-Efficient PC: A Developer's Guide to ACPI Power Management, First Edition, Jerzy Kolinski, Ram Chary, Andrew Henroid, and Barry Press, Intel Press, 2002, ISBN 0-9702846-8-3
- Hardware Bible, Winn L. Rosch, SAMS, 1997, 0-672-30954-8
- The Indispensable PC Hardware Book, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0- 201-62424-9
- The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, Sixth Edition, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1
- PC Hardware in a Nutshell, 3rd Edition, Robert Bruce Thompson and Barbara Fritchman Thompson, O'Reilly, 2003, ISBN 0-596-00513-X

PCIe

- PCI Express Electrical Interconnect Design: Practical Solutions for Board-level Integration and Validation, First Edition, Dave Coleman, Scott Gardiner, Mohamad Kolberhdari, and Stephen Peters, Intel Press, 2005, ISBN 0-9743649-9-1

- Introduction to PCI Express: A Hardware and Software Developer's Guide, First Edition, Adam Wilen, Justin Schade, and Ron Thornburg, Intel Press, 2003, ISBN 0-9702846-9-1

Serial ATA

- Serial ATA Storage Architecture and Applications, First Edition, Knut Grimsrud and Hubbert Smith, Intel Press, 2003, ISBN 0-9717861-8-6

USB

- USB Design by Example, A Practical Guide to Building I/O Devices, Second Edition, John Hyde, Intel Press, ISBN 0-9702846-5-9
- Universal Serial Bus System Architecture, Second Edition, Don Anderson and Dave Dzatko, Mindshare, Inc., ISBN 0-201-30975-0

RS-232 Serial

- RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3

PCB Layout and Signal Integrity

- Printed Circuits Handbook, Fourth Edition, Clyde F. Coombs, Jr., McGraw-Hill, 1996, ISBN 0—07-012754-9
- High Speed Signal Propagation, First Edition, Howard Johnson and Martin Graham, Prentice Hall, 2003, ISBN 0-13-084408-X
- High Speed Digital Design: A Handbook of Black Magic, First Edition, Howard Johnson, Prentice Hall, ISBN: 0133957241

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