PICMG® COM.0

COM Express® Module Base Specification

Revision 2.1
May 14, 2012

Open Modular Computing Specifications

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Revision History

Revision	Date	Action
1.0	July 10, 2005	Revision 1.0
2.0	August 8, 2010	See overview in Section 1.2 'COM.0R2.0 Changes from R1.0' on page 3
2.1	May 14, 2012	See overview in Section 1.4 'COM.0 R2.1 Changes from R2.0' on page 6

1 Introduction

A Computer-On-Module, or COM, is a Module with all components necessary for a bootable host computer, packaged as a super component. A COM requires a Carrier Board to bring out I/O and to power up. COMs are used to build single board computer solutions and offer OEMs fast time-to-market with reduced development cost. Like integrated circuits, they provide OEMs with significant freedom in meeting form-fit-function requirements. For all these reasons the COM methodology has gained much popularity with OEMs in the embedded industry.

COM Express® is an open industry standard for Computer-On-Modules. It is designed to be future proof and to provide a smooth transition path from legacy parallel interfaces to LVDS (Low Voltage Differential Signaling) interfaces. These include the PCI bus and parallel ATA on the one hand and PCI Express and Serial ATA on the other hand.

Key features include:

- Rich complement of contemporary high bandwidth serial interfaces, including PCI Express, Serial ATA, USB, and Gigabit Ethernet
- 32-bit PCI, LPC and Parallel ATA options preserved for easy interface to a range of peripherals
- Extended power-management capabilities
- Robust thermal and mechanical concept
- Cost-effective design
- Legacy-free design (no Super I/O, PS2 keyboard or mouse)
- Small Module size with multiple footprint options to satisfy a range of performance requirements
- High-performance mezzanine connector with several pin-out types to satisfy a range of applications
- Extensive video port support, including VGA, LVDS, SDVO, DP, eDP,DVI and HDMI terminal drivers plus x16 PEG port to Carrier Board graphics controller

The COM Express® specification has been created to appeal to a range of vertical embedded markets. It has also been formulated to be applicable to a broad range of form factors, from floor-installed to bench-top to handheld. Markets and applications include but are not limited to:

- Healthcare - clinical diagnostic imaging systems, patient bedside monitors, etc.
- Retail & advertising - electronic shopping carts, billboards, kiosks, POS systems, etc.
- Test & measurement - scientific and industrial test and measurement instruments
- Gaming & entertainment - simulators, slot machines, etc.
- Industrial automation - industrial robots, vision systems, etc.
- Security - digital CCTV, luggage scanners, intrusion detectors, etc.
- Defense & government - unmanned vehicles, rugged laptops, wearable computers, etc.

Systems based on the COM Express® Specification require the implementation of an application-specific Carrier Board that accepts the Module. User-specific features such as external connector choices and locations and peripheral circuits can be tailored to suit the application. The OEM can focus on application-specific features rather than CPU board design. The OEM also benefits from a wide choice of Modules providing a scalable range of price and performance upgrade options.

1.1 Objective

This specification defines COM Express® Modules at a level of detail sufficient to allow interoperability between independent vendors' Modules and Carrier Boards.

1.2 COM.0R2.0 Changes from R1.0

Type 6

Added definition of a Type 6 pin-out. This pin-out is based on Type 2 with the following changes:

- The PCI interface has been removed and the pins are now used to support the Digital Display Interfaces and additional PCI Express lanes
- The IDE interface has been removed and the pins are now used to support the additional SuperSpeed differential pairs for four USB 3.0 ports
- Three dedicated Digital Display Interfaces have been added (Port 1, Port 2, Port 3). Ports 1, 2, and 3 can be individually configured for DisplayPort, HDMI, or DVI. Port 1 can also be configured for SDVO.
- Added two optional 2 wire serial ports
- SDVO is no longer multiplexed on the PEG port. The SDVO interface is now multiplexed on Digital Display Interface 1
- The PEG interface optionally supports multiplexed display interfaces. Definition of this multiplexing is outside the scope of this specification.
- Added two additional PCI Express lanes (Lane 6 and Lane 7)
- Added support for the physical presence signal for a TPM option, and a lid switch
- Added support for fan tach input and PWM output.
- Removed support for Carrier Board keyboard/mouse controller

Type 10

Added definition of a Type 10 pin-out. This pin-out is based on Type 1 but it is not fully backwards compatible with existing Types. Changes:

- Reduction to single channel LVDS only.
- Added Digital Display Interface, realized as SDVO, DP, or TMDS.
- Added two optional 2 wire serial ports.
- Added support for the physical presence signal for a TPM option, and a lid switch.
- Added support for fan tach input and PWM output.
- Reduction to 4 PCIe x1 links.
- Reduction to 2 SATA interfaces.
- No analog VGA.
- Removed support for Carrier Board keyboard/mouse controller.

All Types

Additional changes to all Module Types

- Added SPI using previously reserved pins on the A-B connector. SPI is the primary interface for Carrier mounted BIOS flash. External BIOS support over SPI is mandatory in R2.0 for all Module Types. In R1.0 the LPC interface was used for external BIOS support. R2.0 Modules must support SPI and might also support LPC external BIOS.
- Added PCI Express Gen2 signaling for all PCI Express lanes.
- AC97 pins are now used to support AC97 and HD audio.
- TV out pins have been redefined. The TV out function is not supported.
- Added the definition for a 95 x 95 mm Module called a Compact Module.
- Added optional support for SDIO using the existing GPIO signals.
- Added multi-master support for the I2C bus.
- Added TYPE10# pin in reclaimed VCC_12V pool to allow detection of Rev 2.0 compliant Module types
- Added a Section “Signals Requiring Module Termination” to further clarify signal terminations
- Incorporated COM.0R1.0 Errata-002
- Incorporated change requests from the Carrier Design Guide subcommittee as well as those submitted during the development of this document.
- Moved I2C to standby power rail to allow interrogation of a Carrier based EEPROM for Module configuration strappings
- Reduced maximum input power for Types 2-5 to 137W and to 68W for Type 1
- Allow optional USB client support on COM.0 USB7

1.3 COM.0 Revision 1.0 vs. 2.0 Compatibility Considerations

For designers wishing to build either Modules compatible with both Revision 1.0 and 2.0 Carriers, or Carriers compatible with both Revision 1.0 and 2.0 Modules, attention is called to the following COM Express® Revision 2.0 compatibility considerations. Even if new Revision 2.0 designs are not intended to support Revision 1.0 counterparts, the 12V pin reclamation consideration is important to protect against pairing with an incompatible Revision 1.0 counterpart.

AC97 / HDA

The original Revision 1.0 AC97 interface on all types has been updated to support High Definition Audio. Refer to Section 4.3.1 'AC97 Audio / High Definition Audio' for further details.

Carrier based BIOS devices

In COM Express® Revision 1.0, Carrier Boards wishing to support an on-Carrier BIOS enabled via the BIOS_DISABLE# pin typically implemented a Firmware Hub via the Module LPC interface. With the progression in technology, the Firmware Hub is less commonly available and COM Express® Revision 2.0 adds support for on Carrier BIOS via the new SPI interface. Refer to Section 4.3.12 'SPI Interface' for further details.

SDVO

To support advances in technology, the SDVO interface, which was formerly multiplexed on the PEG port in Types 2-5, is now de-multiplexed from PEG and supported via a digital display interface in the new Revision 2.0 Types 6 and 10. Refer to Sections 4.3.6 'PEG PCI Express Lanes', 4.3.14 'Multiplexed SDVO', 4.3.15 'Digital Display Interfaces (DDI) - Module Type 6 and 10' and 4.3.17 'DDI Signals: SDVO' for further details.

TV Out

The TV Out interface has been removed and reused on Types 1-5 within COM Express® Revision 2.0

12V Pin Reclamation

COM Express® R2.0 Types 6 and 10 reclaimed several 12V pins for new functions while Revision 2.0 reserved these former 12V pins for Types 1-5. A well designed Revision 2.0 Module needs to be tolerant of 12V on these pins if it is installed on a Revision 1.0 Carrier. Similarly, a Revision 2.0 Carrier needs to be tolerant of 12V on these pins if a Revision 1.0 Module is installed on the Carrier. Refer to Section 5.10 'Protecting COM.0 Pins Reclaimed From the VCC_12V Pool' for further details.

1.4 COM.0 R2.1 Changes from R2.0

Mini form factor

Added definitions for Mini 84x55mm form factor
Section 6.1 'Module Size – Mini Module'

Section 6.10 'Heat-Spreader'

Section Figure 6-11: Mini Module Heat-Spreader'

Section 9.1 'Mounting positions and connector location for Carrier Boards'

I/Os

Added CAN Bus for Type 6 and Type 10 in Section 4.3.30 'CAN Bus'

Added USB 3.0 for Type 10

Added a pin for USB Client Host detection for Type 10

Added option for eDP overlayed on LVDS Channel A for Type 6 and Type 10 Modules

Power

Allowed for wide input voltage range for Mini size Module

Updates

Updated Section 4.5 'Signals Requiring Module Termination'

Corrected SDIO Section 4.3.26 'SDIO', Table 4.31 'SD card interface signals' and Table 4.32 'SDIO Signals, Pin Types, and Descriptions'

Clarify SYS_RESET# and PWR_OK usage

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1.6.1 Necessary Claims (referring to mandatory or recommended features)

Tyco Electronics has the following patents, which may cover some aspects of the PICMG® COM Express® Module and Carrier Board Connector as detailed in Section 6. Contact Tyco Electronics for further information.

- USA patent 6,095,832 “Cap housing for electrical connectors”
- USA patent 6,159,021 “Electrical connector for printed circuit boards”
- USA patent 6,558,195 “Electrical connector for printed circuit boards”
- Japan patent 11-040243 “ELECTRICAL CONNECTOR CAP AND ELECTRICAL CONNECTOR ASSEMBLY”
- Japan patent 11-074027 “BOARD-MOUNTING TYPE CONNECTOR”
- Japan patent 11-260464 “CAP ON ELECTRIC CONNECTOR”
- Japan patent 11-354227 “BASE BOARD INSTALLING TYPE CONNECTOR ASSEMBLY”
- Japan patent 2000-003751 “SUBSTRATE MOUNTING TYPE CONNECTOR ASSEMBLY”
- Japan patent 2000-048876 “ELECTRICAL CONNECTOR FOR CONNECTING MUTUAL BOARDS”

Foxconn Electronics (Hon Hai Precision) has the following patents, which may cover some aspects of the PICMG® COM Express® Module and Carrier Board Connector as detailed in Section 6. Contact Foxconn Electronics for further information.

- USA patent 7,578,701 “Electrical connector for PCB”
- China patent 200720131412.4 “Electrical Connector for PCB”
- Taiwan patent M339102 “Electrical Connector for PCB”

1.6.2 Unnecessary Claims (referring to optional features or non-normative elements)

No disclosures in this category were made during subcommittee review.

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1.8 Special Word Usage

Mandatory features are indicated by the use of the word “***shall***.”

Recommended features are indicated by the use of the word “***should***.”

Optional features are indicated by the use of the word “***may***.”

1.9 Acronyms / Definitions

Table 1.1: Terms and Definitions

Term	Definition
AC '97	Audio CODEC (Coder-Decoder)
ACPI	Advanced Configuration Power Interface – standard to implement power saving modes in PC-AT systems
Basic Module	COM Express® 125mm x 95mm Module form factor.
BIOS	Basic Input Output System – firmware in PC-AT system that is used to initialize system components before handing control over to the operating system.
CAN	Controller-area network (CAN or CAN-bus) is a vehicle bus standard designed to allow microcontrollers to communicate with each other within a vehicle without a host computer.
Carrier Board	An application specific circuit board that accepts a COM Express® Module.
CCTV	Closed Circuit Television
CVBS	Composite Video Baseband Signal
Compact Module	COM Express® 95x95 Module form factor
DDC	Display Data Control – VESA (Video Electronics Standards Association) standard to allow identification of the capabilities of a VGA monitor
DDI	Digital Display Interface – containing DisplayPort, HDMI/DVI and SDVO
DIMM	Dual In-line Memory Module
DisplayPort	DisplayPort is a digital display interface standard put forth by the Video Electronics Standards Association (VESA). It defines a new license free, royalty free, digital audio/video interconnect, intended to be used primarily between a computer and its display monitor.
DRAM	Dynamic Random Access Memory
DVI	Digital Visual Interface - a Digital Display Working Group (DDWG) standard that defines a standard video interface supporting both digital and analog video signals. The digital signals use TMDS.
EAPI	Embedded Application Programming Interface Software interface for COM Express® specific industrial functions • System information • Watchdog timer • I2C Bus • Flat Panel brightness control • User storage area • GPIO
EEPROM	Electrically Erasable Programmable Read-Only Memory
Embedded DisplayPort	Embedded Display Port (eDP) is a digital display interface standard produced by the Video Electronics Standards Association (VESA) for digital interconnect of Audio and Video.
Extended Module	COM Express® 155mm x 110mm Module form factor.
FR4	A type of fiber-glass laminate commonly used for printed circuit boards.
Gb	Gigabit
GBE	Gigabit Ethernet
GPI	General Purpose Input
GPIO	General Purpose Input Output
GPO	General Purpose Output
HDA	Intel High Definition Audio (HD Audio) refers to the specification released by Intel in 2004 for delivering high definition audio that is capable of playing back more channels at higher quality than AC97.
HDMI	High Definition Multimedia Interface
I2C	Inter Integrated Circuit – 2 wire (clock and data) signaling scheme allowing communication between integrated circuits, primarily used to read and load register values.
IDE	Integrated Device Electronics – parallel interface for hard disk drives – also known as PATA
Legacy Device	Relics from the PC-AT computer that are not in use in contemporary PC systems: primarily the ISA bus, UART-based serial ports, parallel printer ports, PS-2 keyboards, and mice. Definitions vary as to what constitutes a legacy device. Some definitions include IDE as a legacy device.
LAN	Local Area Network
LPC	Low Pin-Count Interface: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy-device support into a single IC.
LS	Least Significant
LVDS	Low Voltage Differential Signaling – widely used as a physical interface for TFT flat panels. LVDS can be used for many high-speed signaling applications. In this document, it refers only to TFT flat-panel applications.

Term	Definition
ME	Management Engine
Mini Module	COM Express® 84x55mm Module form factor
MS	Most Significant
NA	Not Available
NC	No Connect
NTSC	National Television Standards Committee – video broadcast standard used in North America
OEM	Original Equipment Manufacturer
PAL	Phase Alternating Line – video broadcast standard used in many European countries.
PATA	Parallel AT Attachment – parallel interface standard for hard-disk drives – also known as IDE, AT Attachment, and as ATA
PC-AT	"Personal Computer – Advanced Technology" – an IBM trademark term used to refer to Intel x86 based personal computers in the 1990s
PCB	Printed Circuit Board
PCI	Peripheral Component Interface
PCI Express **PCIE**	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
PEG	PCI Express Graphics
PHY	Ethernet controller physical layer device
Pin-out Type	A reference to one of seven COM Express® definitions for the signals that appear on the COM Express® Module connector pins.
PS2 **PS2 Keyboard** **PS2 Mouse**	"Personal System 2" - an IBM trademark term used to refer to Intel x86 based personal computers in the 1990s. The term survives as a reference to the style of mouse and keyboard interface that were introduced with the PS2 system.
R_a	Roughness Average – a measure of surface roughness, expressed in units of length.
ROM	Read Only Memory – a legacy term – often the device referred to as a ROM can actually be written to, in a special mode. Such writable ROMs are sometimes called Flash ROMs. BIOS is stored in ROM or Flash ROM.
RTC	Real Time Clock – battery backed circuit in PC-AT systems that keeps system time and date as well as certain system setup parameters
SAS	Serial Attached SCSI – high speed serial version of SCSI
SCSI	Small Computer System Interface – an interface standard for high end disk drives and other computer peripherals
SPD	Serial Presence Detect – refers to serial EEPROM on DRAMs that has DRAM Module configuration information
SPI	Serial Peripheral Interface
SO-DIMM	Small Outline Dual In-line Memory Module
S0, S1, S2, S3, S4, S5	System states describing the power and activity level S0 Full power, all devices powered S1 S2 S3 Suspend to RAM System context stored in RAM; RAM is in standby S4 Suspend to Disk System context stored on disk S5 Soft Off Main power rail off, only standby power rail present
SATA	Serial AT Attachment: serial-interface standard for hard disks
SDVO	Serialized Digital Video Output – Intel defined format for digital video output that can be used with Carrier Board conversion ICs to create parallel, TMDS, and LVDS flat-panel formats as well as NTSC and PAL TV outputs
SM Bus	System Management Bus
Super I/O	An integrated circuit, typically interfaced via the LPC bus that provides legacy PC I/O functions including PS2 keyboard and mouse ports, serial and parallel port(s) and a floppy interface.
TFT	Thin Film Transistor – refers to technology used in active matrix flat-panel displays, in which there is one thin film transistor per display pixel.
TMDS	Transition Minimized Differential Signaling - a digital signaling protocol between the graphics subsystem and display. TMDS is used for the DVI digital signals.
TPM	Trusted Platform Module, chip to enhance the security features of a computer system.
USB	Universal Serial Bus
VGA	Video Graphics Adapter – PC-AT graphics adapter standard defined by IBM.
WDT	Watch Dog Timer.
XAUI	10 Gigabit / sec Attachment Unit Interface.

1.10 Applicable Documents and Standards

The following publications are used in conjunction with this standard. When any of the referenced specifications are superseded by an approved revision, that revision shall apply. All documents may be obtained from their respective organizations.

- Advanced Configuration and Power Interface Specification Revision 4.0, June 16, 2009 Copyright © 1996-2003 Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, Phoenix Technologies Ltd., Toshiba Corporation. All rights reserved. http://www.acpi.info/
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- Display Data Channel Command Interface (DDC/CI) Standard (formerly DDC2Bi) Version 1, August 14, 1998 Copyright © 1998 Video Electronics Standards Association. All rights reserved. http://www.vesa.org
- ExpressCard® Standard 2.0, June 2009 Copyright © 2009 PCMCIA. All rights reserved. http://www.expresscard.org/
- HDA - High Definition Audio Specification, Revision 1.0, April 15, 2004 Copyright © 2002 Intel Corporation. All rights reserved. http://www.intel.com/standards/hdaudio/
- IEEE 802.3-2005, IEEE Standard for Information technology, Telecommunications and information exchange between systems-Local and metropolitan area networks-Specific requirements – Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications." http://www.ieee.org
- IEEE 802.3ae (Amendment to IEEE 802.3-2005), Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications, Amendment: Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10 Gb/s Operation. http://www.ieee.org
- Intel Low Pin Count (LPC) Interface Specification Revision 1.1, August 2002 Copyright © 2002 Intel Corporation. All rights reserved. http://developer.intel.com/design/chipsets/industry/lpc.htm
- PCI Express Base Specification Revision 2.0, December 20, 2006, Copyright © 2002-2006 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI Express Card Electromechanical Specification Revision 2.0, April 11, 2007, Copyright © 2002-2007 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI Local Bus Specification Revision 3.0, February 3, 2004 Copyright © 1992, 1993, 1995, 1998, and 2004 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/

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  http://www.picmg.org/
- PICMG® EAPI - Embedded Application Software Interface Specification, Revision 1.0, 2010, PCI Industrial Computer Manufacturers Group (PICMG®), 401 Edgewater Place, Suite 500, Wakefield, MA 01880 USA, Tel: 781.224.1100, Fax: 781.224.1239.
  http://www.picmg.org/
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  SD Specifications Part E1 SDIO Specification Version 2.00, February 8, 2007
  Copyright 2007 SD Card Association
  http://www.sdcard.org
- Serial ATA: High Speed Serialized AT Attachment Revision 1.0a January 7, 2003
  Copyright © 2000-2003, APT Technologies, Inc., Dell Computer Corporation, Intel Corporation, Maxtor Corporation, Seagate Technology LLC. All rights reserved.
  http://www.sata-io.org/
- Smart Battery Data Specification Revision 1.1, December 11, 1998.
  www.sbs-forum.org
- System Management Bus (SMBus) Specification Version 2.0, August 3, 2000
  Copyright © 1994, 1995, 1998, 2000 Duracell, Inc., Energizer Power Systems, Inc., Fujitsu, Ltd., Intel Corporation, Linear Technology Inc., Maxim Integrated Products, Mitsubishi Electric Semiconductor Company, PowerSmart, Inc., Toshiba Battery Co. Ltd., Unitrode Corporation, USAR Systems, Inc. All rights reserved.
  http://www.smbus.org/
- USB 3.0 Specification, Revision 1.0, November 12, 2008, 2000
  Copyright © 2007-2008 Hewlett-Packard Company, Intel Corporation, Microsoft Corporation, NEC Corporation, ST-NXP Wireless and Texas Instruments. All rights reserved.
  http://www.usb.org/
- SPI, Serial Peripheral Interface Bushttp://elm-chan.org/docs/spi_e.html
- Trusted Platform Module (TPM), Trusted Computing Group Specification 1.2 Revision 103, July 9, 2007
  http://www.trustedcomputinggroup.org
- DisplayPort Standard Version 1.1
  http://www.vesa.org/
- DisplayPort Interoperability Guideline Version 1.1a dated February 5, 2009
  http://www.vesa.org/Standards/free.htm
- High-Definition Multimedia Interface specification version 1.3
  http://www.hdmi.org

1.11 Statement of Compliance

Statements of compliance with this specification take the form specified in the PICMG® Policies and Procedures for Specification Development:

"This product complies with PICMG® COM.0 Revision 2.1."

Products making this simple claim of compliance must provide, at a minimum, all features defined in this specification as being mandatory by the use of the keyword "***shall***" in the body of the specification. Such products may also provide recommended features associated with the keyword "***should***" and permitted features associated with the keyword "***may***" as well.

Because the specification provides for a number of recommended and permitted features beyond the mandatory minimum set and a wide range of performance capabilities, more complete descriptions of product compliance are encouraged.

2 Module Overview

2.1 Module Configuration

Four Module sizes are defined: the Mini Module, Compact Module, Basic Module and the Extended Module. The primary difference between the different size Modules is the over-all physical size and the performance envelope supported by each. The Extended Module is larger and can support larger processor and memory solutions. The Compact Module, Basic Module and Extended Module use the same connectors and pin-outs whereas the 84x55 Mini Module targets, but is not limited to use the COM Express A-B connector, Type 10 and Type 1 pin-outs. In addition the Mini Module allows for wide range power supply operation. The different size Modules share several common mounting hole positions. This level of compatibility allows that a Carrier Board can be designed to accommodate multiple Module sizes.

Up to 440 pins of connectivity are available between COM Express Modules and the Carrier Board. Legacy buses such as PCI, parallel ATA, LPC, AC'97 can be supported as well as new high speed serial interconnects such as PCI Express, Serial ATA or SAS, USB 2.0 / 3.0 and Gigabit Ethernet. To enhance interoperability between COM Express Modules and Carrier Boards, seven common signaling configurations (Pin-out Types) have been defined to ease system integration. Some Pin-out Types definitions require only a single 220-pin connector and others require both 220-pin connectors to supply all the defined signaling.

2.2 Feature Overview - Size

2.2.1 Mini Module

The Mini Module targets the next generation of mobile applications that require energy saving processors, high-end graphics combined with longer battery life. Key features of the Mini Module include:

- Module size: 84mm x 55mm
- 5mm and 8mm stack height options (Module bottom to Carrier Board top)
- Wide-range power supply input (4.75-20V)
- Suggested pin-out: single 220 pin connector, Type 10
- Reduced Z height for components (optional)

Although not a requirement, Mini Modules are often implemented with memory and SSD storage soldered down on the Module. This facilitates their use in ruggedized, small form factor mobile systems.

2.2.2 Compact Module

The Compact Module is intended for mobile systems and space-constrained stationary systems. Key features of the Compact Module include:

- Module size: 95mm x 95mm
- 5mm and 8mm stack height options (Module bottom to Carrier Board top)
- 18mm 'z' height with heat-spreader (using the 5mm stack option)
- Accommodates a single (or two stacked) horizontal mount SO-DIMM
- Single 220 pin or dual 220 pin connectors for up to 440 pins

2.2.3 Basic Module

The Basic Module is intended for mobile systems and space-constrained stationary systems. Key features of the Basic Module include:

- Module size: 125mm x 95mm
- 5mm and 8mm stack height options (Module bottom to Carrier Board top)
- 18mm 'z' height with heat-spreader (using the 5mm stack option)
- Accommodates a single (or two stacked) horizontal mount SO-DIMM
- Single 220 pin or dual 220 pin connectors for up to 440 pins

2.2.4 Extended Module

The Extended Module, which targets OEM applications that require larger amounts of system memory, features a larger Module size to accommodate full size DIMMs and larger chipset and CPU packages.

The key features of the Extended Module include:

- Module size: 155mm x 110mm
- 5mm and 8mm stack height options (Module bottom to Carrier Board top)
- 18mm 'z' height with heat-spreader (using the 5mm stack option)
- Accommodates 2 full-size DIMM or mini DIMM memories or 2 horizontal mount or vertical mount SO-DIMMs
- Single 220 pin or dual 220 pin connectors for up to 440 pins
- Allows for the use of higher performance CPUs that can not be supported on the Compact Module or Basic Module

2.3 Feature Overview - Pin-out Types

2.3.1 Pin-out Type 1

- Single 220 pin connector (A-B connector)
- Up to 8 USB 2.0 ports; 4 shared over-current lines
- Up to 4 Serial ATA or SAS ports
- Up to 6 PCI Express Gen1/Gen2 signaling lanes
- Support pins for up to 2 ExpressCards
- Dual 24-bit LVDS channels
- Analog VGA
- AC '97 / HDA digital audio interface (external CODEC(s) required)
- Single Ethernet interface with integrated PHY – pinned for Gigabit Ethernet
- LPC interface
- SPI[1]
- 8 GPIO pins
- 68W maximum input power over Module connector pins
- +12V primary power supply input
- +5V standby and 3.3V RTC power supply inputs

2.3.2 Pin-out Type 10

The type 10[2] Pin-out was introduced with COM Express Rev. 2.0.

- Single 220 pin connector (A-B connector)
- Up to 8 USB 2.0 ports; 4 shared over-current lines
- USB 3.0 support
- USB Client support
- Up to 2 Serial ATA or SAS ports
- Up to 4 PCI Express Gen1/Gen2 signaling lanes
- Support pins for up to 2 ExpressCards
- Single 24-bit LVDS channel with option to overlay with eDP
- One Digital Display Interface configurable as SDVO, DP, or TMDS
- AC '97 / HDA digital audio interface (external CODEC(s) required)
- Single Ethernet interface with integrated PHY – pinned for Gigabit Ethernet
- LPC interface
- Two TX/RX serial pairs with option to overlay CAN interface
- Fan control
- TPM support
- 8 GPIO pins
- 68W maximum input power over Module connector pins
- +12V primary power supply input for Compact, Basic and Extended form factor
- Wide input voltage range for Mini form factor
- +5V standby and 3.3V RTC power supply inputs

1 *SPI support starts with COM.0 R2.0*

2 *Pin-out Type 10 is not compatible to Type 1-6*

2.3.3 Pin-out Type 2

All Pin-out Type 1 features plus the following:

- Dual 220 pin connectors (A-B and C-D, 440 pins total)
- 32 bit PCI interface
- IDE port (to support legacy ATA devices such as CD-ROM drives and Compact Flash storage cards)
- Up to 22 PCI Express lanes (up to 6 on A-B and up to 16 on C-D)
- 16 of 22 PCI Express lanes commonly used for PCI Express Graphics
- SDVO option (pins shared with PCI Express Graphics)
- Maximum Module input power capability extended to 137W

2.3.4 Pin-out Type 3

All Pin-out Type 2 features with the exception of the following:

- IDE pins are reallocated to provide additional Gigabit Ethernet capability: no IDE
- Up to 3 Gigabit Ethernet channels

2.3.5 Pin-out Type 4

All Pin-out Type 2 features with the exception of the following:

- PCI pins are reallocated to provide additional PCI Express lanes: no PCI
- Up to 32 PCI Express lanes

2.3.6 Pin-out Type 5

All Pin-out Type 2 features with the exception of the following:

- Both IDE and PCI pins are reallocated: no IDE and no PCI
- Up to 32 PCI Express lanes
- Up to 3 Gigabit Ethernet channels

2.3.7 Pin-out Type 6

All Pin-out Type 2 features with the exception of the following:

- Both IDE and PCI pins are reallocated: no IDE and no PCI
- Up to 24 PCI Express lanes (16 on the PEG port)
- Reserved 16 pins to support the two extra differential pairs required for SuperSpeed USB 3.0. The 16 pins will allow SuperSpeed USB 3.0 support on up to four of the eight USB 2.0 ports. At this point in time, there is not enough information and silicon available for this subcommittee to determine the appropriate trace length and routing rules for SuperSpeed USB 3.0.
- Up to 3 Digital Display Interfaces
- Allow eDP overlay of LVDS Channel A
- Two TX/RX serial pairs with option to overlay CAN interface

3 Required and Optional Features

3.1 Module Pin-out Type Definitions

Seven pin-out types are defined. Pin-out Type 1 and Type 10 Modules have a single 220-pin connector, the A-B connector. Module Pin-out Types 2 through 6 use a pair of 220 pin connectors, designated A-B and C-D, for a total of 440 pins. The variations in Pin-out Type definitions are summarized in the table below.

Table 3.1: Module Pin-out Type Overview

Types	Connector Rows	PCI Express Lanes	PEG/ SDVO	PCI	IDE Ports	SATA Ports	LAN Ports	USB 2.0 / SuperSpeed USB	Display Interfaces
Type 1	A-B	Up to 6	-	-	-	4	1	8 / 0	VGA, LVDS
Type 2	A-B C-D	Up to 22	1/2	32 bit	1	4	1	8 / 0	VGA, LVDS, PEG/SDVO
Type 3	A-B C-D	Up to 22	1/2	32 bit	-	4	3	8 / 0	VGA, LVDS, PEG/SDVO
Type 4	A-B C-D	Up to 32	1/2	-	1	4	1	8 / 0	VGA, LVDS, PEG/SDVO
Type 5	A-B C-D	Up to 32	1/2	-	-	4	3	8 / 0	VGA, LVDS, PEG/SDVO
Type 6	A-B C-D	Up to 24	1/NA	-	-	4	1	8 / 4[3]	VGA, LVDS/eDP,PEG, 3xDDI
Type 10	A-B	Up to 4	-/1	-	-	2	1	8 / 2	LVDS/ eDP,1xDDI

For Module Pin-out Types 2 through 6, a subset of the PCI Express lanes are commonly used as PCI Express Graphics (PEG) lanes. SDVO functions ***may*** be pin-shared with PEG lanes on Types 2-5. In Type 6 SDVO is moved from the PEG to DDI 1. Type 10 does feature one DDI but no PEG lanes.

Type 1 Modules allow for a minimal possible feature set using two of the four available connector rows. Type 1 represents a basic feature set with the benefit of simplified routing of the Carrier Board to allow a lower layer count board.

Type 10 Modules are similar but not completely compatible to Type 1 Modules. These Modules feature less PCI Express and SATA interfaces. Type 10 Modules support a single 24 bit LVDS panel interface, a single DDI and an eDP overlayed on LVDS Channel A and an option to allow a CAN bus to share SER1 pins. 2 of the 8 USB ports can be used as USB 3.0.

Type 2 Modules include PCI and IDE interfaces. These Modules either use on board graphics capabilities or ***may*** use 16 PEG lanes to connect to an external video controller. In case of on board graphics, PEG pins ***may*** be alternatively used for two SDVO ports.

Type 3 Modules trade IDE port pins for two additional LAN ports, allowing up to three GBE interfaces.

Type 4 Modules drop the PCI interface, to allow up to 32 PCI Express lanes for applications with large I/O bandwidth requirements. IDE support is still available.

Type 5 Modules trade IDE and PCI pins for up to 32 PCI Express lanes and up to three GBE interfaces. These Modules are intended for applications with large I/O bandwidth requirements.

Type 6 Modules trade IDE and PCI pins for up to 8 PCI Express lanes, up to three DDIs and 4 of the 8 USB ports can be used as USB 3.0. Type 6 Modules support a single or dual channel 18/24 bit LVDS panel interface, three DDIs and an eDP overlayed on LVDS Channel A and an option to allow a CAN bus to share SER1 pins.

3 *The SuperSpeed USB ports are not in addition to the USB 2.0 ports. Up to 4 of the USB 2.0 ports can support SuperSpeed USB*

3.2 Module Pin-out Types 1-6 & 10 - Required and Optional Features

COM Express Required and Optional features are summarized in the following table. The features identified as Minimum (Min.) ***shall*** be implemented by all Modules. Features identified up to Maximum (Max) ***may*** be additionally implemented by a Module.

Change Key: Green = Generic R2.0 | *Blue = Type 10 only* | Violet = Type 10 & Type 6 only | *Red = Type 6 only*

Table 3.2: Module Pin-out - Required and Optional Features A-B Connector

Connector	Feature	Type 10 (Single connector) Min / Max	Type 1 (Single connector) Min / Max	Type 2 (IDE + PCI) Min / Max	Type 3 (No IDE) Min / Max	Type 4 (No PCI) Min / Max	Type 5 (No IDE, No PCI) Min / Max	Type 6 (No IDE or PCI, add DDI + USB3) Min / Max
A-B	**System I/O**							
A-B	PCI Express Lanes 0 - 5	1 / *4*	1 / 6	1 / 6	1 / 6	1 / 6	1 / 6	1 / 6
A-B	LVDS Channel A	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1
A-B	LVDS Channel B	*NA*	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1
A-B	eDP on LVDS CH A pins	*0 / 1*	NA	NA	NA	NA	NA	0 / 1
A-B	VGA Port	*NA*	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1
A-B	TV-Out	NA	NA	NA	NA	NA	NA	NA
A-B	DDI 0	*0 / 1*	NA	NA	NA	NA	NA	NA
A-B[4]	Serial Ports 1 - 2	0 / 2	NA	NA	NA	NA	NA	0 / 2
A-B	CAN interface on SER1	0 / 1	NA	NA	NA	NA	NA	0 / 1
A-B	SATA / SAS Ports	1 / *2*	1 / 4	1 / 4	1 / 4	1 / 4	1 / 4	1 / 4
A-B	AC'97 / HDA Digital Interface	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1
A-B	USB 2.0 Ports	4 / 8	4 / 8	4 / 8	4 / 8	4 / 8	4 / 8	4 / 8
A-B	USB Client	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1
A-B	USB 3.0 Ports	*0 / 2*	NA	NA	NA	NA	NA	NA
A-B	LAN Port 0	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1
A-B	Express Card Support	0 / 2	1 / 2	1 / 2	1 / 2	1 / 2	1 / 2	1 / 2
A-B	LPC Bus	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1
A-B	SPI	1 / 2	1 / 2	1 / 2	1 / 2	1 / 2	1 / 2	1 / 2
A-B	**System Management**							
A-B[5]	SDIO (muxed on GPIO)	0 / 1	NA	NA	NA	NA	NA	0 / 1
	General Purpose I/O	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8	8 / 8
A-B	SMBus	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1
A-B	I2C	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1
A-B	Watchdog Timer	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1
A-B	Speaker Out	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1
A-B	External BIOS ROM Support	0 / 2	0 / 2	0 / 2	0 / 2	0 / 2	0 / 2	0 / 2
A-B	Reset Functions	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1

4 *Indicates 12V-tolerant features on former VCC_12V signals.*

5 *Cells in the connected columns spanning rows provide a rough approximation of features sharing connector pins.*

Connector	Feature	Type 10 (Single connector) Min / Max	Type 1 (Single connector) Min / Max	Type 2 (IDE + PCI) Min / Max	Type 3 (No IDE) Min / Max	Type 4 (No PCI) Min / Max	Type 5 (No IDE, No PCI) Min / Max	Type 6 (No IDE or PCI, add DDI + USB3) Min / Max
A-B	**Power Management**							
A-B	Thermal Protection	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1
A-B	Battery Low Alarm	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1
A-B	Suspend/Wake Signals	0 / 3	0 / 3	0 / 3	0 / 3	0 / 3	0 / 3	0 / 3
A-B	Power Button Support	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1
A-B	Power Good	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1
A-B	VCC_5V_SBY Contacts	4 / 4	4 / 4	4 / 4	4 / 4	4 / 4	4 / 4	4 / 4
A-B[4]	Sleep Input	0 / 1	NA	NA	NA	NA	NA	0 / 1
A-B[4]	Lid Input	0 / 1	NA	NA	NA	NA	NA	0 / 1
A-B[4]	Fan Control Signals	0 / 2	NA	NA	NA	NA	NA	0 / 2
A-B	Trusted Platform Modules	0 / 1	NA	NA	NA	NA	NA	0 / 1
A-B	**Power**							
A-B	VCC_12V Contacts	12 / 12	12 / 12	12 / 12	12 / 12	12 / 12	12 / 12	12 / 12

Table 3.3: Module Pin-out - Required and Optional Features C-D Connector

Connector	Feature	Type 10 (Single connector) Min / Max	Type 1 (Single connector) Min / Max	Type 2 (IDE + PCI) Min / Max	Type 3 (No IDE) Min / Max	Type 4 (No PCI) Min / Max	Type 5 (No IDE, No PCI) Min / Max	Type 6 (No IDE or PCI, add DDI + USB3) Min / Max
C-D	**System I/O**							
C-D[5]	PCI Express Lanes 16 - 31	NA	NA	0 / 16	0 / 16	0 / 16	0 / 16	0 / 16
	PCI Express Graphics (PEG)	NA	NA	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1
	Muxed SDVO Channels 1 - 2	NA	NA	0 / 2	0 / 2	0 / 2	0 / 2	NA
C-D[5]	PCI Express Lanes 6 - 15	NA	NA	NA	NA	0 / 10	0 / 10	0 / 2
	PCI Bus - 32 Bit	NA	NA	1 / 1	1 / 1	NA	NA	NA
	PATA Port	NA	NA	1 / 1	NA	1 / 1	NA	NA
	LAN Ports 1 - 2	NA	NA	NA	0 / 2	NA	0 / 2	NA
	DDIs 1 - 3	NA	NA	NA	NA	NA	NA	0 / 3
	USB 3.0 Ports	NA	NA	NA	NA	NA	NA	0 / 4
C-D	**Power**							
C-D	VCC_12V Contacts	NA	NA	12 / 12	12 / 12	12 / 12	12 / 12	12 / 12

3.3 Feature Fill Order

COM Express allows a variable number of ports to be implemented for several interfaces, per Table 3.2 and Table 3.3 above. Ports ***shall*** be populated in a "low to high" manner, per the following table.

Table 3.4: Module Feature Fill Order

Feature	Number of Ports	Fill Order
Express Card Support	1	EXCD 0
	2	EXCD 0,1
LAN	1	GBE channel 0
	2	GBE channels 0,1
	3	GBE channels 0,1,2
LVDS	1	LVDS channel A
	2	LVDS channels A,B
SATA / SAS	2	SATA / SAS channels 0,1
	3	SATA / SAS channels 0,1,2
	4	SATA / SAS channels 0,1,2,3
SDVO	1	SDVO channel B
	2	SDVO channels B,C
USB 2.0 Host	4	USB channels 0,1,2,3
	5	USB channels 0,1,2,3,4
	6	USB channels 0,1,2,3,4,5
	7	USB channels 0,1,2,3,4,5,6
	8	USB channels 0,1,2,3,4,5,6,7
USB 2.0 Client	1	USB channel 7
USB 3.0 SuperSpeed[6]	1	USB channel 0
	2	USB channels 0,1
	3	USB channels 0,1,2
	4	USB channels 0,1,2,3
DDI	1	DDI 1
	2	DDI 2
	3	DDI 3

The COM Express PCI Express lanes also have a prescribed fill order, described in Section 5.2 'PCI Express Link Configuration Guidelines' on page 92.

6 *The number of USB 2.0 channels must be equal to or greater than the number of USB 3.0 channels*

3.4 EAPI - Embedded Application Programming Interface

All COM Express Modules ***should*** support the Revision 1.1 of the PICMG defined Software API EAPI. This API allows for an easier interoperability of COM Express Modules.

Addressed functions are:

- System information
- Watchdog timer
- I2C Bus
- Flat Panel brightness control
- User storage area
- GPIO

4 Signal Descriptions

4.1 Signal Naming Convention

Active-low signals are indicated by a trailing '#' sign:	REQ#
Differential pairs are indicated by trailing '+' and '-' signs:	TX+, TX-
Bused signals are indicated by brackets, with LS bit first, MS bit last:	A[0:31]
Bus brackets may appear anywhere in the signal name:	CBE[0:3]#

4.2 Pin and Signal Buffer Types

Pin and Buffer type definitions apply to the signals in the Signal List Section below.

4.2.1 Pin Types

I	Input to the Module
O	Output from the Module
I/O	Bi-directional input / output signal
OD	Open drain output

4.2.2 Buffer Types

CMOS	Logic input or output. Input thresholds and output levels ***shall*** be 80% of supply rail for high side and 20% of the relevant supply rail for low side.
PCIE	PCI Express compatible differential signal. Please refer to the PCI Express Specification for details. PCIE transmit pins (Module outputs) ***shall*** be AC coupled on the Module. PCIE receive pins (Module inputs) ***shall*** be DC coupled on the COM Express Module and ***shall*** be assumed to be AC coupled off-Module, close to the signal source. If the target PCI Express device resides on the Carrier Board, the Module PCIE receive lanes (target PCIE device transmit lanes) ***shall*** be AC coupled near the device on the Carrier Board. If the Carrier Board implements a PCIE slot, then these signals ***shall*** be AC coupled on the add-in card, not on the Carrier Board.
PCI	PCI 2.3 compatible signal. Please refer to the PCI Rev. 2.3 Specification for details.
SATA	SATA compatible differential signal. Please refer to the SATA Specification for details. All COM Express SATA signals ***shall*** be AC coupled on the Module
LVDS	Low Voltage Differential Signal – 330mV nominal; 450mV maximum differential signal.
USB	USB 2.0 compatible differential signal. Please refer to the USB 2.0 Specification for details.
REF	Reference voltage output. ***May*** be sourced from a Module power plane.
PDS	Pull-down strap. A Module output pin that is either tied to GND or is not connected. Used to signal Module capabilities to the Carrier Board.
Analog	Inputs and Outputs used for LAN, and VGA are analog signals.
Power	Inputs used for power delivery to the Module electronics.

4.2.3 Power Rails and Tolerances

Pins are marked in Section 4.3 'Signal List' with the power rail associated with the pin, and, for input and I/O pins, with the input voltage tolerance. The pin power rail and the pin input voltage tolerance may be different. For example, the PCI group is defined as having a 3.3V power rail, meaning that the output signals will only be driven to 3.3V, but the pins are tolerant of 5V signals.

An additional label, “Suspend” indicates that the pin is active during suspend states (S3,S4,S5). If suspend modes are used, then care must be taken to avoid loading signals that are active during suspend to avoid excessive suspend mode current draw.

4.3 Signal List

COM Express signal descriptions are described in the following table. The Pin Availability column in the table indicates in which Pin-out Types the signal is available. Module Pin-out Types 1 through 6 and 10 are designated T1, T2, T3, T4, T5 ,T6, T10 in the Pin Availability column. A notation of “All” indicates that the signal is available to all Module Pin-out Types.

4.3.1 AC97 Audio / High Definition Audio

The AC ’97 audio codec interface is limited to support a single AC ’97 link. High Definition Audio ***may*** be supported.

Table 4.1: AC97/HDA Signals, Pin Types, and Descriptions

AC97 Audio / High Definition Audio	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
AC_RST# / HDA_RST#	O CMOS	3.3V Suspend/ 3.3V	Reset output to CODEC, active low.	All
AC_SYNC/ HDA_SYNC	O CMOS	3.3V / 3.3V	Sample-synchronization signal to the CODEC(s).	All
AC_BITCLK/ HDA_BITCLK	I/O CMOS	3.3V / 3.3V	Serial data clock generated by the external CODEC(s).	All
AC_SDOUT/ HDA_SDOUT	O CMOS	3.3V / 3.3V	Serial TDM data output to the CODEC.	All
AC_SDIN[0:2]/ HDA_SDIN[0:2]	I/O CMOS	3.3V Suspend/ 3.3V	Serial TDM data inputs from up to 3 CODECs.	All

The HDA signal level from some chipsets might be 1.5V. Module designers must add any necessary voltage translation circuitry to meet the COM Express 3.3V signaling requirement for AC-97/HDA signals.

The AC'97 or HDA codec on a COM Express Carrier Board ***shall*** be connected as the primary codec with the codec ID 00 using the data input line 'AC_SDIN0'. Up to two additional codecs with ID 01 and ID 10 ***may*** be connected to the COM Express Module by using the other designated signals AC_SDIN[1:2] / HDA_SDIN[1:2].

4.3.2 Ethernet

Up to 3 Gigabit Ethernet ports are defined, designated GBE0 through GBE2. The ports ***may*** operate in 10, 100, or 1000 Mbit/sec modes. Magnetics are assumed to be on the Carrier Board. All COM Express Modules ***shall*** implement at least one Ethernet port on the GBE0 pin slot and this ***should*** be capable of at least 10/100 mode.

Table 4.2: Gigabit Ethernet Signals, Pin Types, and Descriptions

Gigabit Ethernet	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
GBE0_MDI[0:3]+ GBE0_MDI[0:3]-	I/O Analog	3.3V max Suspend	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following: MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	All
GBE0_ACT#	OD CMOS	3.3V Suspend/ 3.3V	Gigabit Ethernet Controller 0 activity indicator, active low.	All
GBE0_LINK#	OD CMOS	3.3V Suspend/ 3.3V	Gigabit Ethernet Controller 0 link indicator, active low.	All
GBE0_LINK100#	OD CMOS	3.3V Suspend/ 3.3V	Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.	All
GBE0_LINK1000#	OD CMOS	3.3V Suspend/ 3.3V	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.	All
GBE0_CTREF	REF	GND min 3.3V max	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output ***shall*** be current limited on the Module. In the case in which the reference is shorted to ground, the current ***shall*** be limited to 250 mA or less.	All
GBE1_MDI[0:3]+ GBE1_MDI[0:3]-	I/O Analog	3.3V max Suspend	Gigabit Ethernet Controller 1: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following: MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/- This set of differential pairs, in conjunction with the GBE2_MDI[0:3] pairs, ***may*** also be used to implement a 10 Gigabit / sec interface, as described in Section 5.7 of this document. Note: Gigabit Ethernet port 1 does not have a CTREF output to the Carrier Board.	T3,T5
GBE1_ACT#	OD CMOS	3.3V Suspend/ 3.3V	Gigabit Ethernet Controller 1 activity indicator, active low.	T3,T5

Gigabit Ethernet	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
GBE1_LINK#	OD CMOS	3.3V Suspend/ 3.3V	Gigabit Ethernet Controller 1 link indicator, active low.	T3,T5
GBE1_LINK100#	OD CMOS	3.3V Suspend/ 3.3V	Gigabit Ethernet Controller 1 100 Mbit / sec link indicator, active low.	T3,T5
GBE1_LINK1000#	OD CMOS	3.3V Suspend/ 3.3V	Gigabit Ethernet Controller 1 1000 Mbit / sec link indicator, active low.	T3,T5
GBE2_MDI[0:3]+ GBE2_MDI[0:3]-	I/O Analog	3.3V max Suspend	Gigabit Ethernet Controller 2: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following: 1000BASE-T / 100BASE-TX / 10BASE-T MDI[0]+/- : B1_DA+/- : TX+/- : TX+/- MDI[1]+/- : B1_DB+/- : RX+/- : RX+/- MDI[2]+/- : B1_DC+/- MDI[3]+/- : B1_DD+/- This set of differential pairs, in conjunction with the GBE1_MDI[0:3] pairs, ***may*** also be used to implement a 10 Gigabit / sec interface, as described in Section 5.7 of this document.	T3,T5
GBE2_ACT#	OD CMOS	3.3V Suspend/ 3.3V	Gigabit Ethernet Controller 2 activity indicator, active low.	T3,T5
GBE2_LINK#	OD CMOS	3.3V Suspend/ 3.3V	Gigabit Ethernet Controller 2 link indicator, active low.	T3,T5
GBE2_LINK100#	OD CMOS	3.3V Suspend/ 3.3V	Gigabit Ethernet Controller 2 100 Mbit / sec link indicator, active low.	T3,T5
GBE2_LINK1000#	OD CMOS	3.3V Suspend/ 3.3V	Gigabit Ethernet Controller 2 1000 Mbit / sec link indicator, active low.	T3,T5
GBE2_CTREF	REF	GND min 3.3V max	Reference voltage for Carrier Board Ethernet channel 1 and 2 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output ***shall*** be current limited on the Module. In the case in which the reference is shorted to ground, the current ***shall*** be 250 mA or less.	T3,T5

4.3.3 IDE

Parallel ATA support for up to 2 devices in a master/slave configuration. This signaling interface is limited to ATA100 speeds. Higher (ATA133) speeds are not defined. PATA signal pins are reused in Pin-out Type 3 and 5 Modules for 2 additional GB Ethernet interfaces; and for USB3.0 interfaces in Type 6.

Table 4.3: IDE Signals, Pin Types, and Descriptions

IDE	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
IDE_D[0:15]	I/O CMOS	3.3V / 5V	Bidirectional data to / from IDE device.	T2, T4
IDE_A[0:2]	O CMOS	3.3V / 3.3V	Address lines to IDE device.	T2, T4
IDE_IOW#	O CMOS	3.3V / 3.3V	I/O write line to IDE device. Data latched on trailing (rising) edge.	T2, T4
IDE_IOR#	O CMOS	3.3V / 3.3V	I/O read line to IDE device.	T2, T4
IDE_REQ	I CMOS	3.3V / 5V	IDE Device DMA Request. It is asserted by the IDE device to request a data transfer.	T2, T4
IDE_ACK#	O CMOS	3.3V / 3.3V	IDE Device DMA Acknowledge.	T2, T4
IDE_CS1#	O CMOS	3.3V / 3.3V	IDE Device Chip Select for 1F0h to 1FFh range.	T2, T4
IDE_CS3#	O CMOS	3.3V / 3.3V	IDE Device Chip Select for 3F0h to 3FFh range.	T2, T4
IDE_IORDY	I CMOS	3.3V / 5V	IDE device I/O ready input. Pulled low by the IDE device to extend the cycle.	T2, T4
IDE_RESET#	O CMOS	3.3V / 3.3V	Reset output to IDE device, active low.	T2, T4
IDE_IRQ	I CMOS	3.3V / 5V	Interrupt request from IDE device.	T2, T4
IDE_CBLID#	I CMOS	3.3V / 5V	Input from off-Module hardware indicating the type of IDE cable being used. High indicates a 40-pin cable used for legacy IDE modes. Low indicates that an 80-pin cable with interleaved grounds is used. Such a cable is required for Ultra-DMA 66, 100 and 133 modes.	T2, T4

4.3.4 Serial ATA

Serial ATA links for support of existing SATA-150 and SATA-300 devices. Alternatively, this interface ***may*** be used for Serial Attached SCSI (SAS).

Table 4.4: SATA Signals, Pin Types, and Descriptions

Serial ATA	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
SATA0_TX+ SATA0_TX-	O SATA	AC coupled on Module	Serial ATA or SAS Channel 0 transmit differential pair.	All
SATA0_RX+ SATA0_RX-	I SATA	AC coupled on Module	Serial ATA or SAS Channel 0 receive differential pair.	All
SATA1_TX+ SATA1_TX-	O SATA	AC coupled on Module	Serial ATA or SAS Channel 1 transmit differential pair.	All
SATA1_RX+ SATA1_RX-	I SATA	AC coupled on Module	Serial ATA or SAS Channel 1 receive differential pair.	All
SATA2_TX+ SATA2_TX-	O SATA	AC coupled on Module	Serial ATA or SAS Channel 2 transmit differential pair.	T1-6
SATA2_RX+ SATA2_RX-	I SATA	AC coupled on Module	Serial ATA or SAS Channel 2 receive differential pair.	T1-6
SATA3_TX+ SATA3_TX-	O SATA	AC coupled on Module	Serial ATA or SAS Channel 3 transmit differential pair.	T1-6
SATA3_RX+ SATA3_RX-	I SATA	AC coupled on Module	Serial ATA or SAS Channel 3 receive differential pair.	T1-6
(S)ATA_ACT#	I/O CMOS	3.3V / 3.3V	ATA (parallel and serial) or SAS activity indicator, active low.	T1-6

4.3.5 General Purpose PCI Express Lanes

The number of available PCI Express lanes varies with the Module Pin-out Type (refer to Section 5.2 'PCI Express Link Configuration Guidelines' on page 92). If the Module supports off-Module x16 PCI Express Graphics, then PCI Express Lanes 16-31 ***shall*** be used to implement this.

Table 4.5: PCI Express Lanes Signals, Pin Types, and Descriptions

PCI Express Lanes (General Purpose)	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
PCIE_TX[0:3]+ PCIE_TX[0:3]-	O PCIE	AC coupled on Module	PCI Express Differential Transmit Pairs 0 through 3	All
PCIE_RX[0:3]+ PCIE_RX[0:3]-	I PCIE	AC coupled off Module	PCI Express Differential Receive Pairs 0 through 3	All
PCIE_TX[4:5]+ PCIE_TX[4:5]-	O PCIE	AC coupled on Module	PCI Express Differential Transmit Pairs 4 through 5	T1-6
PCIE_RX[4:5]+ PCIE_RX[4:5]-	I PCIE	AC coupled off Module	PCI Express Differential Receive Pairs 4 through 5	T1-6
PCIE_TX[6:7]+ PCIE_TX[6:7]-	O PCIE	AC coupled on Module	PCI Express Differential Transmit Pairs 6 through 7	T4, T5, T6
PCIE_RX[6:7]+ PCIE_RX[6:7]-	I PCIE	AC coupled off Module	PCI Express Differential Receive Pairs 6 through 7	T4, T5, T6
PCIE_TX[8:15]+ PCIE_TX[8:15]-	O PCIE	AC coupled on Module	PCI Express Differential Transmit Pairs 8 through 15	T4, T5
PCIE_RX[8:15]+ PCIE_RX[8:15]-	I PCIE	AC coupled off Module	PCI Express Differential Receive Pairs 8 through 15	T4, T5
PCIE_TX[16:31]+ PCIE_TX[16:31]-	O PCIE	AC coupled on Module	PCI Express Differential Transmit Pairs 16 through 31 These are same lines as PEG_TX[0:15]+ and -	T2, T3, T4, T5, T6
PCIE_RX[16:31]+ PCIE_RX[16:31]-	I PCIE	AC coupled off Module	PCI Express Differential Receive Pairs 16 through 31 These are the same lines as PEG_RX[0:15] + and -	T2, T3, T4, T5, T6
PCIE_CLK_REF+ PCIE_CLK_REF-	O PCIE	PCIE	Reference clock output for all PCI Express and PCI Express Graphics lanes.	All

4.3.6 PEG PCI Express Lanes

These signals ***may*** be multiplexed with SDVO signals or defined as ordinary PCI Express signals on Module Types 2-5. Type 6 provides dedicated PEG and SDVO channels. The PEG lanes are the same lanes as PCI Express lanes 16-31.

Table 4.6: PEG Signals, Pin Types, and Descriptions

PCI Express Lanes **x16 Graphics**	**Pin Type**	**Pwr Rail / Tolerance**		**Pin Availability**
PEG_TX[0:15]+ PEG_TX[0:15]-	O PCIE	AC coupled on Module	PCI Express Graphics transmit differential pairs. Some of these are multiplexed with SDVO lines in Type 2-5. In Type 6 SDVO pins are on DDI 1 (refer to Section 4.4.5 “SDVO (Types 2-5)“). These are the same lines as PCIE_TX[16:31]+ and - in Module pin-out Types 4, 5 and 6.	T2, T3, T4, T5,T6
PEG_RX[0:15]+ PEG_RX[0:15]-	I PCIE	AC coupled off Module	PCI Express Graphics receive differential pairs. Some of these are multiplexed with SDVO lines in Type 2-5. In Type 6 SDVO pins are on DDI 1 (refer to Section 4.4.5 “SDVO (Types 2-5)“). These are the same lines as PCIE_RX[16:31]+ and - in Module pin-out types 4, 5 and 6.	T2, T3, T4, T5,T6
PEG_LANE_RV#	I CMOS	3.3V / 3.3V	PCI Express Graphics lane reversal input strap. Pull low on the Carrier Board to reverse lane order. Be aware that the SDVO lines that share this interface do not necessarily reverse order if this strap is low.	T2, T3, T4, T5,T6
PEG_ENABLE#	I CMOS	3.3V / 3.3V	Strap to enable PCI Express x16 external graphics interface. Pull low to enable the x16 PEG interface.	T2, T3, T4, T5

4.3.7 ExpressCard

ExpressCard is a small form factor expansion card for mobile systems that uses PCI Express or USB as the interface. It is similar in concept and scope to CardBus. COM Express Modules ***shall*** provide support functions for at least one ExpressCard. This does not mean that a Module PCI Express lane or USB link are specifically allocated to ExpressCard use, but it does mean that the Module pins for ExpressCard detection and support are present.

Table 4.7: ExpressCard Signals, Pin Types, and Descriptions

ExpressCard Support	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
EXCD[0:1]_CPPE#	I CMOS	3.3V / 3.3V	PCI ExpressCard: PCI Express capable card request, active low, one per card	All
EXCD[0:1]_PERST#	O CMOS	3.3V / 3.3V	PCI ExpressCard: reset, active low, one per card	All

4.3.8 PCI Bus

The PCI bus interface is specified to be a 32-bit PCI 2.3 compliant bus with speed options of 33MHz or 66MHz.

Table 4.8: PCI Signals, Pin Types, and Descriptions

PCI Bus	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
PCI_AD[0:31]	I/O CMOS	3.3V / 5V	PCI bus multiplexed address and data lines	T2, T3
PCI_C/BE[0:3]#	I/O CMOS	3.3V / 5V	PCI bus byte enable lines, active low	T2, T3
PCI_DEVSEL#	I/O CMOS	3.3V / 5V	PCI bus Device Select, active low.	T2, T3
PCI_FRAME#	I/O CMOS	3.3V / 5V	PCI bus Frame control line, active low.	T2, T3
PCI_IRDY#	I/O CMOS	3.3V / 5V	PCI bus Initiator Ready control line, active low.	T2, T3
PCI_TRDY#	I/O CMOS	3.3V / 5V	PCI bus Target Ready control line, active low.	T2, T3
PCI_STOP#	I/O CMOS	3.3V / 5V	PCI bus STOP control line, active low, driven by cycle initiator.	T2, T3
PCI_PAR	I/O CMOS	3.3V / 5V	PCI bus parity	T2, T3
PCI_PERR#	I/O CMOS	3.3V / 5V	Parity Error: An external PCI device drives PERR# when it receives data that has a parity error.	T2, T3
PCI_REQ[0:3]#	I CMOS	3.3V / 5V	PCI bus master request input lines, active low.	T2, T3
PCI_GNT[0:3]#	O CMOS	3.3V / 5V	PCI bus master grant output lines, active low.	T2, T3
PCI_RESET#	O CMOS	3.3V Suspend/ 5V	PCI Reset output, active low.	T2, T3
PCI_LOCK#	I/O CMOS	3.3V / 5V	PCI Lock control line, active low.	T2, T3
PCI_SERR#	I/O OD CMOS	3.3V / 5V	System Error: SERR# ***may*** be pulsed active by any PCI device that detects a system error condition.	T2, T3
PCI_PME#	I CMOS	3.3V Suspend/ 5V	PCI Power Management Event: PCI peripherals drive PME# to wake system from low-power states S1–S5.	T2, T3
PCI_CLKRUN#	I/O CMOS	3.3V / 5V	Bidirectional pin used to support PCI clock run protocol for mobile systems.	T2, T3
PCI_IRQ[A:D]#	I CMOS	3.3V / 5V	PCI interrupt request lines.	T2, T3
PCI_CLK	O CMOS	3.3V / 3.3V	PCI 33MHz clock output.	T2, T3
PCI_M66EN	I CMOS	3.3V / 5V	Module input signal indicates whether an off-Module PCI device is capable of 66MHz operation. Pulled to GND by Carrier Board device or by Slot Card if the devices are NOT capable of 66 MHz operation. If the Module is not capable of supporting 66 MHz PCI operation, this input ***may*** be a no-connect on the Module. If the Module is capable of supporting 66 MHz PCI operation, and if this input is held low by the Carrier Board, the Module PCI interface ***shall*** operate at 33 MHz.	T2, T3

4.3.9 USB

All USB interfaces ***shall*** be USB 2.0 compliant. The minimum of 4 USB channels provides support for keyboard, mouse, CD/DVD drive, and one additional device. Up to four of the eight USB 2.0 ports ***may*** support the extended signaling for SuperSpeed USB 3.0. USB7 ***may*** optionally be configured as a USB client.

Table 4.9: USB Signals, Pin Types, and Descriptions

USB	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
USB[0:7]+ USB[0:7]-	I/O USB	3.3V Suspend/ 3.3V	USB differential pairs, channels 0 through 7. USB7 ***may*** be configured as a USB client or as a host, or both, at the Module designer's discretion. All other USB ports, if implemented, ***shall*** be host ports.	All
USB_0_1_OC#	I CMOS	3.3V Suspend/ 3.3V	USB over-current sense, USB channels 0 and 1. A pull-up for this line ***shall*** be present on the Module. An open drain driver from a USB current monitor on the Carrier Board ***may*** drive this line low. Do not pull this line high on the Carrier Board.	All
USB_2_3_OC#	I CMOS	3.3V Suspend/ 3.3V	USB over-current sense, USB channels 2 and 3. A pull-up for this line ***shall*** be present on the Module. An open drain driver from a USB current monitor on the Carrier Board ***may*** drive this line low. Do not pull this line high on the Carrier Board.	All
USB_4_5_OC#	I CMOS	3.3V Suspend/ 3.3V	USB over-current sense, USB channels 4 and 5. A pull-up for this line ***shall*** be present on the Module. An open drain driver from a USB current monitor on the Carrier Board ***may*** drive this line low. Do not pull this line high on the Carrier Board.	All
USB_6_7_OC#	I CMOS	3.3V Suspend/ 3.3V	USB over-current sense, USB channels 6 and 7. A pull-up for this line ***shall*** be present on the Module. An open drain driver from a USB current monitor on the Carrier Board ***may*** drive this line low. Do not pull this line high on the Carrier Board.	All
USB_SSTX[0:3]+ USB_SSTX[0:3]-	O PCIE	AC coupled on Module	Additional transmit signal differential pairs for the SuperSpeed USB data path.	T6
USB_SSRX[0:3]+ USB_SSRX[0:3]-	I PCIE	AC coupled off Module	Additional receive signal differential pairs for the SuperSpeed USB data path.	T6
USB_SSTX[0:1]+ USB_SSTX[0:1]-	O PCIE	AC coupled on Module	Additional transmit signal differential pairs for the SuperSpeed USB data path.	T10
USB_SSRX[0:1]+ USB_SSRX[0:1]-	I PCIE	AC coupled off Module	Additional receive signal differential pairs for the SuperSpeed USB data path.	T10
USB_HOST_PRSNT	I CMOS	3.3V Suspend/ 3.3V	Module USB client ***may*** detect the presence of a USB host. A high value indicates that a host is present.	T10

4.3.10 LVDS Flat Panel

Low voltage differential signaling flat-panel interface. The Module pin-out allows one single channel display interface (1 pixel per clock) with up to 24 bit color. Alternatively, one dual channel display (2 pixels per clock) with up to 24 bit color, 48 bits per clock is allowed. Includes panel backlight control and EDID support.

The LVDS A channel and the control signals are pin shared with eDP signals. Refer to Section 4.3.29 'eDP - Embedded DisplayPort'

Table 4.10: LVDS Signals, Pin Types, and Descriptions

LVDS Flat Panel	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
LVDS_A[0:3]+ LVDS_A[0:3]-	O LVDS	LVDS	LVDS Channel A differential pairs	All
LVDS_A_CK+ LVDS_A_CK-	O LVDS	LVDS	LVDS Channel A differential clock	All
LVDS_B[0:3]+ LVDS_B[0:3]-	O LVDS	LVDS	LVDS Channel B differential pairs	T1-6
LVDS_B_CK+ LVDS_B_CK-	O LVDS	LVDS	LVDS Channel B differential clock	T1-6
LVDS_VDD_EN	O CMOS	3.3V / 3.3V	LVDS panel power enable	All
LVDS_BKLT_EN	O CMOS	3.3V / 3.3V	LVDS panel backlight enable	All
LVDS_BKLT_CTRL	O CMOS	3.3V / 3.3V	LVDS panel backlight brightness control	All
LVDS_I2C_CK	I/O OD CMOS	3.3V / 3.3V	I2C clock output for LVDS display use	All
LVDS_I2C_DAT	I/O OD CMOS	3.3V / 3.3V	I2C data line for LVDS display use	All

4.3.11 LPC Interface

The LPC bus provides legacy I/O support on a Carrier Board via a Super I/O and system management devices.

Table 4.11: LPC Signals, Pin Types, and Descriptions

LPC Interface	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
LPC_AD[0:3]	I/O CMOS	3.3V / 3.3V	LPC multiplexed address, command and data bus	All
LPC_FRAME#	O CMOS	3.3V / 3.3V	LPC frame indicates the start of an LPC cycle	All
LPC_DRQ[0:1]#	I CMOS	3.3V / 3.3V	LPC serial DMA request	All
LPC_SERIRQ	I/O CMOS	3.3V / 3.3V	LPC serial interrupt	All
LPC_CLK	O CMOS	3.3V / 3.3V	LPC clock output - 33MHz nominal	All

4.3.12 SPI Interface

The SPI bus is used to support SPI-compatible flash devices. The SPI flash device can be up to 16 MB (128 Mb). The SPI bus is clocked at either 20 MHz, 25 MHz, 33 MHz or 50 MHz. SPI devices selected ***should*** support one of these frequencies. SPI support is introduced in COM.0 R2.0 for all Types.

Table 4.12: SPI Signals, Pin Types, and Descriptions

SPI Interface[7]	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
SPI_CS#	O CMOS	3.3V Suspend/ 3.3V	Chip select for Carrier Board SPI - ***may*** be sourced from chipset SPI0 or SPI1	All
SPI_MISO	I CMOS	3.3V Suspend/ 3.3V	Data in to Module from Carrier SPI	All
SPI_MOSI	O CMOS	3.3V Suspend/ 3.3V	Data out from Module to Carrier SPI	All
SPI_CLK	O CMOS	3.3V Suspend/ 3.3V	Clock from Module to Carrier SPI	All
SPI_POWER	O	3.3V Suspend/ 3.3V	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module ***shall*** provide a minimum of 100mA on SPI_POWER. Carriers ***shall*** use less than 100mA of SPI_POWER. SPI_POWER ***shall*** only be used to power SPI devices on the Carrier Board.	All
BIOS_DIS[0:1]#	I CMOS	NA	Selection straps to determine the BIOS boot device. The Carrier ***should*** only float these or pull them low, please refer to Table 4.13 for strapping options of BIOS disable signals.	All

On COM.0 R1.0, there is a single pin dedicated to the BIOS Disable function. The pin is A34, named BIOS_DISABLE#. If the Carrier Board leaves BIOS_DISABLE# floating, then the Module boots from the BIOS on the Module. That Module BIOS can be on any bus the Module designer chooses (LPC, SPI, etc.). If the Carrier Board pulls BIOS_DISABLE# to GND, then the on-Module BIOS is disabled and the Module boots from a Carrier Board firmware hub on the LPC bus.

From COM.0 R2.0, the Carrier based BIOS options have been expanded to support SPI devices. A second BIOS DISABLE pin (BIOS_DIS1#) has been added to allow for multiple Carrier implementations for external BIOS devices. The BIOS_DISABLE# pin has been renamed to BIOS_DIS0#. Additional pins have been added to bring the SPI signals to the Carrier. These pins are defined in Table 4.12 above.

The Table 4.13 below allows for Carrier Board LPC FWH operation that is backward compatible with COM.0 Rev.1 Carriers. It also allows two Carrier SPI options: SPI0 on Carrier and SPI1 on the Module, or SPI0 on the Module and SP1 on the Carrier.

7 SPI support is introduced in COM.0 R2.0

Table 4.13: Effect of the BIOS disable signals

BIOS_DIS1#	BIOS_DIS0#	Chipset SPI CS1# Destination	Chipset SPI CS0# Destination	Carrier SPI_CS#	SPI Descriptor	Bios Entry	Ref Line
1	1	Module	Module	High	Module	SPI0/SPI1	0
1	0	Module	Module	High	Module	Carrier FWH	1
0	1	Module	Carrier	SPI0	Carrier	SPI0/SPI1	2
0	0	Carrier	Module	SPI1	Module	SPI0/SPI1	3

The BIOS Entry point ***may*** be in SPI0 or SPI1 as determined by the descriptor table in the SPI0 device. The Module ***may*** have one or two SPI devices, or a FWH. Carrier Boards ***may*** have zero or one SPI device, and ***may*** have zero or one LPC FWH.

With special circuitry on the Module it's possible to have a single SPI device, but allow the Module GBE, ME and Platform data to stay with the Module even in the case of a Carrier Board SPI BIOS entry per Ref Line 2 above. The Module SPI would include a descriptor table, BIOS code, GBE parameters, ME parameters, and platform data. For table line entries 0 and 1 above, the Module SPI device would be selected by SPI CS0# from the chipset. For table line entry 2 above, the Module SPI device would be selected by chipset SPI CS1# instead of CS0#. This would be achieved by low cost circuitry on the Module. The Module SPI device descriptor table and the Module BIOS code would be used in table line entries 0, 1 and 3.

An alternative arrangement would be to have two SPI devices on the Module. The descriptor table and the actual BIOS are in SPI0, and that the GBE LAN data, ME data and platform data reside in SPI1. Then a Carrier Board SPI option is allowed (table line ref 2) in which the actual BIOS is on the Carrier, and the Module specific data stays with the Module in SPI1. The Module SPI1 device has to be write-enabled. The Carrier SPI0 device could be write protected if desired (as is the case in some regulated industries such as casino gaming).

Note that in the case of the BIOS boot from Carrier FWH (table line ref 1), the Module SPI devices are still enabled and active. They are used by the GBE LAN hardware and the management engine. They can keep the BIOS code as well, but it is not used. The ICH pin straps cause an LPC FWH BIOS boot.

SPI Power

Introducing a SPI_POWER pin is desirable because some Module implementations will have the SPI power domain in power state S0 and others in S5. It is easier for Carrier Board designers to take the Carrier SPI power from a pin on the Module.

Module Vs Carrier Board Pull-ups

There ***shall*** not be any Carrier Board pull-ups or pull-downs on the five SPI_x signals. All such terminations ***shall*** be on the Module. The Module designer ***shall*** determine the correct power domain that these signals are terminated to.

4.3.13 Analog VGA

Analog RGB interface for CRT monitor and DDC support.

Table 4.14: VGA Signals, Pin Types, and Descriptions

Analog VGA	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
VGA_RED	O Analog	Analog	Red for monitor. Analog DAC output, designed to drive a 37.5Ω equivalent load.	T1-6
VGA_GRN	O Analog	Analog	Green for monitor. Analog DAC output, designed to drive a 37.5Ω equivalent load.	T1-6
VGA_BLU	O Analog	Analog	Blue for monitor. Analog DAC output, designed to drive a 37.5Ω equivalent load.	T1-6
VGA_HSYNC	O CMOS	3.3V / 3.3V	Horizontal sync output to VGA monitor	T1-6
VGA_VSYNC	O CMOS	3.3V / 3.3V	Vertical sync output to VGA monitor	T1-6
VGA_I2C_CK	I/O OD CMOS	3.3V / 3.3V	DDC clock line (I2C port dedicated to identify VGA monitor capabilities)	T1-6
VGA_I2C_DAT	I/O OD CMOS	3.3V / 3.3V	DDC data line.	T1-6

4.3.14 PEG Multiplexed SDVO

Serial Digital Video Output to LVDS or TMDS transmitters on the Carrier Board. These signals, if implemented, ***shall*** be multiplexed with PEG signals on Types 2-5.

Table 4.15: SDVO Signals, Pin Types, and Descriptions

SDVO	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
SDVOB_RED+ SDVOB_RED-	O PCIE	AC coupled on Module	Serial Digital Video B red output differential pair Multiplexed with PEG_TX[0]+ and PEG_TX[0]-	T2, T3, T4, T5
SDVOB_GRN+ SDVOB_GRN-	O PCIE	AC coupled on Module	Serial Digital Video B green output differential pair Multiplexed with PEG_TX[1]+ and PEG_TX[1]-	T2, T3, T4, T5
SDVOB_BLU+ SDVOB_BLU-	O PCIE	AC coupled on Module	Serial Digital Video B blue output differential pair Multiplexed with PEG_TX[2]+ and PEG_TX[2]-	T2, T3, T4, T5
SDVOB_CK+ SDVOB_CK-	O PCIE	AC coupled on Module	Serial Digital Video B clock output differential pair. Multiplexed with PEG_TX[3]+ and PEG_TX[3]-	T2, T3, T4, T5,
SDVOB_INT+ SDVOB_INT-	I PCIE	AC coupled off Module	Serial Digital Video B interrupt input differential pair. Multiplexed with PEG_RX[1]+ and PEG_RX[1]-	T2, T3, T4, T5
SDVOC_RED+ SDVOC_RED-	O PCIE	AC coupled on Module	Serial Digital Video C red output differential pair. Multiplexed with PEG_TX[4]+ and PEG_TX[4]-	T2, T3, T4, T5
SDVOC_GRN+ SDVOC_GRN-	O PCIE	AC coupled on Module	Serial Digital Video C green output differential pair. Multiplexed with PEG_TX[5]+ and PEG_TX[5]-	T2, T3, T4, T5
SDVOC_BLU+ SDVOC_BLU-	O PCIE	AC coupled on Module	Serial Digital Video C blue output differential pair. Multiplexed with PEG_TX[6]+ and PEG_TX[6]-	T2, T3, T4, T5
SDVOC_CK+ SDVOC_CK-	I/O OD CMOS	AC coupled on Module	Serial Digital Video C clock output differential pair. Multiplexed with PEG_TX[7]+ and PEG_TX[7]-	T2, T3, T4, T5
SDVOC_INT+ SDVOC_INT-	I PCIE	AC coupled off Module	Serial Digital Video C interrupt input differential pair. Multiplexed with PEG_RX[5]+ and PEG_RX[5]-	T2, T3, T4, T5
SDVO_TVCLKIN+ SDVO_TVCLKIN-	I PCIE	AC coupled off Module	Serial Digital Video TVOUT synchronization clock input differential pair. Multiplexed with PEG_RX[0]+ and PEG_RX[0]-	T2, T3, T4, T5
SDVO_FLDSTALL+ SDVO_FLDSTALL-	I PCIE	AC coupled off Module	Serial Digital Video Field Stall input differential pair. Multiplexed with PEG_RX[2]+ and PEG_RX[2]-	T2, T3, T4, T5
SDVO_CLK	I/O OD CMOS	2.5V / 2.5V	SDVO I2C clock line - to set up SDVO peripherals.	T2, T3, T4, T5
SDVO_DATA	I/O OD CMOS	2.5V / 2.5V	SDVO I2C data line - to set up SDVO peripherals.	T2, T3, T4, T5

4.3.15 Digital Display Interfaces (DDI) - Module Type 6 and 10

Module Types 6 and 10 use Digital Display Interfaces (DDI) to provide DisplayPort, HDMI/DVI, and SDVO interfaces. Type 10 Modules can contain a single DDI (DDI[0]) that can support DisplayPort, HDMI/DVI, and SDVO. Type 6 Modules can contain up to 3 DDIs (DDI[1:3]) of which DDI[1:3] can support DisplayPort, HDMI/DVI and DDI[1] can support DisplayPort, HDMI/DVI, and SDVO. The main difference is that SDVO is only supported on DDI[0] for Type 10 Modules and DDI[1] for Type 6 Modules.

This specification leverages the work done by VESA to provide guidance on how a Carrier might support DP or HDMI/DVI from a DDI using a cable adapter to convert from DisplayPort to HDMI/DVI. Note that a Carrier can contain the same circuit that VESA shows in the cable adapter for a direct connect HDMI/DVI interface. The DisplayPort Interoperability Guideline Version 1.1a dated February 5, 2009 can be downloaded from the VESA website after registration at http://www.vesa.org/vesa-standards/free-standards. The VESA specification uses the term Dual-Mode Source to define a source that can be configured for DisplayPort or TMDS (HDMI/DVI) - this is equivalent to a Module DDI. Figure 4-1 shows a conceptual example circuit that could be used on a Module. Actual circuit implementations will vary.

Figure 4-1: Dual-Mode COM Express Module Implementation

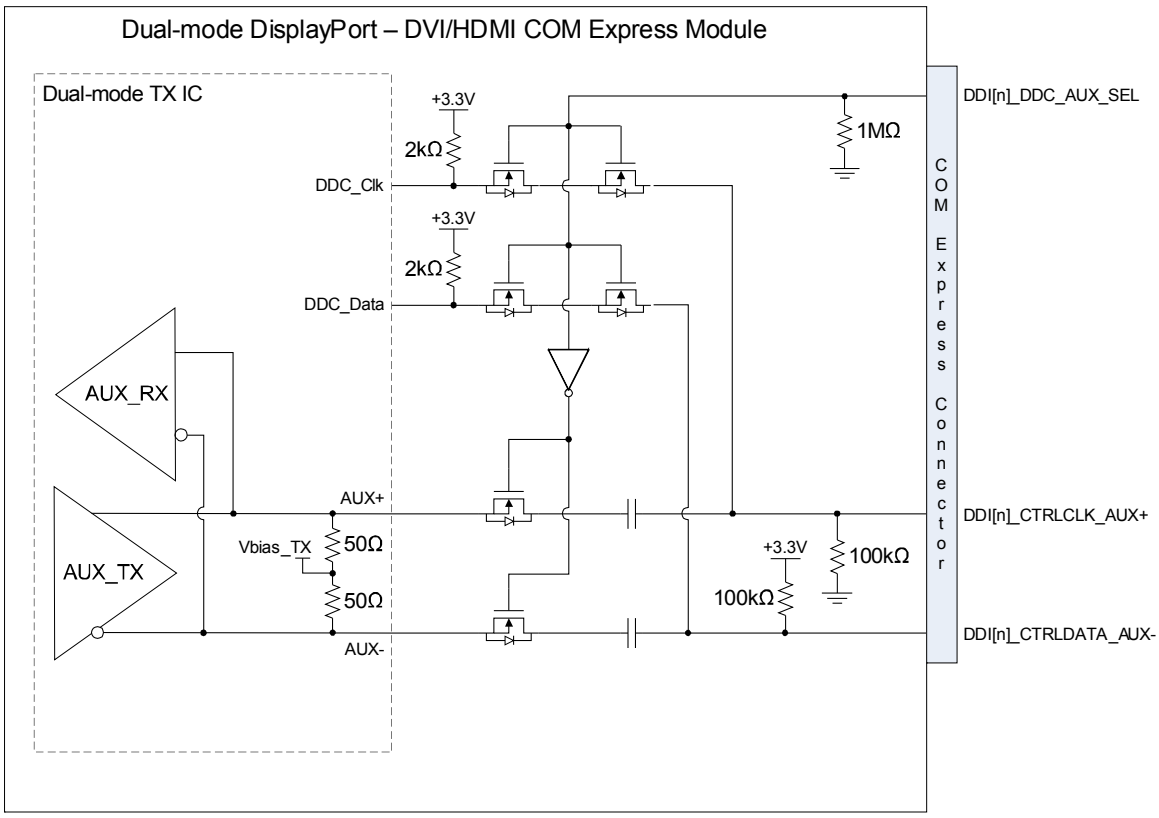


Table 4.16 'Module and Carrier Combinations' provides an idea of the type of circuit that might be necessary for Carriers supporting DisplayPort, HDMI/DVI.

Table 4.16: Module and Carrier Combinations

Module	Carrier / Cable Adapter Requirements	Destination
DP only	None - Straight through to DP receptacle	DisplayPort
	N/A – not a valid combination	DVI/HDMI
DVI/HDMI	N/A – not a valid combination	DisplayPort
	None - Straight through to DVI/HDMI receptacle	DVI/HDMI
Dual Mode	None - Straight through to DP receptacle	DisplayPort
	Level shifters on DDC before DVI/HDMI connector. (Optional level shifters on data, per Module requirements.)	DVI/HDMI

Requirements

Module DDI[0] ***may*** support any combination of DisplayPort, DVI/HDMI and SDVO.

Module DDI[1] ***may*** support any combination of DisplayPort, DVI/HDMI and SDVO.

Module DDI[2:3] ***may*** support any combination of DisplayPort and DVI/HDMI.

Module DDI ports ***should*** support more than DVI/HDMI.

Module that support Dual-Mode DDI interface ***shall*** implement the necessary muxing circuitry and control logic to ensure that the Module works properly with Carriers expecting DisplayPort or DVI/HDMI.

Modules ***shall*** meet the voltage and tolerance requirements as defined in the Signals, Pin Types, and Descriptions. This ***may*** require that a Module contain level shifters.

The pin map uses a generic name for the DDI pins. Table 4.19 below, details the mapping between the DDI pins and the different types of video interfaces supported.

Table 4.17: Type 6 DDI Signals, Pin Types, and Descriptions

DDI	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
DDI[1:3]_PAIR[0:3]+ DDI[1:3]_PAIR[0:3]-	O PCIE	AC coupled off Module	DDI 1 to 3 Pair[0:3] differential pairs	T6
DDI[1:3]_DDC_AUX_SEL	I CMOS	3.3V / 3.3V	Selects the function of DDI[1:3]_CTRLCLK_AUX+ and DDI[1:3]_CTRLDATA_AUX-. This pin ***shall*** have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.	T6
DDI[1:3]_CTRLCLK_AUX+	I/O PCIE	AC coupled on Module	DP AUX+ function if DDI[1:3]_DDC_AUX_SEL is no connect	T6
	I/O OD CMOS	3.3V / 3.3V	HDMI/DVI I2C CTRLCLK if DDI[1:3]_DDC_AUX_SEL is pulled high	T6
DDI[1:3]_CTRLDATA_AUX-	I/O PCIE	AC coupled on Module	DP AUX- function if DDI[1:3]_DDC_AUX_SEL is no connect	T6
	I/O OD CMOS	3.3V / 3.3V	HDMI/DVI I2C CTRLDATA if DDI[1:3]_DDC_AUX_SEL is pulled high	T6
DDI[1:3]_HPD	I CMOS	3.3V / 3.3V	DDI Hot-Plug Detect	T6

Table 4.18: Type 10 DDI Signals, Pin Types, and Descriptions

DDI	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
DDI0_PAIR[0:3]+ DDI0_PAIR[0:3]-	O PCIE	AC coupled off Module	DDI 0 Pair[0:3] differential pairs	T10
DDI[0]_DDC_AUX_SEL	I CMOS	3.3V / 3.3V	Selects the function of DDI[0]_CTRLCLK_AUX+ and DDI[0]_CTRLDATA_AUX-. This pin ***shall*** have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.	T10
DDI[0]_CTRLCLK_AUX+	I/O PCIE	AC coupled on Module	DP AUX+ function if DDI[0]_DDC_AUX_SEL is no connect	T10
	I/O OD CMOS	3.3V / 3.3V	HDMI/DVI I2C CTRLCLK if DDI[0]_DDC_AUX_SEL is pulled high	T10
DDI[0]_CTRLDATA_AUX-	I/O PCIE	AC coupled on Module	DP AUX- function if DDI[0]_DDC_AUX_SEL is no connect	T10
	I/O OD CMOS	3.3V / 3.3V	HDMI/DVI I2C CTRLDATA if DDI[0]_DDC_AUX_SEL is pulled high	T10
DDI0_HPD	I CMOS	3.3V / 3.3V	DDI Hot-Plug Detect	T10

Table 4.19: Type 6 DDI

	Pin Name	Type 6 Pin Number	SDVO	DP	HDMI/DVI (TMDS Signaling)
DDI 1	DDI1_PAIR0+	D26	SDVO1_RED+	DP1_LANE0+	TMDS1_DATA2+
	DDI1_PAIR0-	D27	SDVO1_RED-	DP1_LANE0-	TMDS1_DATA2-
	DDI1_PAIR1+	D29	SDVO1_GRN+	DP1_LANE1+	TMDS1_DATA1+
	DDI1_PAIR1-	D30	SDVO1_GRN-	DP1_LANE1-	TMDS1_DATA1-
	DDI1_PAIR2+	D32	SDVO1_BLU+	DP1_LANE2+	TMDS1_DATA0+
	DDI1_PAIR2-	D33	SDVO1_BLU-	DP1_LANE2-	TMDS1_DATA0-
	DDI1_PAIR3+	D36	SDVO1_CK+	DP1_LANE3+	TMDS1_CLK+
	DDI1_PAIR3-	D37	SDVO1_CK-	DP1_LANE3-	TMDS1_CLK-
	DDI1_PAIR4+	C25	SDVO1_INT+		
	DDI1_PAIR4-	C26	SDVO1_INT-		
	DDI1_PAIR5+	C29	SDVO1_TVCLKIN+		
	DDI1_PAIR5-	C30	SDVO1_TVCLKIN-		
	DDI1_PAIR6+	C15	SDVO1_FLDSTALL+		
	DDI1_PAIR6-	C16	SDVO1_FLDSTALL-		
	DDI1_HPD	C24		DP1_HPD	HDMI1_HPD
	DDI1_CTRLCLK_AUX+	D15	SDVO1_CTRLCLK	DP1_AUX+	HMDI1_CTRLCLK
	DDI1_CTRLDATA_AUX-	D16	SDVO1_CTRLDATA	DP1_AUX-	HMDI1_CTRLDATA
	DDI1_DDC_AUX_SEL	D34			
DDI 2	DDI2_PAIR0+	D39		DP2_LANE0+	TMDS2_DATA2+
	DDI2_PAIR0-	D40		DP2_LANE0-	TMDS2_DATA2-
	DDI2_PAIR1+	D42		DP2_LANE1+	TMDS2_DATA1+
	DDI2_PAIR1-	D43		DP2_LANE1-	TMDS2_DATA1-
	DDI2_PAIR2+	D46		DP2_LANE2+	TMDS2_DATA0+
	DDI2_PAIR2-	D47		DP2_LANE2-	TMDS2_DATA0-
	DDI2_PAIR3+	D49		DP2_LANE3+	TMDS2_CLK+
	DDI2_PAIR3-	D50		DP2_LANE3-	TMDS2_CLK-
	DDI2_HPD	D44		DP2_HPD	HDMI2_HPD
	DDI2_CTRLCLK_AUX+	C32		DP2_AUX+	HDMI2_CTRLCLK
	DDI2_CTRLDATA_AUX-	C33		DP2_AUX-	HDMI2_CTRLDATA
	DDI2_DDC_AUX_SEL	C34			
DDI 3	DDI3_PAIR0+	C39		DP3_LANE0+	TMDS3_DATA2+
	DDI3_PAIR0-	C40		DP3_LANE0-	TMDS3_DATA2-
	DDI3_PAIR1+	C42		DP3_LANE1+	TMDS3_DATA1+
	DDI3_PAIR1-	C43		DP3_LANE1-	TMDS3_DATA1-
	DDI3_PAIR2+	C46		DP3_LANE2+	TMDS3_DATA0+
	DDI3_PAIR2-	C47		DP3_LANE2-	TMDS3_DATA0-
	DDI3_PAIR3+	C49		DP3_LANE3+	TMDS3_CLK+
	DDI3_PAIR3-	C50		DP3_LANE3-	TMDS3_CLK-
	DDI3_HPD	C44		DP3_HPD	HDMI3_HPD
	DDI3_CTRLCLK_AUX+	C36		DP3_AUX+	HDMI3_CTRLCLK
	DDI3_CTRLDATA_AUX-	C37		DP3_AUX-	HDMI3_CTRLDATA
	DDI3_DDC_AUX_SEL	C38			

Table 4.20: Type 10 DDI

	Pin Name	Type 10 Pin Number	SDVO	DP	HDMI/DVI (TMDS Signaling)
DDI 0	DDI0_PAIR0+	B71	SDVO0_RED+	DP0_LANE0+	TMDS0_DATA2+
	DDI0_PAIR0-	B72	SDVO0_RED-	DP0_LANE0-	TMDS0_DATA2-
	DDI0_PAIR1+	B73	SDVO0_GRN+	DP0_LANE1+	TMDS0_DATA1+
	DDI0_PAIR1-	B74	SDVO0_GRN-	DP0_LANE1-	TMDS0_DATA1-
	DDI0_PAIR2+	B75	SDVO0_BLU+	DP0_LANE2+	TMDS0_DATA0+
	DDI0_PAIR2-	B76	SDVO0_BLU-	DP0_LANE2-	TMDS0_DATA0-
	DDI0_PAIR3+	B81	SDVO0_CK+	DP0_LANE3+	TMDS0_CLK+
	DDI0_PAIR3-	B82	SDVO0_CK-	DP0_LANE3-	TMDS0_CLK-
	DDI0_PAIR4+	B77	SDVO0_INT+		
	DDI0_PAIR4-	B78	SDVO0_INT-		
	DDI0_PAIR5+	B91	SDVO0_TVCLKIN+		
	DDI0_PAIR5-	B92	SDVO0_TVCLKIN-		
	DDI0_PAIR6+	B93	SDVO0_FLDSTALL+		
	DDI0_PAIR6-	B94	SDVO0_FLDSTALL-		
	DDI0_HPD	B89		DP0_HPD	HDMI0_HPD
	DDI0_CTRLCLK_AUX+	B98	SDVO0_CTRLCLK	DP0_AUX+	HMDI0_CTRLCLK
	DDI0_CTRLDATA_AUX-	B99	SDVO0_CTRLDATA	DP0_AUX-	HMDI0_CTRLDATA
	DDI0_DDC_AUX_SEL	B95			

4.3.16 DDI Signals: DisplayPort

Table 4.21: DisplayPort Signals, Pin Types, and Descriptions

DisplayPort	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
DP[1:3]_LANE[0:3]+ DP[1:3]_LANE[0:3]-	O PCIE	AC coupled off Module	Uni-directional main link for the transport of isochronous streams and secondary-data packets	T6
DP[1:3]_AUX+ DP[1:3]_AUX-	I/O PCIE	AC coupled on Module	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	T6
DP[1:3]_HPD	I CMOS	3.3V / 3.3V	Detection of Hot Plug / Unplug and notification of the link layer	T6
DP[0]_LANE[0:3]+ DP[0]_LANE[0:3]-	O PCIE	AC coupled off Module	Uni-directional main link for the transport of isochronous streams and secondary-data packets	T10
DP[0]_AUX+ DP[0]_AUX-	I/O PCIE	AC coupled on Module	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	T10
DP[0]_HPD	I CMOS	3.3V / 3.3V	Detection of Hot Plug / Unplug and notification of the link layer	T10

4.3.17 DDI Signals: SDVO

Table 4.22: SDVO Signals, Pin Types, and Descriptions

SDVO	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
SDVO1_RED+ SDVO1_RED-	O PCIE	AC coupled off Module	Serial Digital Video red output differential pair	T6
SDVO1_GRN+ SDVO1_GRN-	O PCIE	AC coupled off Module	Serial Digital Video green output differential pair	T6
SDVO1_BLU+ SDVO1_BLU-	O PCIE	AC coupled off Module	Serial Digital Video blue output differential pair	T6
SDVO1_CK+ SDVO1_CK-	O PCIE	AC coupled off Module	Serial Digital Video clock output differential pair.	T6
SDVO1_INT+ SDVO1_INT-	I PCIE	AC coupled off Module	Serial Digital Video interrupt input differential pair.	T6
SDVO1_TVCLKIN+ SDVO1_TVCLKIN-	I PCIE	AC coupled off Module	Serial Digital Video TVOUT synchronization clock input	T6
SDVO1_FLDSTALL+ SDVO1_FLDSTALL-	I PCIE	AC coupled off Module	Serial Digital Video Field Stall input differential pair.	T6
SDVO1_CTRLCLK	I/O OD CMOS	3.3V / 3.3V	SDVO I2C clock line - to set up SDVO peripherals.	T6
SDVO1_CTRLDATA	I/O OD CMOS	3.3V / 3.3V	SDVO I2C data line - to set up SDVO peripherals.	T6
SDVO0_RED+ SDVO0_RED-	O PCIE	AC coupled off Module	Serial Digital Video red output differential pair	T10
SDVO0_GRN+ SDVO0_GRN-	O PCIE	AC coupled off Module	Serial Digital Video green output differential pair	T10
SDVO0_BLU+ SDVO0_BLU-	O PCIE	AC coupled off Module	Serial Digital Video blue output differential pair	T10
SDVO0_CK+ SDVO0_CK-	O PCIE	AC coupled off Module	Serial Digital Video clock output differential pair.	T10
SDVO0_INT+ SDVO0_INT-	I PCIE	AC coupled off Module	Serial Digital Video interrupt input differential pair.	T10
SDVO0_TVCLKIN+ SDVO0_TVCLKIN-	I PCIE	AC coupled off Module	Serial Digital Video TVOUT synchronization clock input	T10
SDVO0_FLDSTALL+ SDVO0_FLDSTALL-	I PCIE	AC coupled off Module	Serial Digital Video Field Stall input differential pair.	T10
SDVO0_CTRLCLK	I/O OD CMOS	3.3V / 3.3V	SDVO I2C clock line - to set up SDVO peripherals.	T10
SDVO0_CTRLDATA	I/O OD CMOS	3.3V / 3.3V	SDVO I2C data line - to set up SDVO peripherals.	T10

4.3.18 DDI Signals: HDMI / DVI

Table 4.23: HDMI/DVI Signals, Pin Types, and Descriptions

HDMI	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
TMDS[1:3]_CLK+ TMDS[1:3]_CLK-	O PCIE	AC coupled off Module	HDMI/DVI TMDS Clock differential pair	T6
TMDS[1:3]_DATA[0:2]+ TMDS[1:3]_DATA[0:2]-	O PCIE	AC coupled off Module	HDMI/DVI TMDS lanes 0, 1 and 2 differential pairs	T6
HDMI[1:3]_CTRL_CLK	I/O OD CMOS	3.3V / 3.3V	HDMI/DVI I2C control clock	T6
HDMI[1:3]_CTRL_DAT	I/O OD CMOS	3.3V / 3.3V	HDMI/DVI I2C control data	T6
HDMI[1:3]_HPD	I	3.3V / 3.3V	HDMI/DVI Hot-Plug Detect	T6
TMDS[0]_CLK+ TMDS[0]_CLK-	O PCIE	AC coupled off Module	HDMI/DVI TMDS Clock differential pair	T10
TMDS[0]_DATA[0:2]+ TMDS[0]_DATA[0:2]-	O PCIE	AC coupled off Module	HDMI/DVI TMDS lanes 0, 1 and 2 differential pairs	T10
HDMI[0]_CTRL_CLK	I/O OD CMOS	3.3V / 3.3V	HDMI/DVI I2C control clock	T10
HDMI[0]_CTRL_DAT	I/O OD CMOS	3.3V / 3.3V	HDMI/DVI I2C control data	T10
HDMI[0]_HPD	I	3.3V / 3.3V	HDMI/DVI Hot-Plug Detect	T10

4.3.19 General Purpose Serial Interface

Two TTL compatible two wire ports are available on Module Types 6 and 10. This feature is introduced in COM.0 Revision 2 and uses pins on the A-B connector that have been re-claimed from the A-B VCC_12V pool. As such, it is possible that if a Type 6 or 10 Module is deployed in an R1.0 Carrier Board for Module Types 1,2,3,4,5 then the Module TTL level serial pins may be exposed to the 12V supply, and Module designers must plan for this. Similarly, an R1.0 Module deployed on an R2.0 Carrier may bridge 12V to the serial pins and Carrier designers must plan for this. These pins are designated SER0_TX, SER0_RX, SER1_TX and SER1_RX. Data out of the Module is on the _TX pins. Hardware handshaking and hardware flow control are not supported.

Any of the Module asynchronous serial ports, if implemented on an Intel X86 architecture Module platform, ***should*** be I/O mapped serial ports that are register compatible with the National Semiconductor 16550 UARTs that were used in the PC AT architecture.

The Module asynchronous serial ports are intended for general purpose use and for use with debugging software that make use of the “console redirect” features available in many operating systems. The Module asynchronous serial ports ***should not*** be implemented as USB peripherals, as such implementations are generally not useful for low level debug purposes.

The serial ports, if implemented, ***shall*** support standard asynchronous serial port bit rates up to and including 115.2 kbits/second.

Table 4.24: Serial Interface Signals (Type 10), Pin Types, and Descriptions

Serial	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
SER0_TX[8]	O CMOS	5V / 12V	General purpose serial port transmitter	T6, T10
SER0_RX[8]	I CMOS	5V / 12V	General purpose serial port receiver	T6, T10
SER1_TX[8]	O CMOS	5V / 12V	General purpose serial port transmitter This pin is shared with CAN_TX (refer to Section 4.3.30 'CAN Bus')	T6, T10
SER1_RX[8]	I CMOS	5V / 12V	General purpose serial port receiver This pin is shared with CAN_RX (refer to Section 4.3.30 'CAN Bus')	T6, T10

8 *These signals use reclaimed VCC_12V pins. Refer to Section 5.10 'Protecting COM.0 Pins Reclaimed From the VCC_12V Pool' for additional design considerations*

4.3.20 I2C Bus

The I2C port ***shall*** be available in addition to the SMBus. The I2C clock ***shall*** support 100kHz and ***should*** support 400kHz operation. The maximum capacitance on the Carrier Board ***shall*** not exceed 100pF. The I2C interface ***should*** support multi-master operation.[9] This capability will allow a Carrier to read an optional Module EEPROM before powering up the Module.

Revision 1.0 of the specification placed the I2C interface on the non-standby power domain. With this connection, the I2C interface can only be used when the Module is powered on. Since the I2C interface is used to connect to an optional Carrier EEPROM and since it is desirable to allow a Module based board controller access to the optional Carrier EEPROM before the Module is powered on, revision 2.0 of this specification changes the power domain of the I2C interface to standby-power allowing access during power down and suspend states. There is a possible leakage issue that can arise when using a R2.0 Module with a R1.0 Carrier that supports I2C devices. The R1.0 Carrier will power any I2C devices from the non-standby power rail. A R2.0 Module will pull-up the I2C clock and data lines to the standby-rail through a 2.2K resistor. The difference in the power domains on the Module and Carrier can provide a leakage path from the standby power rail to the non-standby power rail.

Table 4.25: I2C Signals, Pin Types, and Descriptions

I2C Bus	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
I2C_CK	I/O OD CMOS	3.3V Suspend/ 3.3V	General purpose I2C port clock output	All
I2C_DAT	I/O OD CMOS	3.3V Suspend/ 3.3V	General purpose I2C port data I/O line	All

9 *I2C multi-master support starts with COM Express Rev. 2.0*

4.3.21 Miscellaneous

Table 4.26: Misc Signals, Pin Types, and Descriptions

Miscellaneous	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
SPKR	O CMOS	3.3V / 3.3V	Output for audio enunciator - the "speaker" in PC-AT systems. This port provides the PC beep signal and is mostly intended for debugging purposes.	All
WDT	O CMOS	3.3V / 3.3V	Output indicating that a watchdog time-out event has occurred. Refer to Section 5.9 'Watchdog Timer' on page 119 for details.	All
KBD_RST#	I CMOS	3.3V / 3.3V	Input to Module from (optional) external keyboard controller that can force a reset. Pulled high on the Module. This is a legacy artifact of the PC-AT.	T1-5
KBD_A20GATE	I CMOS	3.3V / 3.3V	Input to Module from (optional) external keyboard controller that can be used to control the CPU A20 gate line. The A20GATE restricts the memory access to the bottom megabyte and is a legacy artifact of the PC-AT. Pulled high on the Module.	T1-5
FAN_PWMOUT[10]	O OD CMOS	3.3V / 12V	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	T6,T10
FAN_TACHIN[10]	I OD CMOS	3.3V / 12V	Fan tachometer input for a fan with a two pulse output.	T6,T10
TPM_PP[10]	I CMOS	3.3V / 3.3V	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	T6,T10

10 *These signals use reclaimed VCC_12V pins. Refer to Section 5.10 'Protecting COM.0 Pins Reclaimed From the VCC_12V Pool' for additional design considerations*

4.3.22 Power and System Management

Signals PWR_OK, SYS_RESET#, and CB_RESET# ***shall*** be supported for all Module pin-out types. Signal PCI_RESET# ***shall*** be supported for pin-out types 2 and 3. Signal IDE_RESET# ***shall*** be supported for pin-out types 2 and 4. Additionally, signal PWR_OK indicates that all the power supplies to the Module are stable within specified ranges and can be used to enable Module internal power supplies.

PWR_OK has been traditionally used to hold off a Module startup to allow devices on the Carrier such as FPGAs to initialize. The Module will typically not power up until the PWR_OK signal goes active. There is the potential for the Carrier to back drive voltages from the Carrier to the Module when the Carrier is powered but the Module is not. Designers of Modules and Carrier are encourage to follow the terminations as specified in Section 4.4 'Signals Requiring Carrier Board Termination'. The use of SYS_RESET# to hold off a Module startup may not produce the desired results since the behavior of SYS_RESET# is Module chipset dependent. In typical designs, the reset initiation happens on the falling edge of SYS_RESET# therefore holding the SYS_RESET# low will not result in preventing the Module for starting. PWR_OK ***should not*** be deactivated after the Module enters S0 unless there is a power fail condition.

Signals SUS_S3#, SUS_S4# and SUS_S5# defines the signaling to indicate that the Module has entered the ACPI power-saving mode S3 (Suspend-To-RAM or STR), S4 (Suspend-To-Disk or STD), or S5 (Soft-Off).

Table 4.27: Power and System Management Signals, Pin Types, and Descriptions

Power and System Management	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
PWRBTN#	I CMOS	3.3V Suspend/ 3.3V	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down.	All
SYS_RESET#	I CMOS	3.3V Suspend/ 3.3V	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle ***may*** be used.	All
CB_RESET#	O CMOS	3.3V Suspend/ 3.3V	Reset output from Module to Carrier Board. Active low. Issued by Module chipset and ***may*** result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or ***may*** be initiated by the Module software.	All
PWR_OK	I CMOS	3.3V / 3.3V	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed.	All
SUS_STAT#	O CMOS	3.3V Suspend/ 3.3V	Indicates imminent suspend operation; used to notify LPC devices.	All
SUS_S3#	O CMOS	3.3V Suspend/ 3.3V	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board ***may*** be used to enable the non-standby power on a typical ATX supply.	All
SUS_S4#	O CMOS	3.3V Suspend/ 3.3V	Indicates system is in Suspend to Disk state. Active low output.	All
SUS_S5#	O CMOS	3.3V Suspend/ 3.3V	Indicates system is in Soft Off state.	All
WAKE0#	I CMOS	3.3V Suspend/ 3.3V	PCI Express wake up signal.	All
WAKE1#	I CMOS	3.3V Suspend/ 3.3V	General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.	All
BATLOW#	I CMOS	3.3V Suspend/ 3.3V	Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.	All
LID#[11]	I OD CMOS	3.3V Suspend/ 12V	LID switch. Low active signal used by the ACPI operating system for a LID switch.	T6, T10
SLEEP#[11]	I OD CMOS	3.3V Suspend/ 12V	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	T6, T10

11 *These signals use reclaimed VCC_12V pins. Refer to Section 5.10 'Protecting COM.0 Pins Reclaimed From the VCC_12V Pool' for additional design considerations*

4.3.23 Thermal Protection

This port provides thermal signaling to protect critical components on the Module and the Carrier Board.

Table 4.28: Thermal Protection Signals, Pin Types, and Descriptions

Thermal Protection	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
THRM#	I CMOS	3.3V / 3.3V	Input from off-Module temp sensor indicating an over-temp situation.	All
THRMTRIP#	O CMOS	3.3V / 3.3V	Active low output indicating that the CPU has entered thermal shutdown.	All

4.3.24 SM Bus

The SMBus port is specified for system management functions. It is used on the Module to manage system functions such as reading the DRAM SPD EEPROM and setting clock synthesizer parameters. If the SMBus is used on the baseboard, then great care must be taken that no conflicts with the on-Module SMBus devices occur. It may be useful for implementation on the Carrier Board of standards such as Smart Battery. The maximum capacitance on the Carrier Board ***shall*** not exceed 100pF.

Table 4.29: SM Bus Signals, Pin Types, and Descriptions

SM Bus	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
SMB_CK	I/O OD CMOS	3.3V Suspend/ 3.3V	System Management Bus bidirectional clock line.	All
SMB_DAT	I/O OD CMOS	3.3V Suspend/ 3.3V	System Management Bus bidirectional data line.	All
SMB_ALERT#	I CMOS	3.3V Suspend/ 3.3V	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	All

4.3.25 General Purpose Input Output

GPI and GPO pins ***may*** be implemented as GPIO (Module specific). GPI and GPO pins ***may*** be implemented as SDIO (refer to Section 4.3.26 'SDIO'). If SDIO is supported the BIOS **may** be used to set the default state (SDIO or GPIO) of the GPIO.

Table 4.30: GPIO Signals, Pin Types, and Descriptions

General Purpose I/O	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
GPO[0:3]	O CMOS	3.3V / 3.3V	General purpose output pins. Upon a hardware reset, these outputs ***should*** be low.	All
GPI[0:3]	I CMOS	3.3V / 3.3V	General purpose input pins. Pulled high internally on the Module.	All

4.3.26 SDIO

Support for an SDIO interface is optional and added in R2.0. The SDIO signals are piggy-backed on the existing COM.0 General Purpose IO (GPIO) signals (refer to Section 4.3.25 'General Purpose Input Output'). An EEPROM bit is added so that the Carrier Board can define if the GPIO are used as GPIO or SDIO. The Module ***may*** use this information to allow boot from SDIO. Modules that support SDIO over GPIO ***shall*** implement the pin mapping based on the table below.

Table 4.31: SD card interface signals

COM Express Signal	SD card interface signals	Comments
GPI0	SD_DATA0	Bidirectional signal
GPI1	SD_DATA1	Bidirectional signal
GPI2	SD_DATA2	Bidirectional signal
GPI3	SD_DATA3	Bidirectional signal
GPO0	SD_CLK	Output from COM Ex, input to SD
GPO1	SD_CMD	Output from COM Ex, input to SD
GPO2	SD_WP	Input to COM Ex when used as SD_WP
GPO3	SD_CD#	Input to COM Ex when used as SD_CD#

Table 4.32: SDIO Signals, Pin Types, and Descriptions

SDIO	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
SDIO_CD#	I CMOS	3.3V / 3.3V	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present. Maps to GPO3; used as an input when used for SD card support	T6, T10
SDIO_CLK	O CMOS	3.3V / 3.3V	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz. Maps to GPO0.	T6, T10
SDIO_CMD	O CMOS	3.3V / 3.3V	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode. Maps to GPO1	T6, T10
SDIO_WP	I CMOS	3.3V / 3.3V	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards. Maps to GPO2; used as an input when used for SD card support	T6, T10
SDIO_DAT[0:3]	IO CMOS	3.3V / 3.3V	SDIO Data lines. These signals operate in push-pull mode. Maps to GPI[0:3]	T6, T10

4.3.27 Module Type Definition

Table 4.33: Module Type Signals, Pin Types, and Descriptions

Module Type Definition	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
TYPE[0:2]#	PDS		The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). For Pin-out Type 1 and Type 10, these pins are not present (X). TYPE2# TYPE1# TYPE0# X X X Pin-out Type 1 NC NC NC Pin-out Type 2 NC NC GND Pin-out Type 3 (no IDE) NC GND NC Pin-out Type 4 (no PCI) NC GND GND Pin-out Type 5 (no IDE, no PCI) GND NC NC Pin-out Type 6 (no IDE, no PCI) The Carrier Board ***should*** implement combinatorial logic that monitors the Module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible Module pin-out type is detected. The Carrier Board logic ***may*** also implement a fault indicator such as an LED.	T2, T3, T4, T5, T6
TYPE10#	PDS		Dual use pin. Indicates to the Carrier Board that a Type 10 Module is installed. Indicates to the Carrier that a Rev 1.0/2.0 Module is installed TYPE10# NC Pin-out R2.0 PD Pin-out Type 10 pull down to ground with 47K resistor 12V Pin-out R1.0 This pin is reclaimed from the VCC_12V pool. In R1.0 Modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no connect for types 1-6. A Carrier can detect a R1.0 Module by the presence of 12V on this pin. R2.0 Module types 1-6 will no connect this pin. Type 10 Modules ***shall*** pull this pin to ground through a 47K resistor.	All

4.3.28 Power and Ground

Table 4.34: Power Signals, Pin Types, and Descriptions

Power and GND	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
VCC_12V	Power		Primary power input: +12V nominal. Refer to Section 7 “Electrical Specifications“ for allowable input range. All available VCC_12V pins on the connector(s) ***shall*** be used.	All
VCC_5V_SBY	Power		Standby power input: +5.0V nominal. Refer to Section 7 “Electrical Specifications“ for allowable input range. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) ***shall*** be used. Only used for standby and suspend functions. ***May*** be left unconnected if these functions are not used in the system design.	All
VCC_RTC	Power		Real-time clock circuit-power input. Nominally +3.0V. Refer to Section 7 “Electrical Specifications“ for details.	All
GND	Power		Ground - DC power and signal and AC signal return path. All available GND connector pins ***shall*** be used and tied to Carrier Board GND plane.	All

4.3.29 eDP - Embedded DisplayPort

Type 6 and Type 10 Modules allow the LVDS channel A signals (refer to Section 4.3.10 'LVDS Flat Panel') to be alternatively used for eDP. The manner in which LVDS or eDP operation is chosen is vendor dependent.

Table 4.35: Module and Carrier Combinations Type 6 and Type 10 Modules

Module	Carrier / Panel Adapter Requirements	Destination
eDP only	None - Straight through to eDP Header	eDP
	N/A – not a valid combination	LVDS
LVDS only	N/A – not a valid combination	eDP
	None - Straight through to LVDS receptacle	LVDS
Dual Mode	None - Straight through to eDP receptacle	eDP
	None – Straight through to LVDS receptacle	LVDS

Requirements

Module LVDS Channel A/eDP ***may*** support any combination of LVDS and eDP.

Module LVDS Channel A/eDP ***may*** support Dual Mode.

Module that support Dual-Mode ***shall*** implement the necessary muxing circuitry and control logic to ensure that the Module works properly with Carriers expecting either eDP or LVDS.

Table 4.36: **eDP** Signals

eDP	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
eDP_TX[0:3]+ eDP_TX[0:3]-	O PCIE	AC coupled off Module	eDP differential pairs	T6, T10
eDP _VDD_EN	O CMOS	3.3V / 3.3V	eDP power enable	T6,T10
eDP _BKLT_EN	O CMOS	3.3V / 3.3V	eDP backlight enable	T6,T10
eDP _BKLT_CTRL	O CMOS	3.3V / 3.3V	eDP backlight brightness control	T6,T10
eDP _AUX+	I/O PCIE	AC coupled off Module	eDP AUX+	T6,T10
eDP _AUX-	I/O PCIE	AC coupled off Module	eDP AUX-	T6,T10
eDP_HPD	I CMOS	3.3V / 3.3V	Detection of Hot Plug / Unplug and notification of the link layer	T6,T10

The off Module AC coupling of the eDP signals makes dual LVDS/eDP Module implementations easier.

Table 4.37: LVDS / eDP Pin Assignment

Pin Name	Type 6/10 Pin Number	eDP
LVDS_A0+	A71	eDP_TX2+
LVDS_A0-	A72	eDP_TX2-
LVDS_A1+	A73	eDP_TX1+
LVDS_A1-	A74	eDP_TX1-
LVDS_A2+	A75	eDP_TX0+
LVDS_A2-	A76	eDP_TX0-
LVDS_A_CK+	A81	eDP_TX3+
LVDS_A_CK-	A82	eDP_TX3-
LVDS_VDD_EN	A77	eDP_VDD_EN
LVDS_BKLT_EN	B79	eDP_BKLT_EN
LVDS_I2C_CK	A83	eDP_AUX+
LVDS_I2C_DAT	A84	eDP_AUX-
LVDS_BKLT_CTRL	B83	eDP_BKLT_CTRL
RSVD	A87	eDP_HPD

4.3.30 CAN Bus

CAN Bus Operation Over SER1 Lines

The SER1_TX and SER1_RX asynchronous serial port lines defined for COM.0 Types 6 and 10 ***may*** be used alternatively to carry CMOS 3.3V logic level CAN (Controller Area Network) bus signals from a COM Express Module based CAN protocol controller. The CAN bus is an asynchronous, message based protocol widely used in the automotive and industrial control sectors. It is defined by ISO 11519, ISO 11898, and SAEJ2411. Data rates on a CAN bus ***may*** be as high as 1 MBit/s, although lower rates in the range from 10 kBit/s to 125 kBit/s are more common.

Use of the CAN bus in a COM Express system requires a CAN bus transceiver on the Carrier Board to interface to the CAN physical layer. CAN bus transceivers are available from NXP, Texas Instruments, Linear Technology, and others.

Data from the COM Express Module based CAN controller to the Carrier Board CAN transceiver is carried on Module line SER1_TX. Data from the Carrier Board CAN transceiver to the COM Express Module based CAN controller is carried on Module line SER1_RX. The Carrier Board CAN transceiver converts the logic level CAN protocol TX and RX signals from the Module into a differential half duplex line per the CAN specification.

How the SER1 asynchronous lines are shared with CAN bus operation is Module vendor specific. A vendor ***may*** choose to use the SER1 TX and RX lines to support asynchronous serial port operation, or CAN bus operation, or both, or neither. Module build option(s) or software controlled muxing implementations ***may*** be used.

Table 4.38: CAN Bus Signals

CAN Bus	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
CAN_TX	O CMOS	3.3V / 3.3V	CAN (Controller Area Network) TX output for CAN Bus channel 0. This pin is shared with SER1_TX (refer to Section 4.3.19 'General Purpose Serial Interface')	T6, T10
CAN_RX	I CMOS	3.3V / 3.3V	RX input for CAN Bus channel 0. This pin is shared with SER1_RX (refer to Section 4.3.19 'General Purpose Serial Interface')	T6, T10

4.4 Signals Requiring Carrier Board Termination

Some signals, detailed below, require Carrier Board termination for proper operation. If the signals and the feature are not used, no Carrier Board termination is required, and the pins ***may*** be left open.

4.4.1 Ethernet

External Ethernet magnetics ***shall*** be implemented on the Carrier Board.

4.4.2 Analog VGA

If analog VGA is used, the VGA_RED, VGA_GRN, and VGA_BLU signals ***shall*** each be terminated on the Carrier Board through a 150Ω resistor to ground. These resistors ***should*** be placed close to the VGA connector on the Carrier Board. These lines ***may*** be left unterminated if the analog VGA function is not used.

4.4.3 LVDS

The LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-. LVDS_A_CK+/-, LVDS_B_CK+/-) ***shall*** have 100Ω terminations across the pairs at the destination. These terminations ***may*** be on the Carrier Board if the Carrier Board implements a LVDS de-serializer on-board.

Unused LVDS lines ***may*** be left open.

4.4.4 USB

No termination is required on USB pairs. A common mode choke is advisable if USB pairs on the Carrier Board are routed to a connector for use with an external cable.

Signals USB_0_1_OC#, USB_2_3_OC#, USB_4_5_OC# and USB_6_7_OC# are used to flag a USB over-current situation. Carrier Board USB current monitors ***may*** pull these lines to GND with open drain drivers to indicate that the monitor's current limit has been exceeded. Do not pull up these lines to 3.3V on the Carrier Board – this ***shall*** be done on the Module (Section 4.5.2).

If a USB 2.0 Debug port is present it ***should*** be routed to port 0.

4.4.5 SDVO (Types 2-5)

When implementing SDVO devices on the Carrier Board, the SDVO_CLK and SDVO_DATA lines ***shall*** have pull-up resistors to 2.5V +/- 5%. The resistor value ***should*** be 3.5kΩ. When implementing slots for SDVO cards on the Carrier Board, the pull-up resistors ***shall not*** be placed on the Carrier Board because add-on SDVO cards have pull-up resistors. The pull-up resistors on the SDVO_CLK and SDVO_DATA allow the Module chipset to determine that the pins shared between PCI Express Graphics and SDVO are to be used for SDVO. The following signals require AC coupling on the Carrier Board:

- SDVOB_INT+/-
- SDVOC_INT+/-
- SDVO_TVCLKIN+/-
- SDVO_FLDSTALL+/-

4.4.6 Digital Display Interfaces (DDI)

The Carrier based termination requirements are dependent on the video interfaces supported by the Module's DDI implementation as well as the display type connected to the Carrier. A DDI can be used to support one or more of the following interfaces: SDVO, DP, TMDS(DVI/HDMI), or Dual-Mode (DisplayPort and TMDS). Refer to the VESA DisplayPort Interoperability Guideline Version 1.1a dated February 5, 2009 available at the VESA website after registration http://www.vesa.org/vesa-standards/ for more information on supporting TMDS (DVI/HDMI) from a Dual-Mode Module.

Carriers that support TMDS (DVI/HDMI):

- DDI[n]_DDC_AUX_SEL ***shall*** be pulled to 3.3V on the Carrier with a 100K Ohm resistor to configure the DDI[n]_AUX pair as the DDC channel.
- Bi-directional level translators ***shall*** be placed on the Carrier DDI[n]_CTRLDATA_AUX- and DDI[n]_CTRLCLK_AUX+ to convert the 3.3V DDC channel on the Module to the 5V DDC channel for the TMDS display.
- Pull-up resistors ***shall*** be placed on the Carrier from 3.3V (Module side of level translator) and 5V (display side of level translator) and the [n]_CTRLDATA_AUX- and DDI[n]_CTRLCLK_AUX+ signals. The pull-up resistor ***should*** be 2k.
- Level translators ***may*** be placed on the DDI[n]_PAIR[0:3] signals if required by Module silicon. If such level translators are implemented, they shall be placed on the Carrier Board.
- Some Modules ***may*** require DC blocking capacitors on DDI[n]_PAIR[0:3]. If DC blocking capacitors are required by the DDI generating silicon, the DC blocking capacitors ***shall*** be placed on the Carrier.
- The Carrier ***shall*** include a blocking FET on DDI[n]_HPD to prevent back-drive current from damaging the Module.

Carriers that support DisplayPort (DisplayPort only or dual mode):

- Carrier DDI[n]_DDC_AUX_SEL ***should*** be connected to pin 13 of the DisplayPort connector to enable Modules that can support a Dual-Mode DisplayPort interface.
- DC blocking capacitors ***shall*** be placed on the Carrier for the DDI[n]_PAIR[0:3] signals.
- The Carrier ***shall*** include a blocking FET on DDI[n]_HPD to prevent back-drive current from damaging the Module.

Carriers that support SDVO:

- DDI[n]_DDC_AUX_SEL ***shall*** be pulled to 3.3V on the Carrier with a 100K Ohm resistor to configure the DDI[n]_AUX pair as the DDC channel.
- DC blocking capacitors ***shall*** be placed on the Carrier for the SDVO RED, GRN, BLU, CK, INT, TVCLKIN, and FLDSTALL signals.

4.4.7 VCC_RTC

To implement the RTC Battery according to the Underwriters Laboratories Inc® (UL) guidelines, battery cells must be protected against a reverse current going to the cell. This can be done by either a series Schottky diode or a series resistor. Revision 1.0 of this specification did not specify the location of this diode and the location was vendor implementation specific. For revision 2.0 Carrier Boards, a protection diode or a series

resistor ***shall*** be placed on the Carrier Board. For backwards compatibility, a revision 2.0 Module ***may*** also implement the protection diode.

4.5 Signals Requiring Module Termination

The signals below require Module termination if used. They are mentioned to provide guidance to both the Module and Carrier designer. These terminations defined below ***may*** be omitted if the feature is not implemented on the Module.

4.5.1 AC coupled on the Module

The following signals ***shall*** be AC coupled on the Module.

- SDVO[B:C]_RED+/-
- SDVO[B:C]_GRN+/-
- SDVO[B:C]_BLU+/-
- SDVO[B:C]_CK+/-
- SATA[0:3]TX+/-
- SATA[0:3]RX+/-
- PCIE_TX[0:31]+/-
- PEG_TX[0:15]+/-
- USB_SSTX[0:3]+/-

4.5.2 Misc

The Module ***shall*** provide the termination for the signals below. The following signals ***should*** be pulled-up to 3.3V with a 2.2kΩ resistor

- LVDS_I2C_CK
- LVDS_I2C_DAT
- VGA_I2C_CK
- VGA_I2C_DAT

The Module ***shall*** provide the termination for the signals below. The following signals ***should*** be pulled-up to 3.3V with a 4.7kΩ resistor

- IDE_IORDY

The Module ***shall*** provide the termination for the signals below. The following signals ***should*** be pulled-up to 3.3V with a 8.2kΩ resistor

- PCI_IRQ[A:D]#
- PCI_IRDY#
- PCI_LOCK#
- PCI_PERR#
- PCI_REQ[0:3]#
- PCI_SERR#
- PCI_STOP#
- PCI_TRDY#
- PCI_FRAME#
- PCI_CLKRUN#
- LPC_SERIRQ

The Module ***shall*** provide the termination for the signals below. The following signals ***should*** be pulled-up to 3.3V with a 10kΩ resistor

- KBD_A20GATE
- KBD_RST#
- BIOS_DIS[0:1]#
- EXCD[0:1]_CPPE#
- FAN_TACHIN

The Module ***shall*** provide the termination for the signals below. The following signals ***should*** be pulled-up to 3.3V Standby with a 2.2kΩ resistor

- I2C_CK
- I2C_DAT
- SMB_CK
- SMB_DAT

The Module ***shall*** provide the termination for the signals below. The following signals ***should*** be pulled-up to 3.3V Standby with a 10kΩ resistor

- USB_[0,2,4,6]_[1,3,5,7]_OC#
- SYS_RESET#
- BATLOW#
-
- WAKE0#
- WAKE1#
- PCI_PME#
- PWRBTN#
- SLEEP#
- LID#

Module termination of IDE_IRQ is dependent on the controller used. The Module ***shall*** provide the necessary termination.

When supporting Carrier Board based SPI devices, the SPI_MISO line ***shall*** have a series resistor of 33Ω.

Modules implementing a TPM ***shall*** pull down TPM_PP. The value of the pull down resistor will be Module specific. Carrier Boards that support TPM ***should*** drive this signal to 3.3V when TPM features that require physical presence detection are implemented.

The PWR_OK signal ***should*** be terminated by the Module designer. If the signal is driven low by the Carrier Board the Module power supplies do not start. If the signal is floated or driven to 3.3V logic high by the Carrier Board, and Module hardware determines that the incoming power is good then the Module power supplies proceed with their start up.

4.6 Pin-out Tables

Pin-out information for Module pin-out Types 1-6 and 10 are provided in the seven tables on the following pages.

4.6.1 Type 1

Module Pin-out Type 1 implements a single 220 pin connector and a minimal feature set including up to 6 PCI Express lanes, up to 8 USB, up to 4 SATA, LPC, LVDS, analog VGA, SPI, power management and miscellaneous functions. Modules implementing Pin-out Type 1 ***shall*** use the pin-out shown in this table. Refer to Table 3.2 for minimum requirements and Table 3.4 for the order in which interfaces ***shall*** be implemented.

Table 4.39: Pin List for Pin-out Type 1

Pin	Row A	Row B
1	GND(FIXED)	GND(FIXED)
2	GBE0_MDI3-	GBE0_ACT#
3	GBE0_MDI3+	LPC_FRAME#
4	GBE0_LINK100#	LPC_AD0
5	GBE0_LINK1000#	LPC_AD1
6	GBE0_MDI2-	LPC_AD2
7	GBE0_MDI2+	LPC_AD3
8	GBE0_LINK#	LPC_DRQ0#
9	GBE0_MDI1-	LPC_DRQ1#
10	GBE0_MDI1+	LPC_CLK
11	GND(FIXED)	GND(FIXED)
12	GBE0_MDI0-	PWRBTN#
13	GBE0_MDI0+	SMB_CK
14	GBE0_CTREF	SMB_DAT
15	SUS_S3#	SMB_ALERT#
16	SATA0_TX+	SATA1_TX+
17	SATA0_TX-	SATA1_TX-
18	SUS_S4#	SUS_STAT#
19	SATA0_RX+	SATA1_RX+
20	SATA0_RX-	SATA1_RX-
21	GND(FIXED)	GND(FIXED)
22	SATA2_TX+	SATA3_TX+
23	SATA2_TX-	SATA3_TX-
24	SUS_S5#	PWR_OK
25	SATA2_RX+	SATA3_RX+
26	SATA2_RX-	SATA3_RX-
27	BATLOW#	WDT
28	(S)ATA_ACT#	AC/HDA_SDIN2
29	AC/HDA_SYNC	AC/HDA_SDIN1
30	AC/HDA_RST#	AC/HDA_SDIN0
31	GND(FIXED)	GND(FIXED)
32	AC/HDA_BITCLK	SPKR
33	AC/HDA_SDOUT	I2C_CK
34	BIOS_DIS0#	I2C_DAT
35	THRMTRIP#	THRM#
36	USB6-	USB7-
37	USB6+	USB7+

Pin	Row A	Row B
38	USB_6_7_OC#	USB_4_5_OC#
39	USB4-	USB5-
40	USB4+	USB5+
41	GND(FIXED)	GND(FIXED)
42	USB2-	USB3-
43	USB2+	USB3+
44	USB_2_3_OC#	USB_0_1_OC#
45	USB0-	USB1-
46	USB0+	USB1+
47	VCC_RTC	EXCD1_PERST#
48	EXCD0_PERST#	EXCD1_CPPE#
49	EXCD0_CPPE#	SYS_RESET#
50	LPC_SERIRQ	CB_RESET#
51	GND(FIXED)	GND(FIXED)
52	PCIE_TX5+	PCIE_RX5+
53	PCIE_TX5-	PCIE_RX5-
54	GPI0	GPO1
55	PCIE_TX4+	PCIE_RX4+
56	PCIE_TX4-	PCIE_RX4-
57	GND	GPO2
58	PCIE_TX3+	PCIE_RX3+
59	PCIE_TX3-	PCIE_RX3-
60	GND(FIXED)	GND(FIXED)
61	PCIE_TX2+	PCIE_RX2+
62	PCIE_TX2-	PCIE_RX2-
63	GPI1	GPO3
64	PCIE_TX1+	PCIE_RX1+
65	PCIE_TX1-	PCIE_RX1-
66	GND	WAKE0#
67	GPI2	WAKE1#
68	PCIE_TX0+	PCIE_RX0+
69	PCIE_TX0-	PCIE_RX0-
70	GND(FIXED)	GND(FIXED)
71	LVDS_A0+	LVDS_B0+
72	LVDS_A0-	LVDS_B0-
73	LVDS_A1+	LVDS_B1+
74	LVDS_A1-	LVDS_B1-
75	LVDS_A2+	LVDS_B2+
76	LVDS_A2-	LVDS_B2-
77	LVDS_VDD_EN	LVDS_B3+
78	LVDS_A3+	LVDS_B3-
79	LVDS_A3-	LVDS_BKLT_EN
80	GND(FIXED)	GND(FIXED)
81	LVDS_A_CK+	LVDS_B_CK+
82	LVDS_A_CK-	LVDS_B_CK-
83	LVDS_I2C_CK	LVDS_BKLT_CTRL
84	LVDS_I2C_DAT	VCC_5V_SBY
85	GPI3	VCC_5V_SBY
86	KBD_RST#	VCC_5V_SBY

Pin	Row A	Row B
87	KBD_A20GATE	VCC_5V_SBY
88	PCIE_CLK_REF+	BIOS_DIS1#
89	PCIE_CLK_REF-	VGA_RED
90	GND(FIXED)	GND(FIXED)
91	SPI_POWER	VGA_GRN
92	SPI_MISO	VGA_BLU
93	GPO0	VGA_HSYNC
94	SPI_CLK	VGA_VSYNC
95	SPI_MOSI	VGA_I2C_CK
96	GND	VGA_I2C_DAT
97	TYPE10#	SPI_CS#
98	RSVD[12]	RSVD[12]
99	RSVD[12]	RSVD[12]
100	GND(FIXED)	GND(FIXED)
101	RSVD[12]	RSVD[12]
102	RSVD[12]	RSVD[12]
103	RSVD[12]	RSVD[12]
104	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V
109	VCC_12V	VCC_12V
110	GND(FIXED)	GND(FIXED)

12 *RSVD pins are reserved for future use and* ***should*** *be no connect. Do not tie the RSVD pins together.*

4.6.2 Type 10

Module Pin-out Type 10 implements a single 220 pin connector and a minimal feature set including up to 4 PCI Express lanes, up to 2 USB SuperSpeed, up to 8 USB, a USB client host detect, up to 2 SATA, LPC, single LVDS, 1 DDI, SPI, power management and miscellaneous functions. Modules implementing Pin-out Type 10 ***shall*** use the pin-out shown in this table. Refer to Table 3.2 for minimum requirements and Table 3.4 for the order in which interfaces ***shall*** be implemented.

Table 4.40: Pin List for Pin-out Type 10

Pin	Row A	Row B
1	GND(FIXED)	GND(FIXED)
2	GBE0_MDI3-	GBE0_ACT#
3	GBE0_MDI3+	LPC_FRAME#
4	GBE0_LINK100#	LPC_AD0
5	GBE0_LINK1000#	LPC_AD1
6	GBE0_MDI2-	LPC_AD2
7	GBE0_MDI2+	LPC_AD3
8	GBE0_LINK#	LPC_DRQ0#
9	GBE0_MDI1-	LPC_DRQ1#
10	GBE0_MDI1+	LPC_CLK
11	GND(FIXED)	GND(FIXED)
12	GBE0_MDI0-	PWRBTN#
13	GBE0_MDI0+	SMB_CK
14	GBE0_CTREF	SMB_DAT
15	SUS_S3#	SMB_ALERT#
16	SATA0_TX+	SATA1_TX+
17	SATA0_TX-	SATA1_TX-
18	SUS_S4#	SUS_STAT#
19	SATA0_RX+	SATA1_RX+
20	SATA0_RX-	SATA1_RX-
21	GND(FIXED)	GND(FIXED)
22	USB_SSRX0-	USB_SSTX0-
23	USB_SSRX0+	USB_SSTX0+
24	SUS_S5#	PWR_OK
25	USB_SSRX1-	USB_SSTX1-
26	USB_SSRX1+	USB_SSTX1+
27	BATLOW#	WDT
28	(S)ATA_ACT#	AC/HDA_SDIN2
29	AC/HDA_SYNC	AC/HDA_SDIN1
30	AC/HDA_RST#	AC/HDA_SDIN0
31	GND(FIXED)	GND(FIXED)
32	AC/HDA_BITCLK	SPKR
33	AC/HDA_SDOUT	I2C_CK
34	BIOS_DIS0#	I2C_DAT
35	THRMTRIP#	THRM#
36	USB6-	USB7-
37	USB6+	USB7+
38	USB_6_7_OC#	USB_4_5_OC#
39	USB4-	USB5-
40	USB4+	USB5+

Pin	Row A	Row B
41	GND(FIXED)	GND(FIXED)
42	USB2-	USB3-
43	USB2+	USB3+
44	USB_2_3_OC#	USB_0_1_OC#
45	USB0-	USB1-
46	USB0+	USB1+
47	VCC_RTC	EXCD1_PERST#
48	EXCD0_PERST#	EXCD1_CPPE#
49	EXCD0_CPPE#	SYS_RESET#
50	LPC_SERIRQ	CB_RESET#
51	GND(FIXED)	GND(FIXED)
52	RSVD[13]	RSVD[13]
53	RSVD[13]	RSVD[13]
54	GPI0	GPO1
55	RSVD[13]	RSVD[13]
56	RSVD[13]	RSVD[13]
57	GND	GPO2
58	PCIE_TX3+	PCIE_RX3+
59	PCIE_TX3-	PCIE_RX3-
60	GND(FIXED)	GND(FIXED)
61	PCIE_TX2+	PCIE_RX2+
62	PCIE_TX2-	PCIE_RX2-
63	GPI1	GPO3
64	PCIE_TX1+	PCIE_RX1+
65	PCIE_TX1-	PCIE_RX1-
66	GND	WAKE0#
67	GPI2	WAKE1#
68	PCIE_TX0+	PCIE_RX0+
69	PCIE_TX0-	PCIE_RX0-
70	GND(FIXED)	GND(FIXED)
71	LVDS_A0+	DDI0_PAIR0+
72	LVDS_A0-	DDI0_PAIR0-
73	LVDS_A1+	DDI0_PAIR1+
74	LVDS_A1-	DDI0_PAIR1-
75	LVDS_A2+	DDI0_PAIR2+
76	LVDS_A2-	DDI0_PAIR2-
77	LVDS_VDD_EN	DDI0_PAIR4+
78	LVDS_A3+	DDI0_PAIR4-
79	LVDS_A3-	LVDS_BKLT_EN
80	GND(FIXED)	GND(FIXED)
81	LVDS_A_CK+	DDI0_PAIR3+
82	LVDS_A_CK-	DDI0_PAIR3-
83	LVDS_I2C_CK	LVDS_BKLT_CTRL
84	LVDS_I2C_DAT	VCC_5V_SBY
85	GPI3	VCC_5V_SBY
86	RSVD[13]	VCC_5V_SBY
87	eDP_HPD	VCC_5V_SBY

13 RSVD pins are reserved for future use and ***should*** be no connect. Do not tie the RSVD pins together.

Pin	Row A	Row B
88	PCIE_CLK_REF+	BIOS_DIS1#
89	PCIE_CLK_REF-	DD0_HPD
90	GND(FIXED)	GND(FIXED)
91	SPI_POWER	DDI0_PAIR5+
92	SPI_MISO	DDI0_PAIR5-
93	GPO0	DDI0_PAIR6+
94	SPI_CLK	DDI0_PAIR6-
95	SPI_MOSI	DDI0_DDC_AUX_SEL
96	TPM_PP	USB_HOST_PRSNT
97	TYPE10#	SPI_CS#
98	SER0_TX	DDI0_CTRLCLK_AUX+
99	SER0_RX	DDI0_CTRLDATA_AUX-
100	GND(FIXED)	GND(FIXED)
101	SER1_TX	FAN_PWMOUT
102	SER1_RX	FAN_TACHIN
103	LID#	SLEEP#
104	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V
109	VCC_12V	VCC_12V
110	GND(FIXED)	GND(FIXED)

4.6.3 Type 2

Type 2 includes PCI, IDE, a single GBE, up to 22 general-purpose PCIE lanes (PCIE 0-5 and PCIE 16-31). For most Type 2 implementations, it is expected that PCIE lanes 16-31 are used for graphics. Hence they are designated PEG lanes 0-15 in this table. Modules implementing Pin-out Type 2 ***shall*** use the pin-out shown in this table. Refer to Table 3.2 for minimum requirements and Table 3.4 for the order in which interfaces ***shall*** be implemented.

Table 4.41: Pin List for Pin-out Type 2

Pin	Row A	Row B	Row C	Row D
1	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
2	GBE0_MDI3-	GBE0_ACT#	IDE_D7	IDE_D5
3	GBE0_MDI3+	LPC_FRAME#	IDE_D6	IDE_D10
4	GBE0_LINK100#	LPC_AD0	IDE_D3	IDE_D11
5	GBE0_LINK1000#	LPC_AD1	IDE_D15	IDE_D12
6	GBE0_MDI2-	LPC_AD2	IDE_D8	IDE_D4
7	GBE0_MDI2+	LPC_AD3	IDE_D9	IDE_D0
8	GBE0_LINK#	LPC_DRQ0#	IDE_D2	IDE_REQ
9	GBE0_MDI1-	LPC_DRQ1#	IDE_D13	IDE_IOW#
10	GBE0_MDI1+	LPC_CLK	IDE_D1	IDE_ACK#
11	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
12	GBE0_MDI0-	PWRBTN#	IDE_D14	IDE_IRQ
13	GBE0_MDI0+	SMB_CK	IDE_IORDY	IDE_A0
14	GBE0_CTREF	SMB_DAT	IDE_IOR#	IDE_A1
15	SUS_S3#	SMB_ALERT#	PCI_PME#	IDE_A2
16	SATA0_TX+	SATA1_TX+	PCI_GNT2#	IDE_CS1#
17	SATA0_TX-	SATA1_TX-	PCI_REQ2#	IDE_CS3#
18	SUS_S4#	SUS_STAT#	PCI_GNT1#	IDE_RESET#
19	SATA0_RX+	SATA1_RX+	PCI_REQ1#	PCI_GNT3#
20	SATA0_RX-	SATA1_RX-	PCI_GNT0#	PCI_REQ3#
21	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
22	SATA2_TX+	SATA3_TX+	PCI_REQ0#	PCI_AD1
23	SATA2_TX-	SATA3_TX-	PCI_RESET#	PCI_AD3
24	SUS_S5#	PWR_OK	PCI_AD0	PCI_AD5
25	SATA2_RX+	SATA3_RX+	PCI_AD2	PCI_AD7
26	SATA2_RX-	SATA3_RX-	PCI_AD4	PCI_C/BE0#
27	BATLOW#	WDT	PCI_AD6	PCI_AD9
28	(S)ATA_ACT#	AC/HDA_SDIN2	PCI_AD8	PCI_AD11
29	AC/HDA_SYNC	AC/HDA_SDIN1	PCI_AD10	PCI_AD13
30	AC/HDA_RST#	AC/HDA_SDIN0	PCI_AD12	PCI_AD15
31	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
32	AC/HDA_BITCLK	SPKR	PCI_AD14	PCI_PAR
33	AC/HDA_SDOUT	I2C_CK	PCI_C/BE1#	PCI_SERR#
34	BIOS_DIS0#	I2C_DAT	PCI_PERR#	PCI_STOP#
35	THRMTRIP#	THRM#	PCI_LOCK#	PCI_TRDY#
36	USB6-	USB7-	PCI_DEVSEL#	PCI_FRAME#
37	USB6+	USB7+	PCI_IRDY#	PCI_AD16
38	USB_6_7_OC#	USB_4_5_OC#	PCI_C/BE2#	PCI_AD18
39	USB4-	USB5-	PCI_AD17	PCI_AD20
40	USB4+	USB5+	PCI_AD19	PCI_AD22

Pin	Row A	Row B	Row C	Row D
41	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
42	USB2-	USB3-	PCI_AD21	PCI_AD24
43	USB2+	USB3+	PCI_AD23	PCI_AD26
44	USB_2_3_OC#	USB_0_1_OC#	PCI_C/BE3#	PCI_AD28
45	USB0-	USB1-	PCI_AD25	PCI_AD30
46	USB0+	USB1+	PCI_AD27	PCI_IRQC#
47	VCC_RTC	EXCD1_PERST#	PCI_AD29	PCI_IRQD#
48	EXCD0_PERST#	EXCD1_CPPE#	PCI_AD31	PCI_CLKRUN#
49	EXCD0_CPPE#	SYS_RESET#	PCI_IRQA#	PCI_M66EN
50	LPC_SERIRQ	CB_RESET#	PCI_IRQB#	PCI_CLK
51	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
52	PCIE_TX5+	PCIE_RX5+	PEG_RX0+	PEG_TX0+
53	PCIE_TX5-	PCIE_RX5-	PEG_RX0-	PEG_TX0-
54	GPI0	GPO1	TYPE0#	PEG_LANE_RV#
55	PCIE_TX4+	PCIE_RX4+	PEG_RX1+	PEG_TX1+
56	PCIE_TX4-	PCIE_RX4-	PEG_RX1-	PEG_TX1-
57	GND	GPO2	TYPE1#	TYPE2#
58	PCIE_TX3+	PCIE_RX3+	PEG_RX2+	PEG_TX2+
59	PCIE_TX3-	PCIE_RX3-	PEG_RX2-	PEG_TX2-
60	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
61	PCIE_TX2+	PCIE_RX2+	PEG_RX3+	PEG_TX3+
62	PCIE_TX2-	PCIE_RX2-	PEG_RX3-	PEG_TX3-
63	GPI1	GPO3	RSVD[14]	RSVD[14]
64	PCIE_TX1+	PCIE_RX1+	RSVD[14]	RSVD[14]
65	PCIE_TX1-	PCIE_RX1-	PEG_RX4+	PEG_TX4+
66	GND	WAKE0#	PEG_RX4-	PEG_TX4-
67	GPI2	WAKE1#	RSVD[14]	GND
68	PCIE_TX0+	PCIE_RX0+	PEG_RX5+	PEG_TX5+
69	PCIE_TX0-	PCIE_RX0-	PEG_RX5-	PEG_TX5-
70	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
71	LVDS_A0+	LVDS_B0+	PEG_RX6+	PEG_TX6+
72	LVDS_A0-	LVDS_B0-	PEG_RX6-	PEG_TX6-
73	LVDS_A1+	LVDS_B1+	SDVO_DATA	SDVO_CLK
74	LVDS_A1-	LVDS_B1-	PEG_RX7+	PEG_TX7+
75	LVDS_A2+	LVDS_B2+	PEG_RX7-	PEG_TX7-
76	LVDS_A2-	LVDS_B2-	GND	GND
77	LVDS_VDD_EN	LVDS_B3+	RSVD[14]	IDE_CBLID#
78	LVDS_A3+	LVDS_B3-	PEG_RX8+	PEG_TX8+
79	LVDS_A3-	LVDS_BKLT_EN	PEG_RX8-	PEG_TX8-
80	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
81	LVDS_A_CK+	LVDS_B_CK+	PEG_RX9+	PEG_TX9+
82	LVDS_A_CK-	LVDS_B_CK-	PEG_RX9-	PEG_TX9-
83	LVDS_I2C_CK	LVDS_BKLT_CTRL	RSVD[14]	RSVD[14]
84	LVDS_I2C_DAT	VCC_5V_SBY	GND	GND
85	GPI3	VCC_5V_SBY	PEG_RX10+	PEG_TX10+
86	KBD_RST#	VCC_5V_SBY	PEG_RX10-	PEG_TX10-
87	KBD_A20GATE	VCC_5V_SBY	GND	GND

14 *RSVD pins are reserved for future use and* ***should*** *be no connect. Do not tie the RSVD pins together.*

Pin	Row A	Row B	Row C	Row D
88	PCIE_CLK_REF+	BIOS_DIS1#	PEG_RX11+	PEG_TX11+
89	PCIE_CLK_REF-	VGA_RED	PEG_RX11-	PEG_TX11-
90	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
91	SPI_POWER	VGA_GRN	PEG_RX12+	PEG_TX12+
92	SPI_MISO	VGA_BLU	PEG_RX12-	PEG_TX12-
93	GPO0	VGA_HSYNC	GND	GND
94	SPI_CLK	VGA_VSYNC	PEG_RX13+	PEG_TX13+
95	SPI_MOSI	VGA_I2C_CK	PEG_RX13-	PEG_TX13-
96	GND	VGA_I2C_DAT	GND	GND
97	TYPE10#	SPI_CS#	RSVD[14]	PEG_ENABLE#
98	RSVD[14]	RSVD[14]	PEG_RX14+	PEG_TX14+
99	RSVD[14]	RSVD	PEG_RX14-	PEG_TX14-
100	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
101	RSVD[14]	RSVD[14]	PEG_RX15+	PEG_TX15+
102	RSVD[14]	RSVD[14]	PEG_RX15-	PEG_TX15-
103	RSVD[14]	RSVD[14]	GND	GND
104	VCC_12V	VCC_12V	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V	VCC_12V	VCC_12V
109	VCC_12V	VCC_12V	VCC_12V	VCC_12V
110	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)

4.6.4 Type 3

Type 3 reassigns IDE to two additional GBE ports. Modules implementing Pin-out Type 3 ***shall*** use the pin-out shown in this table. Refer to Table 3.2 for minimum requirements and Table 3.4 for the order in which interfaces ***shall*** be implemented.

Table 4.42: Pin List for Pin-out Type 3

Pin	Row A	Row B	Row C	Row D
1	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
2	GBE0_MDI3-	GBE0_ACT#	GBE1_ACT#	GBE2_ACT#
3	GBE0_MDI3+	LPC_FRAME#	GBE1_MDI3-	GBE2_MDI3-
4	GBE0_LINK100#	LPC_AD0	GBE1_MDI3+	GBE2_MDI3+
5	GBE0_LINK1000#	LPC_AD1	GBE1_LINK100#	GBE2_LINK100#
6	GBE0_MDI2-	LPC_AD2	GBE1_MDI2-	GBE2_MDI2-
7	GBE0_MDI2+	LPC_AD3	GBE1_MDI2+	GBE2_MDI2+
8	GBE0_LINK#	LPC_DRQ0#	GBE1_LINK1000#	GBE2_LINK1000#
9	GBE0_MDI1-	LPC_DRQ1#	GBE1_MDI1-	GBE2_MDI1-
10	GBE0_MDI1+	LPC_CLK	GBE1_MDI1+	GBE2_MDI1+
11	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
12	GBE0_MDI0-	PWRBTN#	GBE1_MDI0-	GBE2_MDI0-
13	GBE0_MDI0+	SMB_CK	GBE1_MDI0+	GBE2_MDI0+
14	GBE0_CTREF	SMB_DAT	GBE1_LINK#	GBE2_LINK#
15	SUS_S3#	SMB_ALERT#	PCI_PME#	GBE2_CTREF
16	SATA0_TX+	SATA1_TX+	PCI_GNT2#	RSVD[15]
17	SATA0_TX-	SATA1_TX-	PCI_REQ2#	RSVD[15]
18	SUS_S4#	SUS_STAT#	PCI_GNT1#	RSVD[15]
19	SATA0_RX+	SATA1_RX+	PCI_REQ1#	PCI_GNT3#
20	SATA0_RX-	SATA1_RX-	PCI_GNT0#	PCI_REQ3#
21	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
22	SATA2_TX+	SATA3_TX+	PCI_REQ0#	PCI_AD1
23	SATA2_TX-	SATA3_TX-	PCI_RESET#	PCI_AD3
24	SUS_S5#	PWR_OK	PCI_AD0	PCI_AD5
25	SATA2_RX+	SATA3_RX+	PCI_AD2	PCI_AD7
26	SATA2_RX-	SATA3_RX-	PCI_AD4	PCI_C/BE0#
27	BATLOW#	WDT	PCI_AD6	PCI_AD9
28	(S)ATA_ACT#	AC/HDA_SDIN2	PCI_AD8	PCI_AD11
29	AC/HDA_SYNC	AC/HDA_SDIN1	PCI_AD10	PCI_AD13
30	AC/HDA_RST#	AC/HDA_SDIN0	PCI_AD12	PCI_AD15
31	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
32	AC/HDA_BITCLK	SPKR	PCI_AD14	PCI_PAR
33	AC/HDA_SDOUT	I2C_CK	PCI_C/BE1#	PCI_SERR#
34	BIOS_DIS0#	I2C_DAT	PCI_PERR#	PCI_STOP#
35	THRMTRIP#	THRM#	PCI_LOCK#	PCI_TRDY#
36	USB6-	USB7-	PCI_DEVSEL#	PCI_FRAME#
37	USB6+	USB7+	PCI_IRDY#	PCI_AD16
38	USB_6_7_OC#	USB_4_5_OC#	PCI_C/BE2#	PCI_AD18
39	USB4-	USB5-	PCI_AD17	PCI_AD20
40	USB4+	USB5+	PCI_AD19	PCI_AD22
41	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)

15 *RSVD pins are reserved for future use and* ***should*** *be no connect. Do not tie the RSVD pins together.*

Pin	Row A	Row B	Row C	Row D
42	USB2-	USB3-	PCI_AD21	PCI_AD24
43	USB2+	USB3+	PCI_AD23	PCI_AD26
44	USB_2_3_OC#	USB_0_1_OC#	PCI_C/BE3#	PCI_AD28
45	USB0-	USB1-	PCI_AD25	PCI_AD30
46	USB0+	USB1+	PCI_AD27	PCI_IRQC#
47	VCC_RTC	EXCD1_PERST#	PCI_AD29	PCI_IRQD#
48	EXCD0_PERST#	EXCD1_CPPE#	PCI_AD31	PCI_CLKRUN#
49	EXCD0_CPPE#	SYS_RESET#	PCI_IRQA#	PCI_M66EN
50	LPC_SERIRQ	CB_RESET#	PCI_IRQB#	PCI_CLK
51	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
52	PCIE_TX5+	PCIE_RX5+	PEG_RX0+	PEG_TX0+
53	PCIE_TX5-	PCIE_RX5-	PEG_RX0-	PEG_TX0-
54	GPI0	GPO1	TYPE0#	PEG_LANE_RV#
55	PCIE_TX4+	PCIE_RX4+	PEG_RX1+	PEG_TX1+
56	PCIE_TX4-	PCIE_RX4-	PEG_RX1-	PEG_TX1-
57	GND	GPO2	TYPE1#	TYPE2#
58	PCIE_TX3+	PCIE_RX3+	PEG_RX2+	PEG_TX2+
59	PCIE_TX3-	PCIE_RX3-	PEG_RX2-	PEG_TX2-
60	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
61	PCIE_TX2+	PCIE_RX2+	PEG_RX3+	PEG_TX3+
62	PCIE_TX2-	PCIE_RX2-	PEG_RX3-	PEG_TX3-
63	GPI1	GPO3	RSVD[15]	RSVD[15]
64	PCIE_TX1+	PCIE_RX1+	RSVD[15]	RSVD[15]
65	PCIE_TX1-	PCIE_RX1-	PEG_RX4+	PEG_TX4+
66	GND	WAKE0#	PEG_RX4-	PEG_TX4-
67	GPI2	WAKE1#	RSVD[15]	GND
68	PCIE_TX0+	PCIE_RX0+	PEG_RX5+	PEG_TX5+
69	PCIE_TX0-	PCIE_RX0-	PEG_RX5-	PEG_TX5-
70	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
71	LVDS_A0+	LVDS_B0+	PEG_RX6+	PEG_TX6+
72	LVDS_A0-	LVDS_B0-	PEG_RX6-	PEG_TX6-
73	LVDS_A1+	LVDS_B1+	SDVO_DATA	SDVO_CLK
74	LVDS_A1-	LVDS_B1-	PEG_RX7+	PEG_TX7+
75	LVDS_A2+	LVDS_B2+	PEG_RX7-	PEG_TX7-
76	LVDS_A2-	LVDS_B2-	GND	GND
77	LVDS_VDD_EN	LVDS_B3+	RSVD[15]	RSVD[15]
78	LVDS_A3+	LVDS_B3-	PEG_RX8+	PEG_TX8+
79	LVDS_A3-	LVDS_BKLT_EN	PEG_RX8-	PEG_TX8-
80	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
81	LVDS_A_CK+	LVDS_B_CK+	PEG_RX9+	PEG_TX9+
82	LVDS_A_CK-	LVDS_B_CK-	PEG_RX9-	PEG_TX9-
83	LVDS_I2C_CK	LVDS_BKLT_CTRL	RSVD[15]	RSVD[15]
84	LVDS_I2C_DAT	VCC_5V_SBY	GND	GND
85	GPI3	VCC_5V_SBY	PEG_RX10+	PEG_TX10+
86	KBD_RST#	VCC_5V_SBY	PEG_RX10-	PEG_TX10-
87	KBD_A20GATE	VCC_5V_SBY	GND	GND
88	PCIE_CLK_REF+	BIOS_DIS1#	PEG_RX11+	PEG_TX11+
89	PCIE_CLK_REF-	VGA_RED	PEG_RX11-	PEG_TX11-
90	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)

Pin	Row A	Row B	Row C	Row D
91	SPI_POWER	VGA_GRN	PEG_RX12+	PEG_TX12+
92	SPI_MISO	VGA_BLU	PEG_RX12-	PEG_TX12-
93	GPO0	VGA_HSYNC	GND	GND
94	SPI_CLK	VGA_VSYNC	PEG_RX13+	PEG_TX13+
95	SPI_MOSI	VGA_I2C_CK	PEG_RX13-	PEG_TX13-
96	GND	VGA_I2C_DAT	GND	GND
97	TYPE10#	SPI_CS#	RSVD[15]	PEG_ENABLE#
98	RSVD	RSVD[15]	PEG_RX14+	PEG_TX14+
99	RSVD	RSVD[15]	PEG_RX14-	PEG_TX14-
100	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
101	RSVD[15]	RSVD[15]	PEG_RX15+	PEG_TX15+
102	RSVD[15]	RSVD[15]	PEG_RX15-	PEG_TX15-
103	RSVD[15]	RSVD[15]	GND	GND
104	VCC_12V	VCC_12V	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V	VCC_12V	VCC_12V
109	VCC_12V	VCC_12V	VCC_12V	VCC_12V
110	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)

4.6.5 Type 4

Type 4 reassigns PCI to create 10 additional PCIE lanes. PEG lanes 0-15 are renamed PCIE lanes 16-31. These lanes ***may*** be used as PEG lanes 0-15 or as general purpose PCIE lanes 16-31. Modules implementing Pin-out Type 4 ***shall*** use the pin-out shown in this table. Refer to Table 3.2 for minimum requirements and Table 3.4 for the order in which interfaces ***shall*** be implemented.

Table 4.43: Pin List for Pin-out Type 4

Pin	Row A	Row B	Row C	Row D
1	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
2	GBE0_MDI3-	GBE0_ACT#	IDE_D7	IDE_D5
3	GBE0_MDI3+	LPC_FRAME#	IDE_D6	IDE_D10
4	GBE0_LINK100#	LPC_AD0	IDE_D3	IDE_D11
5	GBE0_LINK1000#	LPC_AD1	IDE_D15	IDE_D12
6	GBE0_MDI2-	LPC_AD2	IDE_D8	IDE_D4
7	GBE0_MDI2+	LPC_AD3	IDE_D9	IDE_D0
8	GBE0_LINK#	LPC_DRQ0#	IDE_D2	IDE_REQ
9	GBE0_MDI1-	LPC_DRQ1#	IDE_D13	IDE_IOW#
10	GBE0_MDI1+	LPC_CLK	IDE_D1	IDE_ACK#
11	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
12	GBE0_MDI0-	PWRBTN#	IDE_D14	IDE_IRQ
13	GBE0_MDI0+	SMB_CK	IDE_IORDY	IDE_A0
14	GBE0_CTREF	SMB_DAT	IDE_IOR#	IDE_A1
15	SUS_S3#	SMB_ALERT#	RSVD[16]	IDE_A2
16	SATA0_TX+	SATA1_TX+	RSVD[16]	IDE_CS1#
17	SATA0_TX-	SATA1_TX-	RSVD[16]	IDE_CS3#
18	SUS_S4#	SUS_STAT#	RSVD[16]	IDE_RESET#
19	SATA0_RX+	SATA1_RX+	PCIE_RX6+	PCIE_TX6+
20	SATA0_RX-	SATA1_RX-	PCIE_RX6-	PCIE_TX6-
21	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
22	SATA2_TX+	SATA3_TX+	PCIE_RX7+	PCIE_TX7+
23	SATA2_TX-	SATA3_TX-	PCIE_RX7-	PCIE_TX7-
24	SUS_S5#	PWR_OK	RSVD[16]	RSVD[16]
25	SATA2_RX+	SATA3_RX+	RSVD[16]	RSVD[16]
26	SATA2_RX-	SATA3_RX-	PCIE_RX8+	PCIE_TX8+
27	BATLOW#	WDT	PCIE_RX8-	PCIE_TX8-
28	(S)ATA_ACT#	AC/HDA_SDIN2	RSVD[16]	RSVD[16]
29	AC/HDA_SYNC	AC/HDA_SDIN1	PCIE_RX9+	PCIE_TX9+
30	AC/HDA_RST#	AC/HDA_SDIN0	PCIE_RX9-	PCIE_TX9-
31	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
32	AC/HDA_BITCLK	SPKR	PCIE_RX10+	PCIE_TX10+
33	AC/HDA_SDOUT	I2C_CK	PCIE_RX10-	PCIE_TX10-
34	BIOS_DIS0#	I2C_DAT	RSVD[16]	RSVD[16]
35	THRMTRIP#	THRM#	RSVD[16]	RSVD[16]
36	USB6-	USB7-	PCIE_RX11+	PCIE_TX11+
37	USB6+	USB7+	PCIE_RX11-	PCIE_TX11-
38	USB_6_7_OC#	USB_4_5_OC#	RSVD[16]	RSVD[16]
39	USB4-	USB5-	PCIE_RX12+	PCIE_TX12+

16 *RSVD pins are reserved for future use and* ***should*** *be no connect. Do not tie the RSVD pins together.*

Pin	Row A	Row B	Row C	Row D
40	USB4+	USB5+	PCIE_RX12-	PCIE_TX12-
41	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
42	USB2-	USB3-	PCIE_RX13+	PCIE_TX13+
43	USB2+	USB3+	PCIE_RX13-	PCIE_TX13-
44	USB_2_3_OC#	USB_0_1_OC#	RSVD[16]	RSVD[16]
45	USB0-	USB1-	RSVD[16]	RSVD[16]
46	USB0+	USB1+	PCIE_RX14+	PCIE_TX14+
47	VCC_RTC	EXCD1_PERST#	PCIE_RX14-	PCIE_TX14-
48	EXCD0_PERST#	EXCD1_CPPE#	RSVD[16]	RSVD[16]
49	EXCD0_CPPE#	SYS_RESET#	PCIE_RX15+	PCIE_TX15+
50	LPC_SERIRQ	CB_RESET#	PCIE_RX15-	PCIE_TX15-
51	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
52	PCIE_TX5+	PCIE_RX5+	PCIE_RX16+	PCIE_TX16+
53	PCIE_TX5-	PCIE_RX5-	PCIE_RX16-	PCIE_TX16-
54	GPI0	GPO1	TYPE0#	PEG_LANE_RV#
55	PCIE_TX4+	PCIE_RX4+	PCIE_RX17+	PCIE_TX17+
56	PCIE_TX4-	PCIE_RX4-	PCIE_RX17-	PCIE_TX17-
57	GND	GPO2	TYPE1#	TYPE2#
58	PCIE_TX3+	PCIE_RX3+	PCIE_RX18+	PCIE_TX18+
59	PCIE_TX3-	PCIE_RX3-	PCIE_RX18-	PCIE_TX18-
60	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
61	PCIE_TX2+	PCIE_RX2+	PCIE_RX19+	PCIE_TX19+
62	PCIE_TX2-	PCIE_RX2-	PCIE_RX19-	PCIE_TX19-
63	GPI1	GPO3	RSVD[16]	RSVD[16]
64	PCIE_TX1+	PCIE_RX1+	RSVD[16]	RSVD[16]
65	PCIE_TX1-	PCIE_RX1-	PCIE_RX20+	PCIE_TX20+
66	GND	WAKE0#	PCIE_RX20-	PCIE_TX20-
67	GPI2	WAKE1#	RSVD[16]	GND
68	PCIE_TX0+	PCIE_RX0+	PCIE_RX21+	PCIE_TX21+
69	PCIE_TX0-	PCIE_RX0-	PCIE_RX21-	PCIE_TX21-
70	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
71	LVDS_A0+	LVDS_B0+	PCIE_RX22+	PCIE_TX22+
72	LVDS_A0-	LVDS_B0-	PCIE_RX22-	PCIE_TX22-
73	LVDS_A1+	LVDS_B1+	SDVO_DATA	SDVO_CLK
74	LVDS_A1-	LVDS_B1-	PCIE_RX23+	PCIE_TX23+
75	LVDS_A2+	LVDS_B2+	PCIE_RX23-	PCIE_TX23-
76	LVDS_A2-	LVDS_B2-	GND	GND
77	LVDS_VDD_EN	LVDS_B3+	RSVD[16]	IDE_CBLID#
78	LVDS_A3+	LVDS_B3-	PCIE_RX24+	PCIE_TX24+
79	LVDS_A3-	LVDS_BKLT_EN	PCIE_RX24-	PCIE_TX24-
80	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
81	LVDS_A_CK+	LVDS_B_CK+	PCIE_RX25+	PCIE_TX25+
82	LVDS_A_CK-	LVDS_B_CK-	PCIE_RX25-	PCIE_TX25-
83	LVDS_I2C_CK	LVDS_BKLT_CTRL	RSVD[16]	RSVD[16]
84	LVDS_I2C_DAT	VCC_5V_SBY	GND	GND
85	GPI3	VCC_5V_SBY	PCIE_RX26+	PCIE_TX26+
86	KBD_RST#	VCC_5V_SBY	PCIE_RX26-	PCIE_TX26-
87	KBD_A20GATE	VCC_5V_SBY	GND	GND
88	PCIE_CLK_REF+	BIOS_DIS1#	PCIE_RX27+	PCIE_TX27+

Pin	Row A	Row B	Row C	Row D
89	PCIE_CLK_REF-	VGA_RED	PCIE_RX27-	PCIE_TX27-
90	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
91	SPI_POWER	VGA_GRN	PCIE_RX28+	PCIE_TX28+
92	SPI_MISO	VGA_BLU	PCIE_RX28-	PCIE_TX28-
93	GPO0	VGA_HSYNC	GND	GND
94	SPI_CLK	VGA_VSYNC	PCIE_RX29+	PCIE_TX29+
95	SPI_MOSI	VGA_I2C_CK	PCIE_RX29-	PCIE_TX29-
96	GND	VGA_I2C_DAT	GND	GND
97	TYPE10#	SPI_CS#	RSVD[16]	PEG_ENABLE#
98	RSVD[16]	RSVD[16]	PCIE_RX30+	PCIE_TX30+
99	RSVD[16]	RSVD[16]	PCIE_RX30-	PCIE_TX30-
100	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
101	RSVD[16]	RSVD[16]	PCIE_RX31+	PCIE_TX31+
102	RSVD[16]	RSVD[16]	PCIE_RX31-	PCIE_TX31-
103	RSVD[16]	RSVD[16]	GND	GND
104	VCC_12V	VCC_12V	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V	VCC_12V	VCC_12V
109	VCC_12V	VCC_12V	VCC_12V	VCC_12V
110	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)

4.6.6 Type 5

Type 5 reassigns PCI to 10 additional PCIE lanes and IDE to 2 additional GBE ports. PEG lanes 0-15 are renamed PCIE lanes 16-31. These lanes ***may*** be used as PEG lanes 0-15 or as general purpose PCIE lanes 16-31. Modules implementing Pin-out Type 5 ***shall*** use the pin-out shown in this table. Refer to Table 3.2 for minimum requirements and Table 3.4 for the order in which interfaces ***shall*** be implemented.

Table 4.44: Pin List for Pin-out Type 5

Pin	Row A	Row B	Row C	Row D
1	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
2	GBE0_MDI3-	GBE0_ACT#	GBE1_ACT#	GBE2_ACT#
3	GBE0_MDI3+	LPC_FRAME#	GBE1_MDI3-	GBE2_MDI3-
4	GBE0_LINK100#	LPC_AD0	GBE1_MDI3+	GBE2_MDI3+
5	GBE0_LINK1000#	LPC_AD1	GBE1_LINK100#	GBE2_LINK100#
6	GBE0_MDI2-	LPC_AD2	GBE1_MDI2-	GBE2_MDI2-
7	GBE0_MDI2+	LPC_AD3	GBE1_MDI2+	GBE2_MDI2+
8	GBE0_LINK#	LPC_DRQ0#	GBE1_LINK1000#	GBE2_LINK1000#
9	GBE0_MDI1-	LPC_DRQ1#	GBE1_MDI1-	GBE2_MDI1-
10	GBE0_MDI1+	LPC_CLK	GBE1_MDI1+	GBE2_MDI1+
11	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
12	GBE0_MDI0-	PWRBTN#	GBE1_MDI0-	GBE2_MDI0-
13	GBE0_MDI0+	SMB_CK	GBE1_MDI0+	GBE2_MDI0+
14	GBE0_CTREF	SMB_DAT	GBE1_LINK#	GBE2_LINK#
15	SUS_S3#	SMB_ALERT#	RSVD[17]	GBE2_CTREF
16	SATA0_TX+	SATA1_TX+	RSVD[17]	RSVD[17]
17	SATA0_TX-	SATA1_TX-	RSVD[17]	RSVD[17]
18	SUS_S4#	SUS_STAT#	RSVD[17]	RSVD[17]
19	SATA0_RX+	SATA1_RX+	PCIE_RX6+	PCIE_TX6+
20	SATA0_RX-	SATA1_RX-	PCIE_RX6-	PCIE_TX6-
21	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
22	SATA2_TX+	SATA3_TX+	PCIE_RX7+	PCIE_TX7+
23	SATA2_TX-	SATA3_TX-	PCIE_RX7-	PCIE_TX7-
24	SUS_S5#	PWR_OK	RSVD[17]	RSVD[17]
25	SATA2_RX+	SATA3_RX+	RSVD[17]	RSVD[17]
26	SATA2_RX-	SATA3_RX-	PCIE_RX8+	PCIE_TX8+
27	BATLOW#	WDT	PCIE_RX8-	PCIE_TX8-
28	(S)ATA_ACT#	AC/HDA_SDIN2	RSVD[17]	RSVD[17]
29	AC/HDA_SYNC	AC/HDA_SDIN1	PCIE_RX9+	PCIE_TX9+
30	AC/HDA_RST#	AC/HDA_SDIN0	PCIE_RX9-	PCIE_TX9-
31	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
32	AC/HDA_BITCLK	SPKR	PCIE_RX10+	PCIE_TX10+
33	AC/HDA_SDOUT	I2C_CK	PCIE_RX10-	PCIE_TX10-
34	BIOS_DIS0#	I2C_DAT	RSVD[17]	RSVD[17]
35	THRMTRIP#	THRM#	RSVD[17]	RSVD[17]
36	USB6-	USB7-	PCIE_RX11+	PCIE_TX11+
37	USB6+	USB7+	PCIE_RX11-	PCIE_TX11-
38	USB_6_7_OC#	USB_4_5_OC#	RSVD[17]	RSVD[17]
39	USB4-	USB5-	PCIE_RX12+	PCIE_TX12+

17 *RSVD pins are reserved for future use and* ***should*** *be no connect. Do not tie the RSVD pins together.*

Pin	Row A	Row B	Row C	Row D
40	USB4+	USB5+	PCIE_RX12-	PCIE_TX12-
41	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
42	USB2-	USB3-	PCIE_RX13+	PCIE_TX13+
43	USB2+	USB3+	PCIE_RX13-	PCIE_TX13-
44	USB_2_3_OC#	USB_0_1_OC#	RSVD[17]	RSVD[17]
45	USB0-	USB1-	RSVD[17]	RSVD[17]
46	USB0+	USB1+	PCIE_RX14+	PCIE_TX14+
47	VCC_RTC	EXCD1_PERST#	PCIE_RX14-	PCIE_TX14-
48	EXCD0_PERST#	EXCD1_CPPE#	RSVD[17]	RSVD[17]
49	EXCD0_CPPE#	SYS_RESET#	PCIE_RX15+	PCIE_TX15+
50	LPC_SERIRQ	CB_RESET#	PCIE_RX15-	PCIE_TX15-
51	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
52	PCIE_TX5+	PCIE_RX5+	PCIE_RX16+	PCIE_TX16+
53	PCIE_TX5-	PCIE_RX5-	PCIE_RX16-	PCIE_TX16-
54	GPI0	GPO1	TYPE0#	PEG_LANE_RV#
55	PCIE_TX4+	PCIE_RX4+	PCIE_RX17+	PCIE_TX17+
56	PCIE_TX4-	PCIE_RX4-	PCIE_RX17-	PCIE_TX17-
57	GND	GPO2	TYPE1#	TYPE2#
58	PCIE_TX3+	PCIE_RX3+	PCIE_RX18+	PCIE_TX18+
59	PCIE_TX3-	PCIE_RX3-	PCIE_RX18-	PCIE_TX18-
60	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
61	PCIE_TX2+	PCIE_RX2+	PCIE_RX19+	PCIE_TX19+
62	PCIE_TX2-	PCIE_RX2-	PCIE_RX19-	PCIE_TX19-
63	GPI1	GPO3	RSVD[17]	RSVD[17]
64	PCIE_TX1+	PCIE_RX1+	RSVD[17]	RSVD[17]
65	PCIE_TX1-	PCIE_RX1-	PCIE_RX20+	PCIE_TX20+
66	GND	WAKE0#	PCIE_RX20-	PCIE_TX20-
67	GPI2	WAKE1#	RSVD[17]	GND
68	PCIE_TX0+	PCIE_RX0+	PCIE_RX21+	PCIE_TX21+
69	PCIE_TX0-	PCIE_RX0-	PCIE_RX21-	PCIE_TX21-
70	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
71	LVDS_A0+	LVDS_B0+	PCIE_RX22+	PCIE_TX22+
72	LVDS_A0-	LVDS_B0-	PCIE_RX22-	PCIE_TX22-
73	LVDS_A1+	LVDS_B1+	SDVO_DATA	SDVO_CLK
74	LVDS_A1-	LVDS_B1-	PCIE_RX23+	PCIE_TX23+
75	LVDS_A2+	LVDS_B2+	PCIE_RX23-	PCIE_TX23-
76	LVDS_A2-	LVDS_B2-	GND	GND
77	LVDS_VDD_EN	LVDS_B3+	RSVD[17]	RSVD[17]
78	LVDS_A3+	LVDS_B3-	PCIE_RX24+	PCIE_TX24+
79	LVDS_A3-	LVDS_BKLT_EN	PCIE_RX24-	PCIE_TX24-
80	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
81	LVDS_A_CK+	LVDS_B_CK+	PCIE_RX25+	PCIE_TX25+
82	LVDS_A_CK-	LVDS_B_CK-	PCIE_RX25-	PCIE_TX25-
83	LVDS_I2C_CK	LVDS_BKLT_CTRL	RSVD[17]	RSVD[17]
84	LVDS_I2C_DAT	VCC_5V_SBY	GND	GND
85	GPI3	VCC_5V_SBY	PCIE_RX26+	PCIE_TX26+
86	KBD_RST#	VCC_5V_SBY	PCIE_RX26-	PCIE_TX26-
87	KBD_A20GATE	VCC_5V_SBY	GND	GND
88	PCIE_CLK_REF+	BIOS_DIS1#	PCIE_RX27+	PCIE_TX27+

Pin	Row A	Row B	Row C	Row D
89	PCIE_CLK_REF-	VGA_RED	PCIE_RX27-	PCIE_TX27-
90	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
91	SPI_POWER	VGA_GRN	PCIE_RX28+	PCIE_TX28+
92	SPI_MISO	VGA_BLU	PCIE_RX28-	PCIE_TX28-
93	GPO0	VGA_HSYNC	GND	GND
94	SPI_CLK	VGA_VSYNC	PCIE_RX29+	PCIE_TX29+
95	SPI_MOSI	VGA_I2C_CK	PCIE_RX29-	PCIE_TX29-
96	GND	VGA_I2C_DAT	GND	GND
97	TYPE10#	SPI_CS#	RSVD[17]	PEG_ENABLE#
98	RSVD[17]	RSVD[17]	PCIE_RX30+	PCIE_TX30+
99	RSVD[17]	RSVD[17]	PCIE_RX30-	PCIE_TX30-
100	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
101	RSVD[17]	RSVD[17]	PCIE_RX31+	PCIE_TX31+
102	RSVD[17]	RSVD[17]	PCIE_RX31-	PCIE_TX31-
103	RSVD[17]	RSVD[17]	GND	GND
104	VCC_12V	VCC_12V	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V	VCC_12V	VCC_12V
109	VCC_12V	VCC_12V	VCC_12V	VCC_12V
110	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)

4.6.7 Type 6

Modules implementing Pin-out Type 6 ***shall*** use the pin-out shown in this table. Refer to Table 3.2 for minimum requirements and Table 3.4 for the order in which interfaces ***shall*** be implemented.

Table 4.45: Pin List for Pin-out Type 6

Pin	Row A	Row B	Row C	Row D
1	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
2	GBE0_MDI3-	GBE0_ACT#	GND	GND
3	GBE0_MDI3+	LPC_FRAME#	USB_SSRX0-	USB_SSTX0-
4	GBE0_LINK100#	LPC_AD0	USB_SSRX0+	USB_SSTX0+
5	GBE0_LINK1000#	LPC_AD1	GND	GND
6	GBE0_MDI2-	LPC_AD2	USB_SSRX1-	USB_SSTX1-
7	GBE0_MDI2+	LPC_AD3	USB_SSRX1+	USB_SSTX1+
8	GBE0_LINK#	LPC_DRQ0#	GND	GND
9	GBE0_MDI1-	LPC_DRQ1#	USB_SSRX2-	USB_SSTX2-
10	GBE0_MDI1+	LPC_CLK	USB_SSRX2+	USB_SSTX2+
11	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
12	GBE0_MDI0-	PWRBTN#	USB_SSRX3-	USB_SSTX3-
13	GBE0_MDI0+	SMB_CK	USB_SSRX3+	USB_SSTX3+
14	GBE0_CTREF	SMB_DAT	GND	GND
15	SUS_S3#	SMB_ALERT#	DDI1_PAIR6+	DDI1_CTRLCLK_AUX+
16	SATA0_TX+	SATA1_TX+	DDI1_PAIR6-	DDI1_CTRLDATA_AUX-
17	SATA0_TX-	SATA1_TX-	RSVD[18]	RSVD[18]
18	SUS_S4#	SUS_STAT#	RSVD[18]	RSVD[18]
19	SATA0_RX+	SATA1_RX+	PCIE_RX6+	PCIE_TX6+
20	SATA0_RX-	SATA1_RX-	PCIE_RX6-	PCIE_TX6-
21	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
22	SATA2_TX+	SATA3_TX+	PCIE_RX7+	PCIE_TX7+
23	SATA2_TX-	SATA3_TX-	PCIE_RX7-	PCIE_TX7-
24	SUS_S5#	PWR_OK	DDI1_HPD	RSVD[18]
25	SATA2_RX+	SATA3_RX+	DDI1_PAIR4 +	RSVD[18]
26	SATA2_RX-	SATA3_RX-	DDI1_PAIR4-	DDI1_PAIR0+
27	BATLOW#	WDT	RSVD[18]	DDI1_PAIR0-
28	(S)ATA_ACT#	AC/HDA_SDIN2	RSVD[18]	RSVD[18]
29	AC/HDA_SYNC	AC/HDA_SDIN1	DDI1_PAIR5+	DDI1_PAIR1+
30	AC/HDA_RST#	AC/HDA_SDIN0	DDI1_PAIR5-	DDI1_PAIR1-
31	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
32	AC/HDA_BITCLK	SPKR	DDI2_CTRLCLK_AUX+	DDI1_PAIR2+
33	AC/HDA_SDOUT	I2C_CK	DDI2_CTRLDATA_AUX-	DDI1_PAIR2-
34	BIOS_DIS0#	I2C_DAT	DDI2_DDC_AUX_SEL	DDI1_DDC_AUX_SEL
35	THRMTRIP#	THRM#	RSVD[18]	RSVD[18]
36	USB6-	USB7-	DDI3_CTRLCLK_AUX+	DDI1_PAIR3+
37	USB6+	USB7+	DDI3_CTRLDATA_AUX-	DDI1_PAIR3-
38	USB_6_7_OC#	USB_4_5_OC#	DDI3_DDC_AUX_SEL	RSVD[18]
39	USB4-	USB5-	DDI3_PAIR0+	DDI2_PAIR0+
40	USB4+	USB5+	DDI3_PAIR0-	DDI2_PAIR0-
41	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)

18 *RSVD pins are reserved for future use and* ***should*** *be no connect. Do not tie the RSVD pins together.*

Pin	Row A	Row B	Row C	Row D
42	USB2-	USB3-	DDI3_PAIR1+	DDI2_PAIR1+
43	USB2+	USB3+	DDI3_PAIR1-	DDI2_PAIR1-
44	USB_2_3_OC#	USB_0_1_OC#	DDI3_HPD	DDI2_HPD
45	USB0-	USB1-	RSVD[18]	RSVD[18]
46	USB0+	USB1+	DDI3_PAIR2+	DDI2_PAIR2+
47	VCC_RTC	EXCD1_PERST#	DDI3_PAIR2-	DDI2_PAIR2-
48	EXCD0_PERST#	EXCD1_CPPE#	RSVD[18]	RSVD[18]
49	EXCD0_CPPE#	SYS_RESET#	DDI3_PAIR3+	DDI2_PAIR3+
50	LPC_SERIRQ	CB_RESET#	DDI3_PAIR3-	DDI2_PAIR3-
51	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
52	PCIE_TX5+	PCIE_RX5+	PEG_RX0+	PEG_TX0+
53	PCIE_TX5-	PCIE_RX5-	PEG_RX0-	PEG_TX0-
54	GPI0	GPO1	TYPE0#	PEG_LANE_RV#
55	PCIE_TX4+	PCIE_RX4+	PEG_RX1+	PEG_TX1+
56	PCIE_TX4-	PCIE_RX4-	PEG_RX1-	PEG_TX1-
57	GND	GPO2	TYPE1#	TYPE2#
58	PCIE_TX3+	PCIE_RX3+	PEG_RX2+	PEG_TX2+
59	PCIE_TX3-	PCIE_RX3-	PEG_RX2-	PEG_TX2-
60	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
61	PCIE_TX2+	PCIE_RX2+	PEG_RX3+	PEG_TX3+
62	PCIE_TX2-	PCIE_RX2-	PEG_RX3-	PEG_TX3-
63	GPI1	GPO3	RSVD[18]	RSVD[18]
64	PCIE_TX1+	PCIE_RX1+	RSVD[18]	RSVD[18]
65	PCIE_TX1-	PCIE_RX1-	PEG_RX4+	PEG_TX4+
66	GND	WAKE0#	PEG_RX4-	PEG_TX4-
67	GPI2	WAKE1#	RSVD[18]	GND
68	PCIE_TX0+	PCIE_RX0+	PEG_RX5+	PEG_TX5+
69	PCIE_TX0-	PCIE_RX0-	PEG_RX5-	PEG_TX5-
70	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
71	LVDS_A0+	LVDS_B0+	PEG_RX6+	PEG_TX6+
72	LVDS_A0-	LVDS_B0-	PEG_RX6-	PEG_TX6-
73	LVDS_A1+	LVDS_B1+	GND	GND
74	LVDS_A1-	LVDS_B1-	PEG_RX7+	PEG_TX7+
75	LVDS_A2+	LVDS_B2+	PEG_RX7-	PEG_TX7-
76	LVDS_A2-	LVDS_B2-	GND	GND
77	LVDS_VDD_EN	LVDS_B3+	RSVD[18]	RSVD[18]
78	LVDS_A3+	LVDS_B3-	PEG_RX8+	PEG_TX8+
79	LVDS_A3-	LVDS_BKLT_EN	PEG_RX8-	PEG_TX8-
80	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
81	LVDS_A_CK+	LVDS_B_CK+	PEG_RX9+	PEG_TX9+
82	LVDS_A_CK-	LVDS_B_CK-	PEG_RX9-	PEG_TX9-
83	LVDS_I2C_CK	LVDS_BKLT_CTRL	RSVD[18]	RSVD[18]
84	LVDS_I2C_DAT	VCC_5V_SBY	GND	GND
85	GPI3	VCC_5V_SBY	PEG_RX10+	PEG_TX10+
86	RSVD[18]	VCC_5V_SBY	PEG_RX10-	PEG_TX10-
87	eDP_HPD	VCC_5V_SBY	GND	GND
88	PCIE_CLK_REF+	BIOS_DIS1#	PEG_RX11+	PEG_TX11+
89	PCIE_CLK_REF-	VGA_RED	PEG_RX11-	PEG_TX11-
90	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)

Pin	Row A	Row B	Row C	Row D
91	SPI_POWER	VGA_GRN	PEG_RX12+	PEG_TX12+
92	SPI_MISO	VGA_BLU	PEG_RX12-	PEG_TX12-
93	GPO0	VGA_HSYNC	GND	GND
94	SPI_CLK	VGA_VSYNC	PEG_RX13+	PEG_TX13+
95	SPI_MOSI	VGA_I2C_CK	PEG_RX13-	PEG_TX13-
96	TPM_PP	VGA_I2C_DAT	GND	GND
97	TYPE10#	SPI_CS#	RSVD[18]	RSVD[18]
98	SER0_TX	RSVD[18]	PEG_RX14+	PEG_TX14+
99	SER0_RX	RSVD[18]	PEG_RX14-	PEG_TX14-
100	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
101	SER1_TX	FAN_PWNOUT	PEG_RX15+	PEG_TX15+
102	SER1_RX	FAN_TACHIN	PEG_RX15-	PEG_TX15-
103	LID#	SLEEP#	GND	GND
104	VCC_12V	VCC_12V	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V	VCC_12V	VCC_12V
109	VCC_12V	VCC_12V	VCC_12V	VCC_12V
110	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)

5 Module and Carrier Board Implementation Specifications

5.1 PCI Express Link Configuration Definitions

Lane: A "lane" or "PCI Express lane" is a set of 4 pins on the COM Express connector that can be used for a single PCI Express transmit pair and a single receive pair. Clocking information is embedded into the data stream.

Link: A "link" or "PCI Express link" is a group of PCI Express lanes between two PCI Express agents. Allowable link widths are x1, x2, x4, x8, x16 and x32. An x1 link utilizes 1 lane; an x2 link 2 lanes, etc. The link bandwidth scales up proportionally with the link width.

Link Configuration:

The COM Express connector allows up to 32 PCI Express lanes to be used. The count varies with the Module Pin-out Type. Chipsets used on COM Express Modules have a variety of PCI Express lane and link capabilities. On some chipsets, the PCI Express lanes can be grouped into various links under software control; on other chipsets, the PCI Express links are of a fixed width. The mapping of the chipset PCI Express lanes to the COM Express lanes and the grouping of the lanes into links is referred to as "link configuration."

Bucket: A "bucket" is a group of 8 PCI Express lanes on the COM Express connector. The 32 PCI Express lanes on the COM Express connector are conceptually divided into 4 buckets to facilitate a description of how the available PCI Express lanes should be assigned to COM Express connector pins. The "bucket" terminology is only a vehicle to facilitate the description of an orderly mapping of chipset PCI Express lanes to COM Express connector PCI Express lanes. A bucket is not a link.

5.2 PCI Express Link Configuration Guidelines

The COM Express connector PCI Express lanes are conceptually divided into four “buckets,” labeled B1, B2, B3, and B4. The buckets ***shall*** be filled according to the following rules:

- The fill starts from the lowest lane number in a bucket and proceeds upwards.
- The largest links go into the lower lane numbers in a bucket.
- Links that are 16 lanes wide ***shall*** span buckets B3 and B4 or buckets B1 and B2.
- PCI Express Graphics (PEG) link(s) ***shall*** use B3 and B4 for the first link and ***shall*** use B1 and B2 for a 2nd link.
- Links that span more than one bucket ***shall*** start in the bucket with the lowest lane number.

Table 5.1: PCI Express Lane Numbers and Bucket Groupings

COM Express Pin Label	Lane Number	Availability By Module Pin-out Type	Bucket Reference
PEG15	31	Module Pin-out Types 2,3,4,5,6 (PCI Express Graphics) Module Pin-out Types 2,3,4,5,6 (PCI Express, general I/O)	Bucket B4
PEG14	30		
PEG13	29		
PEG12	28		
PEG11	27		
PEG10	26		
PEG9	25		
PEG8	24		
PEG7	23		Bucket B3
PEG6	22		
PEG5	21		
PEG4	20		
PEG3	19		
PEG2	18		
PEG1	17		
PEG0	16		
PCIE15	15	Module Pin-out Type 4,5	Bucket B2
PCIE14	14		
PCIE13	13		
PCIE12	12		
PCIE11	11		
PCIE10	10		
PCIE9	9		
PCIE8	8		
PCIE7	7	Module Pin-out Types 4,5,6	Bucket B1
PCIE6	6		
PCIE5	5	Module Pin-out Types 1,2,3,4,5,6	
PCIE4	4		
PCIE3	3	Module Pin-out Types 1,2,3,4,5,6,10	
PCIE2	2		
PCIE1	1		
PCIE0	0		

While many permutations are possible, the set of tables below indicate the preferred mappings of chipset PCI Express lanes and links to COM Express connector lanes and links. On most Module designs, a portion of available COM Express PCI Express lanes are used.

Table 5.2: Module Pin-out Type 1 - Preferred PCI Express Lane Groupings

COM Express Pin Label	Lane	Bucket Reference	Preferred Link Configurations							
PEG15	31	B4								
PEG14	30									
PEG13	29									
PEG12	28									
PEG11	27									
PEG10	26									
PEG9	25									
PEG8	24									
PEG7	23	B3								
PEG6	22									
PEG5	21									
PEG4	20									
PEG3	19									
PEG2	18									
PEG1	17									
PEG0	16									
PCIE15	15	B2								
PCIE14	14									
PCIE13	13									
PCIE12	12									
PCIE11	11									
PCIE10	10									
PCIE9	9									
PCIE8	8									
PCIE7	7									
PCIE6	6									
PCIE5	5	B1							X1	X1
PCIE4	4						X1	X1	X1	X1
PCIE3	3				X1	X4	X1	X4	X1	X4
PCIE2	2			X1	X1		X1		X1	
PCIE1	1		X1	X1	X1		X1		X1	
PCIE0	0		X1	X1	X1		X1		X1	

Note: Grey shaded lanes are not available in Pin-out Type 1.

Table 5.3: Module Pin-out Types 2 and 3 - Preferred Lane Groupings: Bucket B1

COM Express Pin Label	Lane	Bucket Reference	Preferred Link Configurations									
PEG15	31	B4	X16 (PEG)									
PEG14	30											
PEG13	29											
PEG12	28											
PEG11	27											
PEG10	26											
PEG9	25											
PEG8	24											
PEG7	23	B3										
PEG6	22											
PEG5	21											
PEG4	20											
PEG3	19											
PEG2	18											
PEG1	17											
PEG0	16											
PCIE15	15	B2										
PCIE14	14											
PCIE13	13											
PCIE12	12											
PCIE11	11											
PCIE10	10											
PCIE9	9											
PCIE8	8											
PCIE7	7											
PCIE6	6											
PCIE5	5	B1							X1	X1	X1	X1
PCIE4	4						X1	X1	X1	X1	X1	X1
PCIE3	3				X1	X4	X1	X4	X1	X1	X1	X4
PCIE2	2			X1	X1		X1		X1	X1	X1	
PCIE1	1		X1	X1	X1		X1		X1	X1	X1	
PCIE0	0		X1	X1	X1		X1		X1	X1	X1	

Notes:

1) Grey shaded lanes are not available in Pin-out Types 2 and 3.
2) If upper lanes (buckets B3 and B4) are not used for PCI Express Graphics (PEG), then lanes mapped into buckets B3 and B4 ***should*** be grouped per Table 5.4 'Module Pin-out Types 2 and 3 - Preferred Lane Groupings: Buckets B3 and B4' on page 96.

Table 5.4: Module Pin-out Types 2 and 3 - Preferred Lane Groupings: Buckets B3 and B4

COM Express Pin Label	PCI Express Lane	Bucket Reference	Preferred Link Configurations			
PEG15	31	B4	X4	X4	X8	X16 (PEG)
PEG14	30					
PEG13	29					
PEG12	28					
PEG11	27		X4	X4		
PEG10	26					
PEG9	25					
PEG8	24					
PEG7	23	B3	X4	X8	X8	
PEG6	22					
PEG5	21					
PEG4	20					
PEG3	19		X4			
PEG2	18					
PEG1	17					
PEG0	16					
PCIE15	15	B2				
PCIE14	14					
PCIE13	13					
PCIE12	12					
PCIE11	11					
PCIE10	10					
PCIE9	9					
PCIE8	8					
PCIE7	7					
PCIE6	6					
PCIE5	5	B1	Refer to bucket B1 in Table 5.3			
PCIE4	4					
PCIE3	3					
PCIE2	2					
PCIE1	1					
PCIE0	0					

Notes:

1) Grey shaded lanes are not available in Pin-out Types 2 and 3.
2) Bucket B1 groupings for Pin-out Types 2 and 3 covered in Table 5.3 'Module Pin-out Types 2 and 3 - Preferred Lane Groupings: Bucket B1' on page 95.
3) X16 link ***may*** be used for PCI Express Graphics (PEG) or for general purpose I/O.

Table 5.5: Module Pin-out Types 4 and 5 - Preferred PCI Express Lane Groupings

COM Express Pin Label	Lane	Bucket Reference	Preferred Link Configurations								
PEG15	31	B4	X4	X4	X4	X4	X4	X8	X8	X16 (PEG)	X32
PEG14	30										
PEG13	29										
PEG12	28										
PEG11	27		X4	X4	X4	X4	X4				
PEG10	26										
PEG9	25										
PEG8	24										
PEG7	23	B3	X4	X4	X4	X8	X8	X8	X8		
PEG6	22										
PEG5	21										
PEG4	20										
PEG3	19		X4	X4	X4						
PEG2	18										
PEG1	17										
PEG0	16										
PCIE15	15	B2	X4	X4	X8	X8	X8	X8	X16	X16	
PCIE14	14										
PCIE13	13										
PCIE12	12										
PCIE11	11		X4	X4							
PCIE10	10										
PCIE9	9										
PCIE8	8										
PCIE7	7	B1	X4	X8	X8	X8	X8	X8			
PCIE6	6										
PCIE5	5										
PCIE4	4										
PCIE3	3		X4								
PCIE2	2										
PCIE1	1										
PCIE0	0										

Table 5.6: Module Pin-out Type 6 - Preferred Lane Groupings: Bucket B1

COM Express Pin Label	Lane	Bucket Reference	Preferred Link Configurations											
PEG15	31	B4	X16 (PEG)											
PEG14	30													
PEG13	29													
PEG12	28													
PEG11	27													
PEG10	26													
PEG9	25													
PEG8	24													
PEG7	23	B3												
PEG6	22													
PEG5	21													
PEG4	20													
PEG3	19													
PEG2	18													
PEG1	17													
PEG0	16													
PCIE15	15	B2												
PCIE14	14													
PCIE13	13													
PCIE12	12													
PCIE11	11													
PCIE10	10													
PCIE9	9													
PCIE8	8													
PCIE7	7	B1									X1	X1	X4	X8
PCIE6	6								X1	X1	X1			
PCIE5	5							X1	X1	X1	X1			
PCIE4	4					X1	X1	X1	X1	X1	X1			
PCIE3	3				X1		X1		X1	X1	X1			
PCIE2	2			X1	X1	X4	X1	X4	X1	X1	X1	X4	X4	
PCIE1	1		X1	X1	X1		X1		X1	X1	X1			
PCIE0	0		X1	X1	X1		X1		X1	X1	X1			

Notes:

3) Lanes 6 and 7 only available on Type 6
4) Grey shaded lanes are not available in Pin-out Types 2 and 3.
5) If upper lanes (buckets B3 and B4) are not used for PCI Express Graphics (PEG), then lanes mapped into buckets B3 and B4 ***should*** be grouped per Table 5.7 'Module Pin-out Type 6 - Preferred Lane Groupings: Buckets B3 and B4' on page 99.

Table 5.7: Module Pin-out Type 6 - Preferred Lane Groupings: Buckets B3 and B4

COM Express Pin Label	PCI Express Lane	Bucket Reference	Preferred Link Configurations			
PEG15	31	B4	X4	X4	X8	X16 (PEG)
PEG14	30					
PEG13	29					
PEG12	28					
PEG11	27		X4	X4		
PEG10	26					
PEG9	25					
PEG8	24					
PEG7	23	B3	X4	X8	X8	
PEG6	22					
PEG5	21					
PEG4	20					
PEG3	19		X4			
PEG2	18					
PEG1	17					
PEG0	16					
PCIE15	15	B2				
PCIE14	14					
PCIE13	13					
PCIE12	12					
PCIE11	11					
PCIE10	10					
PCIE9	9					
PCIE8	8					
PCIE7	7	B1	Refer to bucket B1 in Table 5.6			
PCIE6	6					
PCIE5	5					
PCIE4	4					
PCIE3	3					
PCIE2	2					
PCIE1	1					
PCIE0	0					

Notes:

1) Grey shaded lanes are not available in Pin-out Types 2 and 3.
2) Bucket B1 groupings for Pin-out Types 2, 3 and 6 covered in Table 5.6 'Module Pin-out Type 6 - Preferred Lane Groupings: Bucket B1' on page 98.
3) X16 link ***may*** be used for PCI Express Graphics (PEG) or for general purpose I/O.

5.3 COM Express EEPROMs

The COM Express EEPROM content is defined in the PICMG COM Express companion document EeeP(Embedded EEPROM) Specification. The COM Express R1.0 Carrier Board configuration EEPROM content and layout is superseded by the EeeP Specification. All new designs implementing either the Module or Carrier EEPROM ***shall*** exclusively use the new EeeP styled layout.

5.3.1 EEPROM Device Information

If the Module and or Carrier EEPROMs are implemented, a two-wire serial interface device operating at a supply voltage of 3.3V ***shall*** be used. The two-wire interface ***shall*** be I2C compatible. The device ***shall*** have a capacity of at least 2 kbits, and ***shall*** have three address inputs. Suitable devices include the Atmel AT24C32C, the ST M24C32 and other compatible devices.

5.3.2 COM Express Module EEPROM

The Module Board ***should*** implement a serial EEPROM that Identifies the Module using the Unique Device Id.

The Module EEPROM allows the COM Express Carrier Board to set up any software configurable Carrier Board features in a way that is appropriate for the Module board.

The Module EEPROM device, if implemented, ***shall*** interface to the Carrier Board over the general purpose I2C interface (COM Express pin names I2C_DAT and I2C_CK). The device address lines, A2, A1 and A0 ***shall*** be pulled to a logic low, placing the device at address 0x50(0xA0) (A6-A3 = 1010b for I2C EEPROM devices).

5.3.3 COM Express Carrier Board EEPROM

The Carrier Board ***should*** implement a serial EEPROM that identifies the Carrier using the Unique Device Id and describe the expected PCI Express link configuration. In addition this EEPROM ***may*** describe the expected link presence for SATA, SAS, Express Card, USB, DDI, VGA, LAN, audio, and the expected presence of miscellaneous I/O signals.

The Carrier EEPROM allows the COM Express Module BIOS to set up any software configurable Module features in a way that is appropriate for the Carrier Board. If there is an incompatibility between the expected Carrier Board configuration and the Module capabilities, an error message ***may*** be generated. The error messaging is Module vendor specific and is not defined by this standard.

The Carrier EEPROM device, if implemented, ***shall*** interface to the Module over the general purpose I2C interface (COM Express pin names I2C_DAT and I2C_CK). The device address lines, A2, A1 and A0 ***shall*** be pulled to a logic high, placing the device at address 0x57(0xAE) (A6-A3 = 1010b for I2C EEPROM devices).

5.4 Loss Budgets for High Speed Differential Interfaces

COM Express Module and Carrier Board insertion loss budgets for the PCI Express, SATA, USB and GBE interfaces are presented in the following Sections.

The COM Express Module and Carrier Board insertion loss budgets were formulated to be compatible with the relevant source specifications. The source specifications vary in their treatment of insertion loss parameters. For example, the PCI Express Card Electromechanical Specification factors cross talk losses into the insertion loss budgets, but the SATA, USB and GBE source specifications do not.

For frequency dependent material losses, a rule-of-thumb insertion loss value of 0.28 dB per inch per GHz is used in all cases, representative of commonly used FR4 PCB laminates. This value is consistent with the PCI Express Card Electromechanical Specification usage (which calls out a 1.4 dB material loss for 4 inches of trace at 1.25 GHz). It is also consistent with other PICMG specifications that use values slightly above and below this value.

Module and Carrier Board vendors ***may*** elect to use PCB laminates with better characteristics than common FR4. If this is done, then the trace lengths referenced in the following Sections may be extended as long as the net insertion loss budgets are met.

Loss budgets for future generations of PCI Express (Gen 3), Ethernet (10 Gbps) and SATA (Gen 3) will be addressed in future revisions to this document.

There is no explicit COM Express jitter budget for the high speed differential interfaces. Designers are referred to the relevant source specifications (PCIE, SATA, USB and GBE) for system jitter budgets.

To develop guidelines for PCI Express Gen 2 (5 GT/s) operation, a series of simulations that modeled PCIe Gen2 operations in the COM Express environment was conducted per the recommendations given in the PCI-SIG PCI Express ® Base Specification, Rev 2.1, Section 4.3.6, “Channel Specifications”. The following two paragraphs excerpted from the PCI-SIG document, Section 4.3.6.2, “Channel Characteristics at 5.0 GT/s” may serve as an overview of the PCI-SIG recommendations:

> At 5.0 GT/s a more accurate method of comprehending the effects of channel loss is required in order to avoid excessive guardbanding. The method described here imports the channel’s s-parameters into a simulation environment that includes worst case models for Transmitters and data patterns. The resulting time domain simulation yields eye diagrams from which voltage and timing margins may be obtained and compared against those defined for the Receiver.
> Note: The methodology described in Sections 4.3.6.2 through 4.3.6.2.7 must be applied to 5.0 GT/s designs, and may be applied to 2.5 GT/s designs.
>
> A channel's characteristics are completely defined by its s-parameters, in particular: insertion loss, return loss, and aggressor-victim coupling. It can been demonstrated that these parameters are sufficient to completely quantize all channel-induced phenomena affecting eye margins including I/O-channel impedance mismatch, insertion loss, jitter amplification, impedance discontinuities, and crosstalk. Long channels tend to be dominated by insertion loss and crosstalk, while short channels tend to dominated by impedance discontinuities. Since both types of channels are possible in PCI Express implementations, it is necessary provide a means of characterizing the channel that comprehends all possible channel characteristics.

All relevant elements of the COM Express environment were included in the simulations: a PCIe Gen 2 source, package breakout, coupling capacitors, Module trace, COM Express connector, Carrier Board trace, and Carrier Board target device, for the “Device Down” case. The “Device Up” case was also simulated, adding in the effects of a Slot Card connector and trace. Cross-talk, jitter and inter-symbol interference effects were included in the simulations, and both the common clocked and data clocked PCIe operations were considered. The simulations were carried out assuming that the Module, Carrier, and Slot PCBs care constructed with standard FR4 dielectrics. Full details of these simulations may be found in the document titled '***PCIe Gen2 COM Express® Hardware Simulation Report***', available from the PICMG.

The conclusions drawn from the simulations are that the eye margins are dominated by the trace length in the various sections and the jitter components, and that connector losses and crosstalk play minor roles. For Gen 2 operation, the maximum allowed PCIe trace lengths need to be shorter than those that were allowed for Gen 1 operation.

5.4.1 PCI Express Insertion Loss Budget with Slot Card

Figure 5-1: PCI Express Insertion Loss Budget with Slot Card

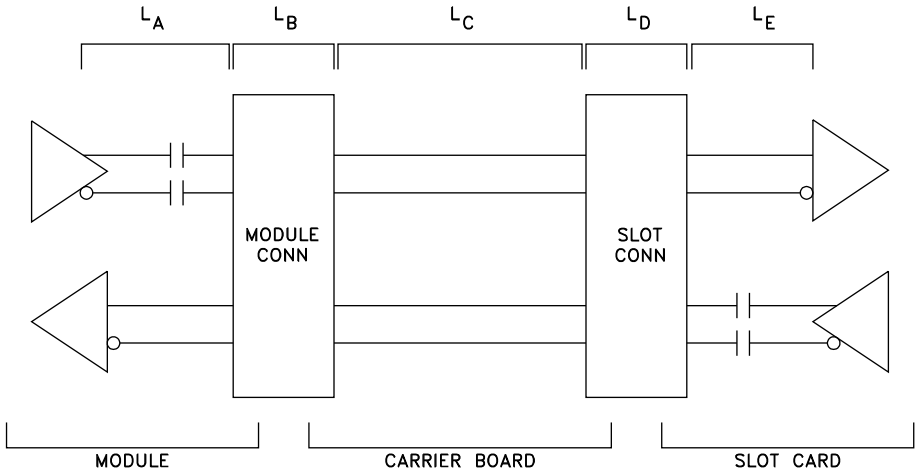


Table 5.8: PCI Express Insertion Loss Budget, 1.25 GHz with Carrier Board Slot Card

Segment	max. Length [mm/inches]	Notes
L_A	130/5.15	Allowance for 3.45 dB loss @ 0.28 dB / GHz / inch and 1.66 dB crosstalk allowance. Coupling caps not included.
Coupling Caps		1.19 dB loss. From PCI Express Card Electromechanical Spec., Rev. 1.1, parameters (L_{ST} – L_{SR}). Includes crosstalk allowance of 0.79 dB.
L_B		COM Express connector at 1.25 GHz measured value: 0.25 dB loss.
L_C	228/9.0	Allowance for 4.40 db loss @ 0.28 dB / GHz / inch and a 1.25 dB crosstalk allowance.
L_D		1.25 dB loss. PCI Express Card Electromechanical Spec Rev 1.1 “guard band” allowance for slot connector – includes 1.0 dB connector loss.
L_E		2.65 dB loss. From PCI Express Card Electromechanical Spec., Rev. 1.1 (without coupling caps; L_{AR}). Implied crosstalk allowance is 1.25 dB.
Total		13.20 dB loss.

The Module transmit and receive insertion loss budgets are different due to the presence of the coupling caps in the Module transmit path. The Module transmit path insertion loss budget ***shall*** be 4.65 dB (3.46 dB + 1.19 dB). The Module receive path insertion loss budget ***shall*** be 3.46 dB. COM Express connector loss is accounted for separately.

The Carrier Board transmit and receive insertion loss budgets are the same in this case. The Carrier Board insertion loss budget ***shall*** be 4.40 dB. COM Express connector and slot card connector losses are accounted for separately.

The slot card transmit and receive insertion loss budgets are different due to the presence of the coupling caps in the slot card’s transmit path. The slot card’s transmit path insertion loss budget is 3.84 dB (2.65 dB + 1.19 dB) per the PCI Express Card Electromechanical Specification Revision 1.1. The slot card’s receive path insertion loss budget is 2.65 dB per the same specification. Slot card connector loss is accounted for separately.

Table 5.9: PCI Express Insertion Loss Budget, 2.5 GHz with Carrier Board Slot Card

Segment	max. Length [mm/inches]	Notes
L_A	127/5.0	Allowance for Module trace. Coupling cap effects included within simulation.
L_B		COM Express connector simulated at 2.5 GHz.
L_C	113/4.45	Allowance for Carrier Board.
L_D		PCI Express Card slot connector simulated at 2.5 GHz.
L_E	80/3.15	Slot Card trace length from PCI Express Card Electromagnetical Spec., Rev. 1.1
Total	320/12.6	PCIe GEN2 Data clocked architecture

For “device up” PCIe Gen 2 operation, the Module PCIe maximum trace length is restricted to 5.0 inches and the Carrier Board maximum trace to 4.45 inches. Shorter lengths will yield additional margin and are encouraged where possible. Results assumed FR4 dielectrics. Other dielectrics with lower losses could be considered, but were not simulated.

It should be noted that a use case exists that might result in reduced PCI Express bandwidth. This use case is tied to Carrier boards with a PCI Express slot (device up). PCI Express Gen 1 and Gen 2 signaling rates use the same PCI Express connector – there is no mechanical keying mechanism to identify the capabilities of the PCI Express slot or the PCI Express board plugged into the slot. This can lead to the situation where the Module and PCI Express board attempt a PCI Express Gen2 signaling rate connection over a Carrier that does not meet the routing guidelines for Gen 2 signaling rates. In a worst case scenario the devices might connect at Gen2 signaling rate with a high number of errors impacting the actual data throughput. It should be noted that there is a Carrier EEPROM which would allow the Module to determine the Carrier Board capabilities but this is not a requirement in COM.0.

5.4.2 PCI Express Insertion Loss Budget with Carrier Board PCIE Device

The insertion losses previously allowed for the slot card and slot card connector are re-allocated for use on the Carrier Board, allowing longer Carrier Board trace lengths and more Carrier Board design flexibility. The Module and COM Express connector loss budgets remain the same.

Figure 5-2: PCI Express Insertion Loss Budget with Carrier Board PCIE Device

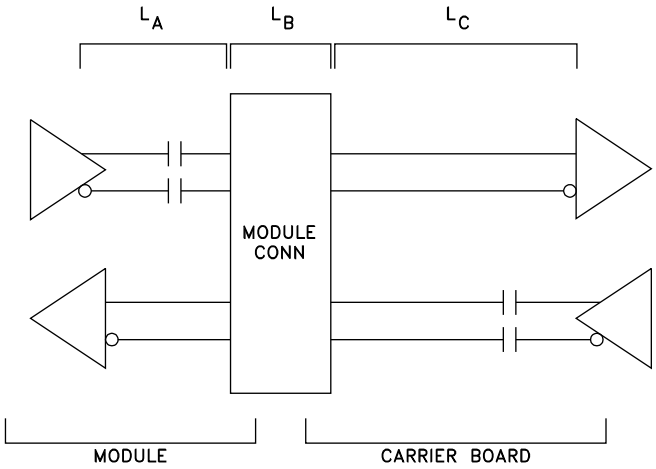


Table 5.10: PCI Express Insertion Loss Budget, 1.25 GHz with Carrier Board PCIE Device

Segment	max. Length [mm/inches]	Notes
L_A	131/5.15	Allowance for 3.46 dB loss @ 0.28 dB / GHz / inch and 1.66 dB crosstalk allowance. Coupling caps not included.
Coupling Caps		1.19 dB loss. From PCI Express Card Electromechanical Spec., Rev. 1.1, parameters (L_{ST} – L_{SR}). Includes crosstalk allowance of 0.79 dB.
L_B		COM Express connector at 1.25 GHz measured value: 0.25 dB loss
L_C	402/15.85	Allowance for 8.30 dB loss @ 0.28 dB / GHz / inch and a 2.75 dB crosstalk allowance.
Total		13.20 dB loss

The Module transmit and receive insertion loss budgets are different due to the presence of the coupling caps in the Module transmit path. The Module transmit path insertion loss budget ***shall*** be 4.65 dB (3.46 dB + 1.19 dB). The Module receive path insertion loss budget ***shall*** be 3.46 dB. COM Express connector loss is accounted for separately.

The Carrier Board transmit and receive insertion loss budgets are different due to the presence of the coupling caps in the Carrier Board transmit path. The Carrier Board transmit path insertion loss budget ***shall*** be 9.49 dB (8.30 dB + 1.19 dB). The Carrier Board receive path insertion loss ***shall*** be 8.30 dB. COM Express connector loss is accounted for separately.

Table 5.11: PCI Express Insertion Loss Budget, 2.5 GHz with Carrier Board PCIE Device

Segment	max. Length [mm/inches]	Notes
L_A	127/5.0	Allowance for Module trace. Coupling cap effects included within simulation.
L_B		COM Express connector simulated at 2.5 GHz.
L_C	203/8.0	Allowance for Carrier Board trace.
Total	330/13.0	PCIe GEN2 Data clocked architecture

For “device down” PCIe Gen 2 operation, the Module PCIe maximum trace length is restricted to 5.0 inches and the Carrier Board maximum trace to 8.0 inches. Shorter lengths will yield additional margin and are encouraged where possible. Results assumed FR4 dielectrics. Other dielectrics with lower losses could be considered, but were not simulated.

5.4.3 SATA Insertion Loss Budget

The Serial ATA source specification provides insertion loss figures only for the SATA cable. There are several cable types defined with insertion losses ranging from 6 dB up to 16 dB. Cross talk losses are separate from material losses in the SATA specification.

The COM Express SATA Insertion loss budgets presented below represent the material losses and do not include cross talk losses. The COM Express SATA Insertion loss budgets are a guideline: Module and Carrier Board vendors ***should not*** exceed the values shown in the tables below.

Figure 5-3: SATA Insertion Loss Budget

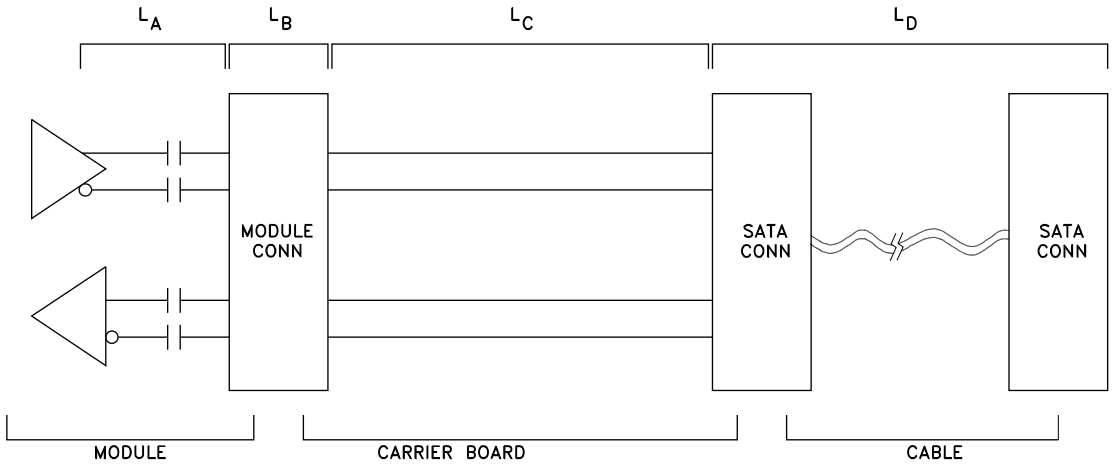


Table 5.12: SATA Gen 1 Insertion Loss Budget, 1.5 GHz

Segment	Loss (dB)	Notes
L_A	1.26	Up to 3.0 inches of Module trace @ 0.28 dB / GHz / inch
Coupling Caps	0.40	
L_B	0.25	COM Express connector at 1.5 GHz measured value
L_C	3.07	Up to 7.2 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	6.00	Source specification cable and cable connector allowance
Total	10.98	

Table 5.13: SATA Gen 2 Insertion Loss Budget, 3.0 GHz

Segment	Loss (dB)	Notes
L_A	1.68	Up to 2.0 inches of Module trace @ 0.28 dB / GHz / inch
Coupling Caps	0.40	
L_B	0.38	COM Express connector at 3.0 GHz measured value
L_C	2.52	Up to 3.0 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	6.00	Source specification cable and cable connector allowance
Total	10.98	

5.4.4 USB 2.0 Insertion Loss Budget

Figure 5-4: USB 2.0 Insertion Loss Budget

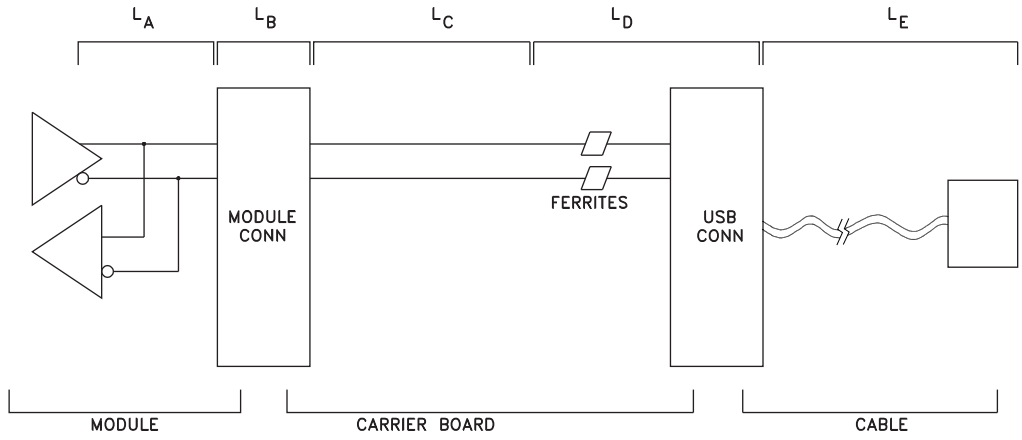


Table 5.14: USB Insertion Loss Budget, 400 MHz

Segment	Loss (dB)	Notes
L_A	0.67	Up to 6 inches of Module trace @ 0.28 dB / GHz / inch
L_B	0.05	COM Express connector at 400 MHz measured value
L_C	1.68	Up to 14 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	1.00	USB connector and ferrite loss
L_E	5.80	USB cable and far end connector loss, per source specification
Total	9.20	

COM Express USB implementations ***should*** conform to insertion loss values less than or equal to those shown in the table above. The insertion loss values shown account for frequency dependent material losses only. Cross talk losses are separate from material losses in the USB specification.

"Device Down" implementations, in which the USB target device is implemented on the Carrier Board, ***may*** add the ferrite and USB connector insertion loss values to the Carrier Board budget. The Carrier Board insertion loss budget then becomes $L_C + L_D$, or 2.68 dB.

5.4.5 SuperSpeed USB Insertion Loss Budget

Figure 5-5: SuperSpeed USB Insertion Loss Budget

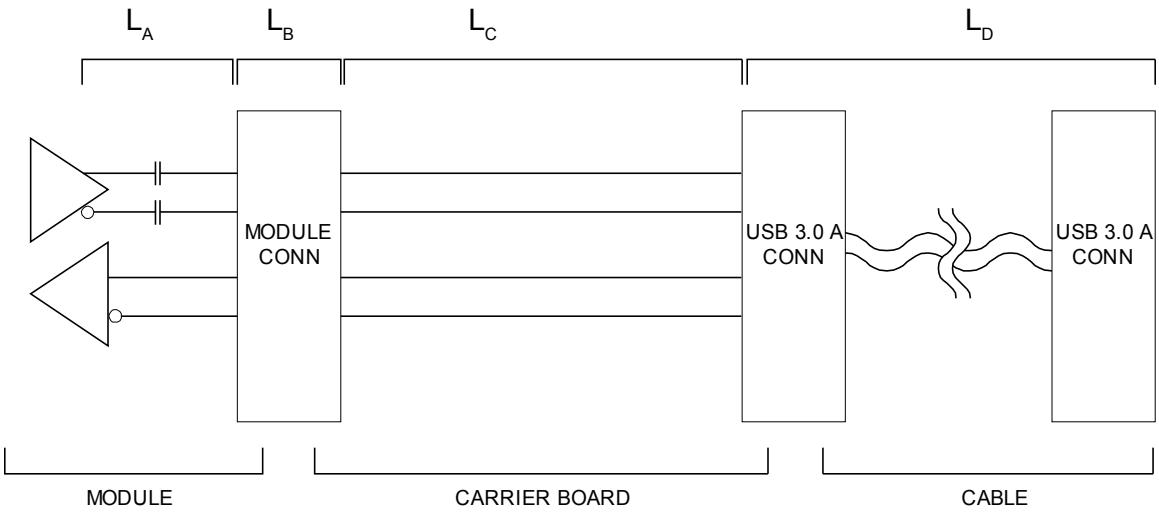


Table 5.15: SuperSpeed USB Insertion Loss Budget

Segment	Loss (dB)	Notes
L_A	1.94	Up to 3 inches of Module trace @ 2.5 GHz
L_B	1.20	COM Express connector at 2.5 GHz
L_C	3.64	Up to 5 inches of Carrier Board trace @ 2.5 GHz with Common-Mode Component
Total	6.78	

5.4.6 10/100/1000 Ethernet Insertion Loss Budget

Figure 5-6: 10/100/1000 Ethernet Insertion Loss Budget

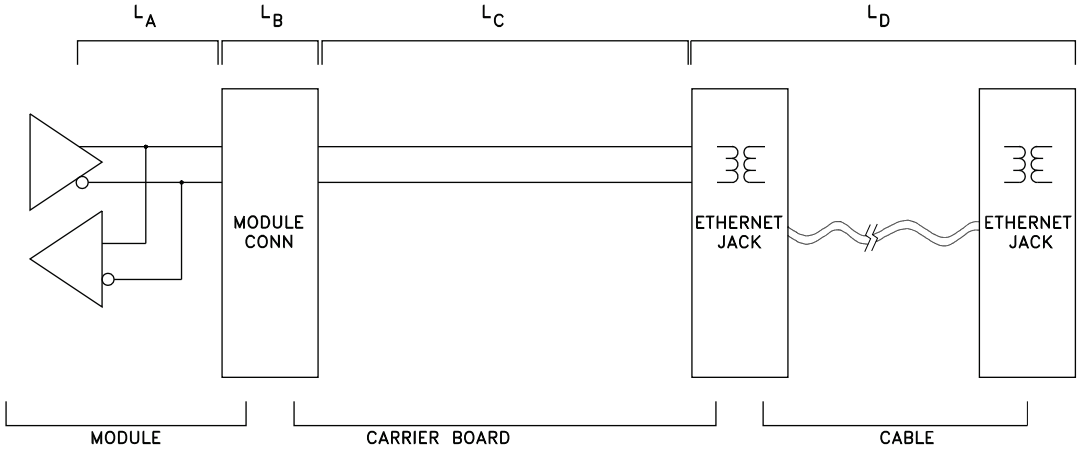


Table 5.16: 10/100/1000 Ethernet Insertion Loss Budget, 100 MHz

Segment	Loss (dB)	Notes
L_A	0.08	Up to 3 inches of Module trace @ 0.28 dB / GHz / inch
L_B	0.02	COM Express connector at 100 MHz measured value
L_C	0.15	Up to 5 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	24.00	Cable and cable connectors, integrated magnetics, per source spec.
Total	24.25	

COM Express Ethernet implementations ***should*** conform to insertion loss values less than or equal to those shown in the table above. The insertion loss values shown account for frequency dependent material losses only. Cross talk losses are separate from material losses in the Gb Ethernet specification.

"Device Down" implementations, in which the Ethernet target device is implemented on the Carrier Board (for instance, an Ethernet switch), ***may*** add the insertion loss for the RJ45 Ethernet jack and integrated magnetics to the Carrier Board budget. This insertion loss value is typically 1 dB. The Carrier Board insertion loss budget then becomes L_C + 1 dB, or 1.15 dB.

5.4.7 DDI Loss Budget

The DDI signals can be used to support a variety of video interfaces. The circuits required to realize the different video interfaces will be determined by a future PICMG Carrier Design Guide subcommittee. At this time, the only requirement placed on Modules for the DDI signals is the maximum trace length specified below.

Figure 5-7: DDI Loss Budget

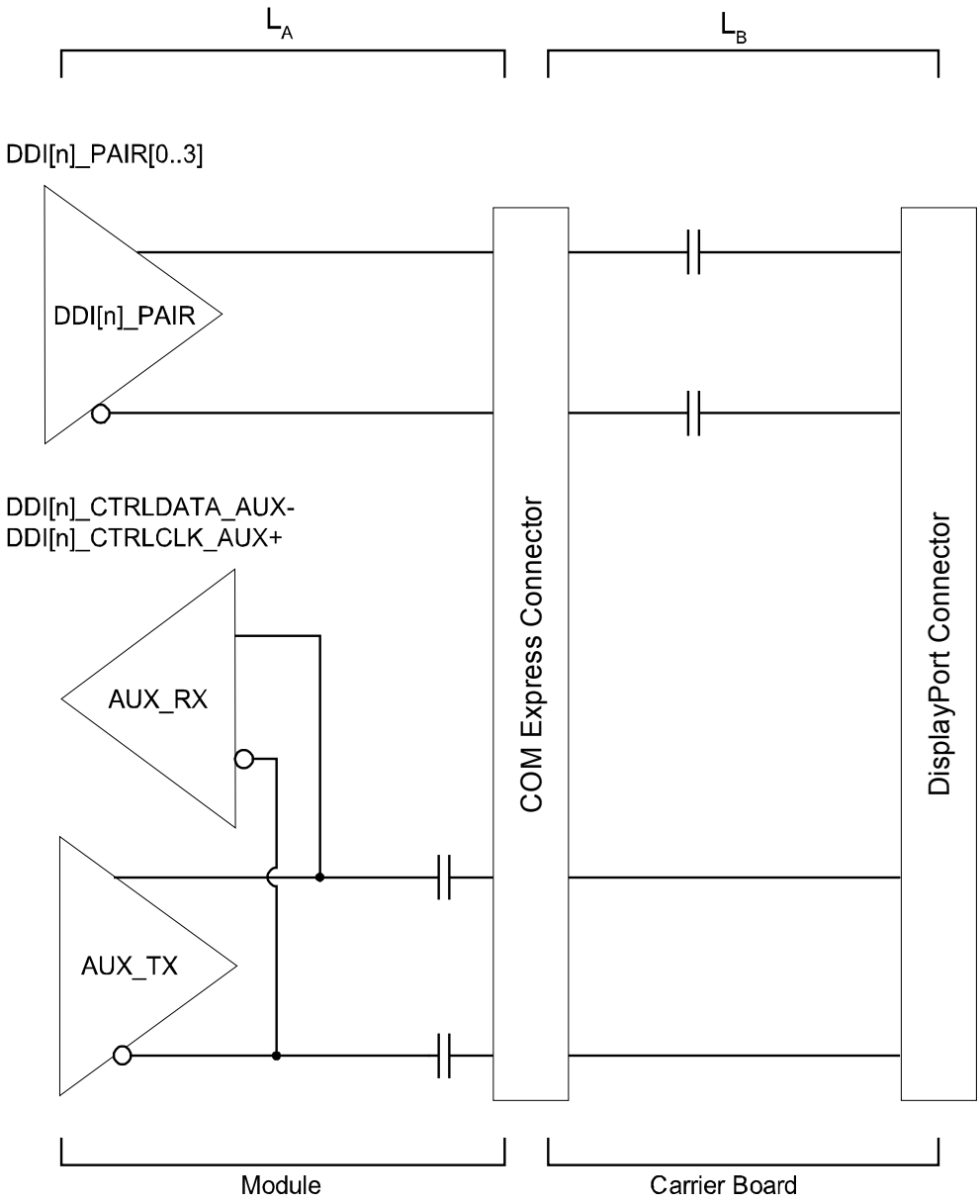
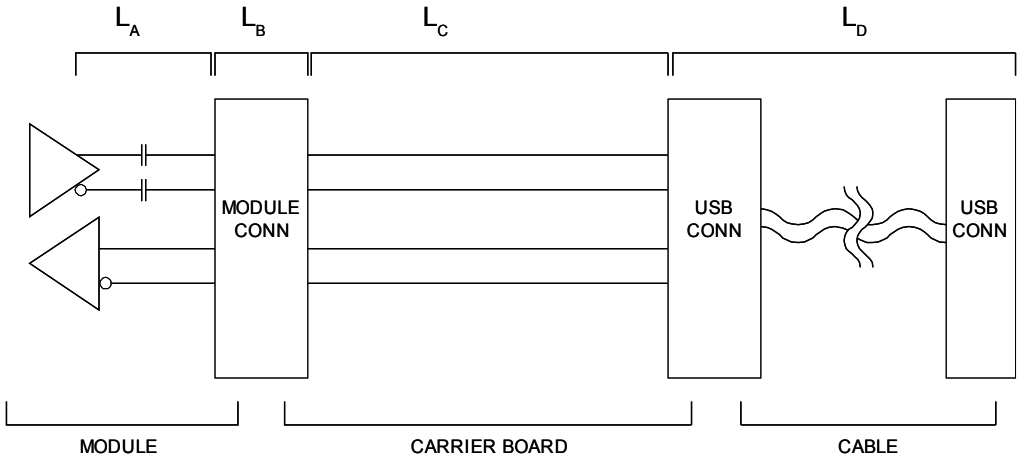


Figure 5-7 above shows a DisplayPort implementation. The DDI can also support SDVO and TMDS. Depending on the type of video interface desired, there ***may*** be level shifters on the Carrier.

Requirements:

- DDI[n]_PAIR[0..3] L_A ***should*** be less than 4.0". L_A is defined as the total Module trace length from the silicon to the COM Express connector including any blocking capacitors that might be required.
- DDI[n]_PAIR[0..3] L_B ***should*** be less than 5.0". L_B is defined as the total trace length on the Carrier from the COM Express connector to the display connector or level shifter including any blocking capacitors that might be required.
- DDI[n]_CTRLDATA_AUX- / DDI[n]_CTRLCLK_AUX+ L_A ***should*** be less than 7.0". L_A is defined as the total Module trace length from the silicon to the COM Express connector including any blocking capacitors that might be required.
- DDI[n]_CTRLDATA_AUX- / DDI[n]_CTRLCLK_AUX+ L_B ***should*** be less than 5.0". L_B is defined as the total trace length on the Carrier from the COM Express connector to the display connector or level shifter including any blocking capacitors that might be required.



5.5 PCI Bus Implementation

5.5.1 Carrier Board PCI Resource Allocation

On COM Express Modules with Type 2 and 3 pin-outs, four Carrier Board PCI targets ***shall*** be supported, referenced as Slot 0, 1, 2, and 3 devices. They ***may*** be PCI slots (connectors) on the Carrier Board, or they ***may*** be actual PCI devices on the Carrier Board itself. The PCI implementation ***shall*** support four REQ / GNT pairs for off-Module use.

The interrupts in Table 5.12 are PCI interrupts defined by the PCI SIG specification and not meant to imply direct connection to the legacy ISA IRQ lines.

The following table summarizes how resources are allocated on a Carrier Board implementation.

Table 5.17: Carrier Board PCI Resource Allocation

Slot / Device Signal	Slot / Device 0	Slot / Device 1	Slot / Device 2	Slot / Device 3
IDSEL	PCI_AD[20]	PCI_AD[21]	PCI_AD[22]	PCI_AD[23]
PCI Clock	PCI_CLK replica	PCI_CLK replica	PCI_CLK replica	PCI_CLK replica
INTA#	PCI_IRQ[A]#	PCI_IRQ[B]#	PCI_IRQ[C]#	PCI_IRQ[D]#
INTB# (if used)	PCI_IRQ[B]#	PCI_IRQ[C]#	PCI_IRQ[D]#	PCI_IRQ[A]#
INTC# (if used)	PCI_IRQ[C]#	PCI_IRQ[D]#	PCI_IRQ[A]#	PCI_IRQ[B]#
INTD# (if used)	PCI_IRQ[D]#	PCI_IRQ[A]#	PCI_IRQ[B]#	PCI_IRQ[C]#
REQ#	PCI_REQ[0]#	PCI_REQ[1]#	PCI_REQ[2]#	PCI_REQ[3]#
GNT#	PCI_GNT[0]#	PCI_GNT[1]#	PCI_GNT[2]#	PCI_GNT[3]#

5.5.2 PCI Clocks

COM Express specifies only a single copy of the PCI clock for Carrier Board target device use. If only one Carrier Board PCI device is implemented, then that single clock ***may*** be routed to the device. If more than one Carrier Board PCI device is implemented, then the Carrier Board ***should*** replicate the PCI clock using a zero delay buffer. The zero delay buffer if used ***should*** support spread spectrum clocking. See the Carrier Design Guide for specific recommendations of buffers that support spread spectrum clocking. The Module EEPROM spread spectrum clocking bit ***should*** be set appropriately so that the Module can determine the capabilities of the Carrier Board.

The PCI Local Bus Specification requires that PCI clocks be synchronous within a 2 ns window at the destination devices; that the maximum propagation delay for the clock be 10 ns, and that PCI slot based add-on cards implement a PCI clock trace length of 2.5 inches.

COM Express Carrier Board implementations ***should*** allow 1.6 ns +/- 0.1 ns for the PCI clock propagation delay from the COM Express Module connector pin to the destination device pin.

Propagation delay varies with construction details such as trace geometry, PCB stack up, and PCB material dielectric constant. Propagation delay values of 140 ps / inch to 180 ps / inch are common for outer layer traces. A propagation delay value of 180 ps / inch is common for inner layer traces. Using 180 ps /inch as the propagation delay value for an inner layer Carrier Board PCI clock, then the COM Express Carrier Board delay of 1.6 ns works out to 8.88 inches of trace.

If the destination device is on an add on card, then the propagation delay associated with the 2.5 inches of add on card trace are deducted from the 1.6 ns. Using 160 ps / inch as a typical value for an outer layer slot card clock trace, the 2.5 inches of slot card clock trace length work out to a propagation delay of 0.4 ns. The Carrier Board PCI clock delay in this example would be 1.6 ns – 0.4 ns or 1.2 ns.

The following definitions and equations apply:

T_{MD} Propagation delay:
Module PCI clock source to on-Module PCI device

T_{MC} Propagation delay:
Module PCI clock source to Module connector PCI clock pin

T_{CD} Propagation delay: Module connector to Carrier Board device
Fixed by COM Express Specification at 1.6 ns

T_{CS} Propagation delay: Module connector to slot connector pin

L_{SD} Length: slot card connector pin to slot card device
Fixed by PCI Local Bus Specification at 2.5 inches

P_{SD} Inverse propagation speed:
slot card connector pin to slot card device
(units of time / length)
Determined by slot card PCB design; typical value 160 ps / inch

$T_{MD} = T_{MC} + T_{CD}$

$T_{MD} = T_{MC} + T_{CS} + L_{SD} * P_{SD}$

$T_{CS} = T_{CD} – L_{SD}*P_{SD}$

The parameters T_{MD} and T_{MC} apply to Module designs. Module designers ***should*** minimize T_{MC}, and then arrange that T_{MD} satisfies the relation $T_{MD} = T_{MC} + T_{CD}$.

Figure 5-8: PCI Clocks - Carrier Board PCI Device

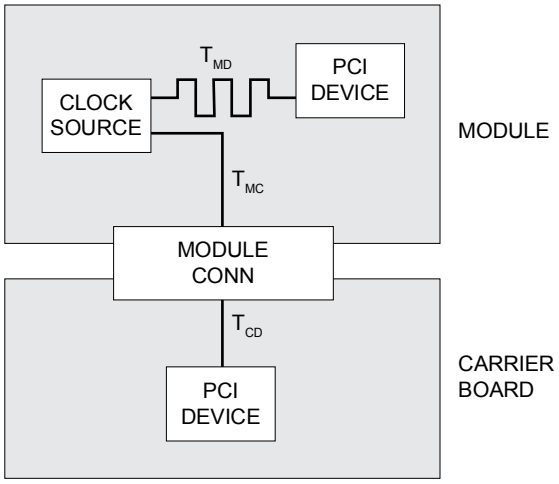
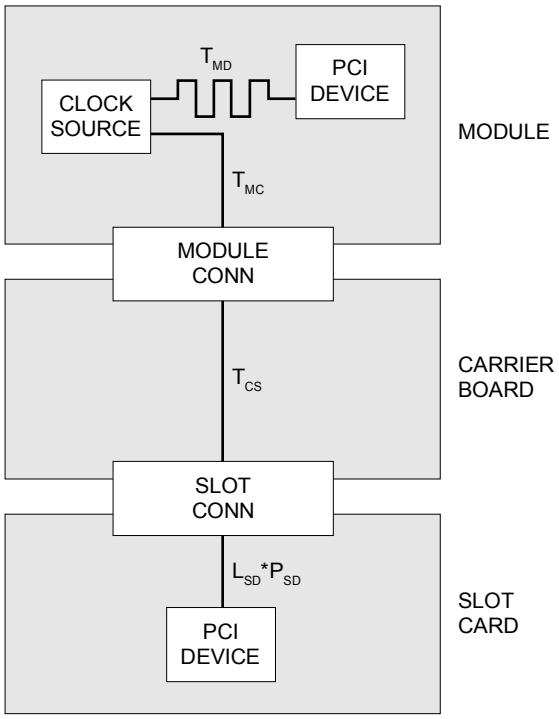


Figure 5-9: PCI Clocks - Slot Card PCI Device



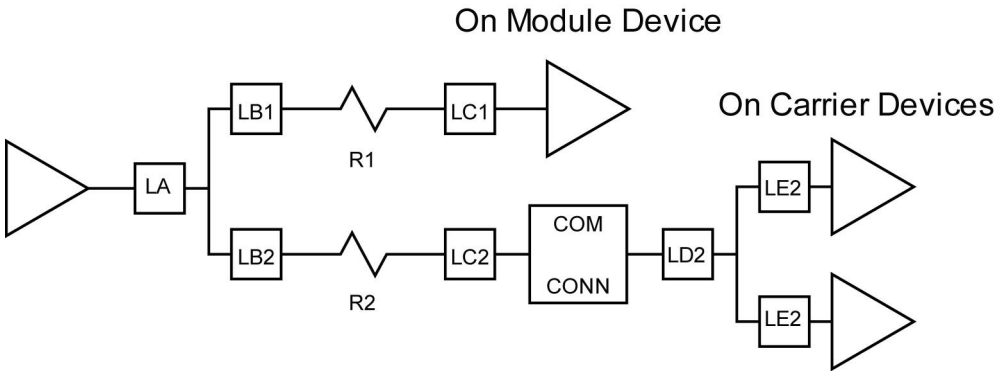
5.6 Carrier Board LPC Devices

Carrier Board LPC devices ***should*** be clocked with the LPC clock provided by the Module interface. If the Carrier Board has two loads on the LPC clock these loads ***should*** be connected to the common clock without a buffer. The Carrier Board ***should*** not have more than two loads on the LPC clock.

Carrier Board LPC devices ***should*** be reset with signal CB_RESET#.

A typical routing topology for a Module LPC device and two Carrier Board LPC devices clock is shown below. This topology is used by Modules that start and stop the LPC clock on the fly. In this case, a buffer cannot be used and all LPC devices must share a common clock.

Figure 5-10: Typical routing topology for a Module LPC device



LA 500 mils max

LB1 = LB2 = 150 mils max

LC1 = 8.88”+LC2

LC2 = .25” max

LE2 = 1” max

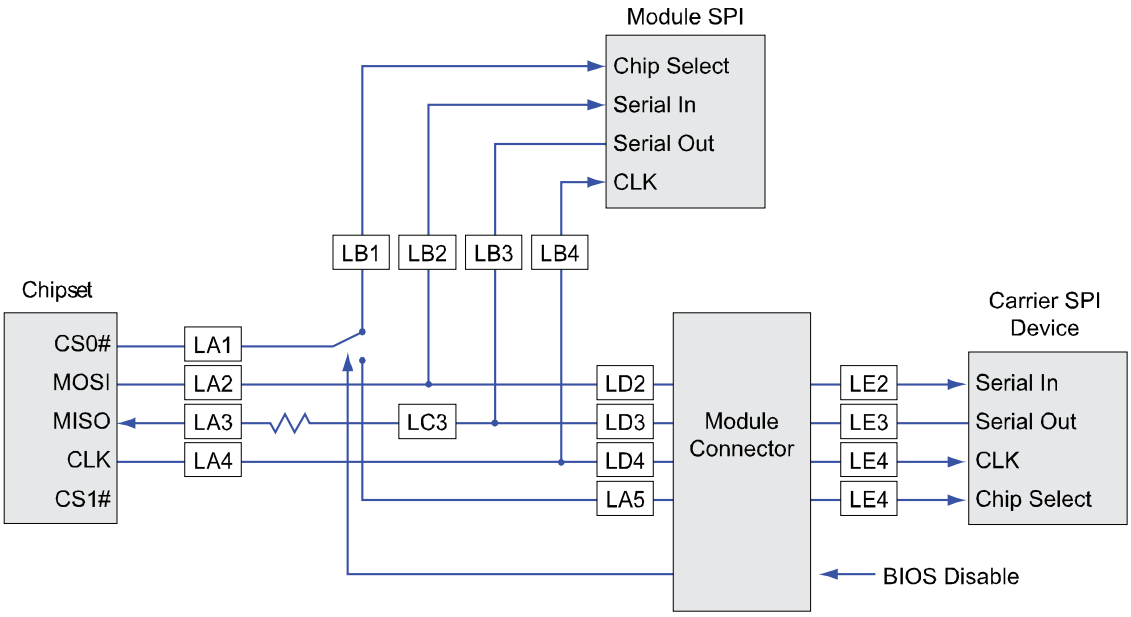
LD2 + LE2 (note 2 instances of LE2) = 8.88”

R1 = R2 = 22Ω

5.7 SPI Devices

All Module types ***may*** implement a SPI bus. The SPI bus is replacing the LPC bus for BIOS EEPROM devices. If a Module supports an external BIOS it ***shall*** support an external SPI BIOS and ***may*** support an external LPC BIOS. The diagram below depicts a typical SPI topology. Note that other SPI configurations are possible including Module or Carrier based CS1# SPI device. Refer to Section 4.3.12 'SPI Interface' for other implementation options.

Figure 5-11: Typical SPI topology



(LA1 + LB1), (LA2 + LB2), (LA3 + LC3 + LB3), (LA4 + LB4) max length 2” match all within .1”
LD2, LD3, LD4, LD5 max length .25” (maximum stub length to COM.0 connector)
LE2, LE3, LE4, LE5 max length 4.5” match within .1”
(LA4 + LB4), (LA2 + LB2) match within .5” (match CLK & MOSI within .5” Module)
(LA4 + LD4), (LA2 + LD2) match within .4” (match CLK & MOSI within .5” Carrier Board)
(LA4 + LB4), (LA1 + LB1) match within .5” (match CLK & CS within .5” Module)
(LA4 + LD4), (LA1 + LA5) match within .4” (match CLK & CS within .5” Carrier Board)
R1 = 33Ω

5.8 10 Gigabit Ethernet Option

Modules that use Pin-out Type 3 or 5 ***may*** implement a 10 Gigabit / sec Ethernet option by remapping the pins used for the GBE1 and GBE2 ports. The 10 Gigabit pin usage is to be defined in a future specification update.

Table 5.18: 10 Gigabit Ethernet Pin Mapping

Row C Pin	GBE1 Pin Use	10 Gigabit Pin Use
C1	GND(FIXED)	GND
C2	GBE1_ACT#	To be defined in a future COM Express Revision
C3	GBE1_MDI3-	
C4	GBE1_MDI3+	
C5	GBE1_LINK100#	
C6	GBE1_MDI2-	
C7	GBE1_MDI2+	
C8	GBE1_LINK1000#	
C9	GBE1_MDI1-	
C10	GBE1_MDI1+	
C11	GND(FIXED)	GND
DL0-	GBE1_MDI0-	
DL0+	GBE1_MDI0+	
GND	GBE1_LINK#	
NC	RSVD	

Row D Pin	GBE2 Pin Use	10 Gigabit Pin Use
D1	GND(FIXED)	GND
D2	GBE2_ACT#	To be defined in a future COM Express Revision
D3	GBE2_MDI3-	
D4	GBE2_MDI3+	
D5	GBE2_LINK100#	
D6	GBE2_MDI2-	
D7	GBE2_MDI2+	
D8	GBE2_LINK1000#	
D9	GBE2_MDI1-	
D10	GBE2_MDI1+	
D11	GND(FIXED)	GND
D12	GBE2_MDI0-	
D13	GBE2_MDI0+	
D14	GBE2_LINK#	
D15	GBE2_CTREF	

5.9 Watchdog Timer

COM Express Modules ***may*** implement a watchdog timer output to the Carrier Board.

5.9.1 Output Modes and Characteristics

The support of a watch dog timer on the Module is optional. If a Module supports a watchdog timer it ***shall*** minimally support output mode 1 and ***may*** also support output modes 2 or 3 as defined below. The selection of the output modes ***may*** be realized by software configurable hardware or by Module build options.

Table 5.19: Watchdog Timer Output Modes

Output Mode	Description
1	The Module generates an internal reset. Module pins PCI_RST#, IDE_RST, and CB_RESET# that are supported are pulsed low. WDT pin is driven high until the unit resets.
2	The Module only drives WDT pin high until cleared by Module software.
3	The Module generates an NMI. WDT pin is driven high until cleared by Module software.

The watchdog output ***shall*** come up as a logic low and ***shall*** be disabled upon power-on-reset (VCC_12V power cycle) or external system reset (when SYS_RST# pin is toggled low by external hardware). The watchdog ***may*** be enabled by BIOS or system software.

5.9.2 Watchdog Enable and Strobe

Typically, the watchdog parameters (output options, enabling, enable delay, timeout delay) are managed by the Module BIOS, often via a BIOS setup screen. The regular watchdog strobes to prevent a watchdog timeout are typically handled by the Module's application software. There ***may*** be BIOS abstractions to isolate the application software from the watchdog hardware.

The software programmable Watchdog Enable Delay is the time between when the watchdog is enabled by firmware and when the first watchdog strobe is needed to prevent a watchdog time out. The enable delay allows time for the operating system to boot and the application to load and initialize.

After the initial Enable Delay, the enabled watchdog must be periodically strobed by software to prevent a watchdog timeout. The Strobe Interval ***shall*** be software programmable.

Recommended ranges in enable delay and max strobe periods are given in the following table.

Table 5.20: Watchdog Enable and Strobe Parameter Range

	Min Value	Max Value
Enable Delay	1 second	10 minutes
Strobe Interval	0.1 second	10 minutes

5.10 Protecting COM.0 Pins Reclaimed From the VCC_12V Pool

The COM.0 Rev. 2 Type 6 and Type 10 pin-out types introduce eight signals that are mapped to pins that are re-claimed from pins that are VCC_12V supply pins on Type 1,2,3,4 and 5 Modules. These signals include

- SER0_TX, SER1_TX TTL level outputs from the Module
- SER0_RX, SER1_RX TTL level inputs to the Module
- LID#, SLEEP# 3.3V logic level inputs to the Module, in the suspend domain
- FAN_TACHIN 3.3V logic level input to the Module
- FAN_PWMOUT 3.3V logic level output from the Module

A new Type strap pin is also introduced in COM.0 Rev 2, for all Module Types. It also falls on a pin that was used exclusively for VCC_12V in COM.0 Rev. 1:

- TYPE10# VCC_12V on COM.0 Rev. 1 Module Types 1,2,3,4,5
  No connect on COM.0 Rev. 2 Module Types 1,2,3,4,5,6
  47K Module pull-down to GND on Module Type 10

All nine of the signals referenced above on COM.0 Rev. 2 compliant Module and Carrier designs ***shall*** be able to withstand continuous direct connections to low impedance 12V sources (i.e. a short to a 12V power supply).

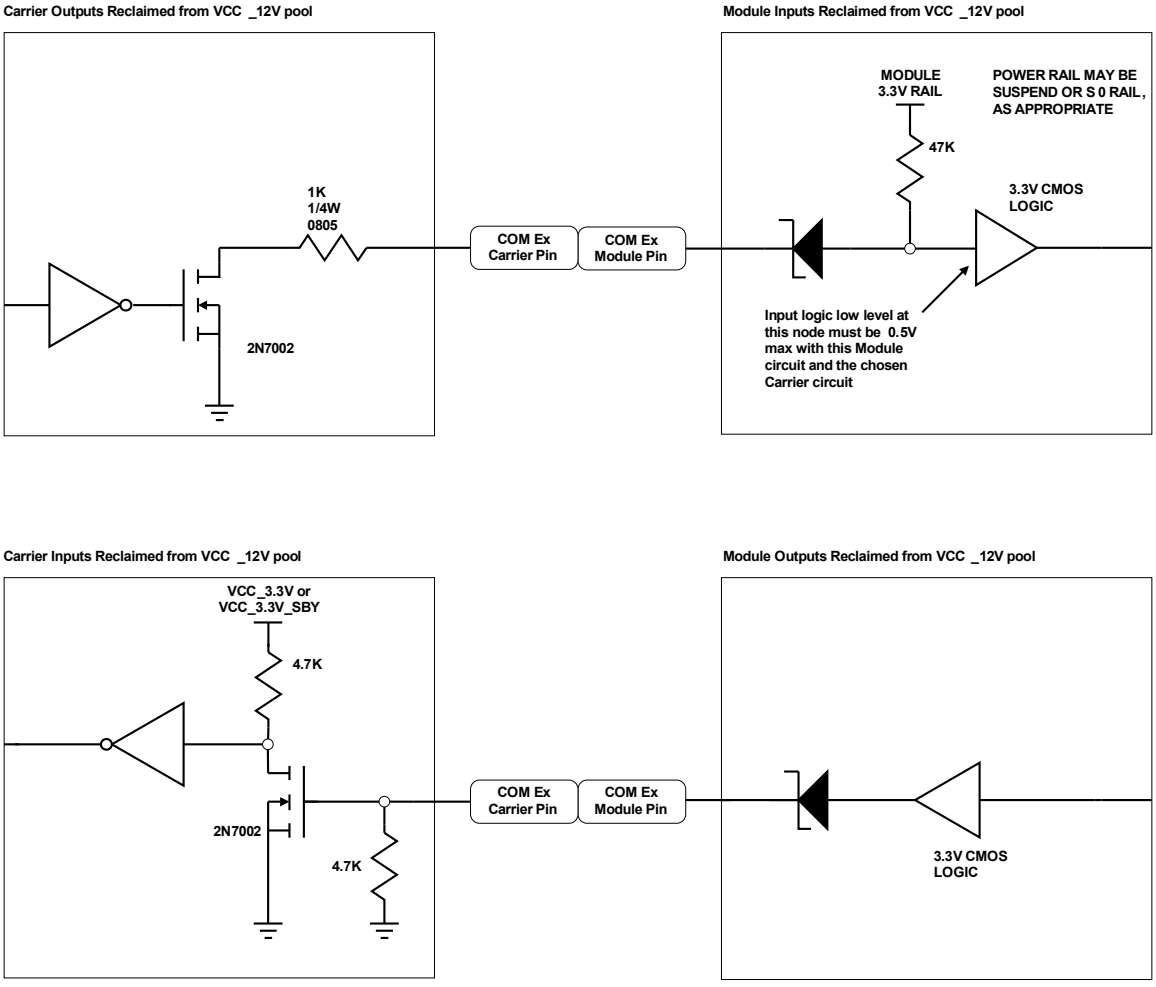
One line of defense against such unintended connections is for Carrier designs to decode the Module TYPE pins (3 pins on the C-D connector, and the new TYPE10# pin on the A-B connector) and to not power the system up if an improper Module Type is detected. Examples of this may be found in the PICMG Carrier Design Guide. However, there are some situations in which this can not be relied upon. One such situation is if a user plugs a Type 10 Module into a Rev. 1 Type 1 Carrier. Since the TYPE10# strap was not anticipated in the Rev. 1 Carrier, the Carrier will apply power to the Type 10 Module. Thus it is very important that Type 10 and 6 Modules be able to withstand 12V exposure to the pins reclaimed from the VCC_12V pool.

5.10.1 Logic Level Signals on Pins Reclaimed from VCC_12V

Module logic level inputs and outputs that are implemented on pins reclaimed from the VCC_12V pool ***shall*** implement the series Schottky diode protection shown in the right side of the figure below. The Schottky diode ***should*** be a BAT54 device. For inputs in this group, a 47K pull-up to the local 3.3V S0 or S5 rail (as appropriate) ***shall*** be used.

Carrier Board logic level inputs and outputs that are implemented on pins reclaimed from the VCC_12V pool ***shall*** be protected against protracted accidental exposure to 12V. The protection scheme shown in the left side of the Figure 5-12 below ***may*** be used. Any scheme that is used ***shall*** be able to pull the reclaimed Module input low enough such that Module CMOS input logic sees a maximum voltage of 0.5V for a logic low, as indicated in the figure.

Figure 5-12: Protecting Logic Level Signals on Pins Reclaimed from VCC_12V



5.10.2 TYPE10# Strap - Reclaimed from VCC_12V

No additional protection is needed for the TYPE10# strap on the Module side:

- On Type 10 Modules, this pin is tied through a 47K resistor to GND. Exposure of this Module pin to 12V is harmless.
- On Rev. 1 Type 1,2,3,4,5 Modules, this pin is tied to VCC_12V already.
- On Rev. 2 Type 1,2,3,4,5 Modules, this pin is a no connect.
- On Type 6 Modules, this pin is a no connect.

On the Carrier side, protection against accidental 12V exposure is required. Carrier Board designs ***shall*** be tolerant of protracted VCC_12V exposure on the TYPE10# pin. A Rev. 1 Type 1 Module, for example, would expose the TYPE10# pin on a Rev. 2 Type 1,2,3,4,5 Carrier to 12V (unless the Carrier design does not allow the system to power up for an incorrect Module type).

The TYPE10# Module pin is, in effect, a tri-level pin: it is tied, depending on Module Type and COM.0 Revision level, to either VCC_12V, to nothing, or to GND through 47K. Carrier Board circuits can be created that distinguish between the 3 levels. If implemented, this would allow the Carrier Board to determine whether a Type 1,2,3,4,5 Module is a built to COM.0 Rev. 1 or Rev. 2. This may be illustrated in a future edition of the PCIMG Carrier Design Guide.

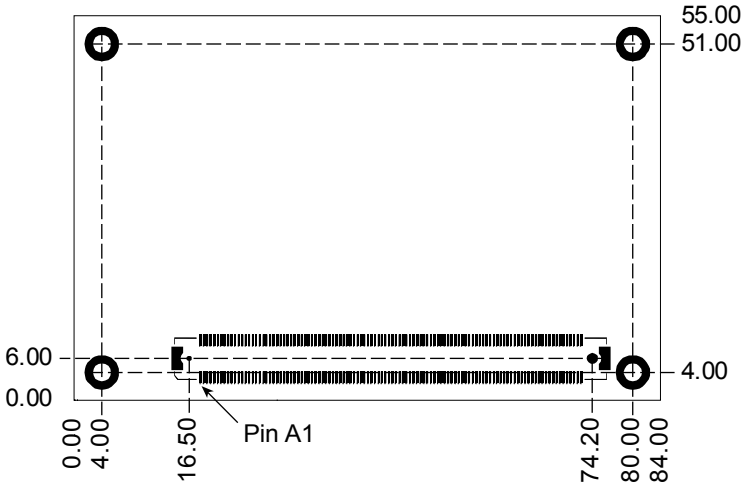
6 Mechanical Specifications

6.1 Module Size – Mini Module

The PCB size for the Mini Module ***shall*** be 84mm x 55mm. The PCB thickness ***should*** be 2mm to allow high layer count stack-ups and facilitate a standard 'z' dimension between the Carrier Board and the top of the heat-spreader (refer to Section 6.10 "Heat-Spreader").

The holes shown in this drawing are intended for mounting the Module / heat-spreader combination to the Carrier Board. An independent, implementation specific set of holes and spacers ***shall*** be used to attach the heat-spreader to the Module.

Figure 6-1: Mini Module Form Factor



All dimensions are shown in millimeters.

Tolerances ***shall*** be ± 0.25mm [±0.010"], unless noted otherwise.

The 220 pin connector pair ***shall*** be mounted on the backside of the PCB and is seen "through" the board in this view.

The four mounting holes shown ***shall*** use 6 mm diameter pads and have 2.7 mm plated holes, for use with 2.5 mm hardware. The pads ***shall*** be tied to the PCB ground plane.

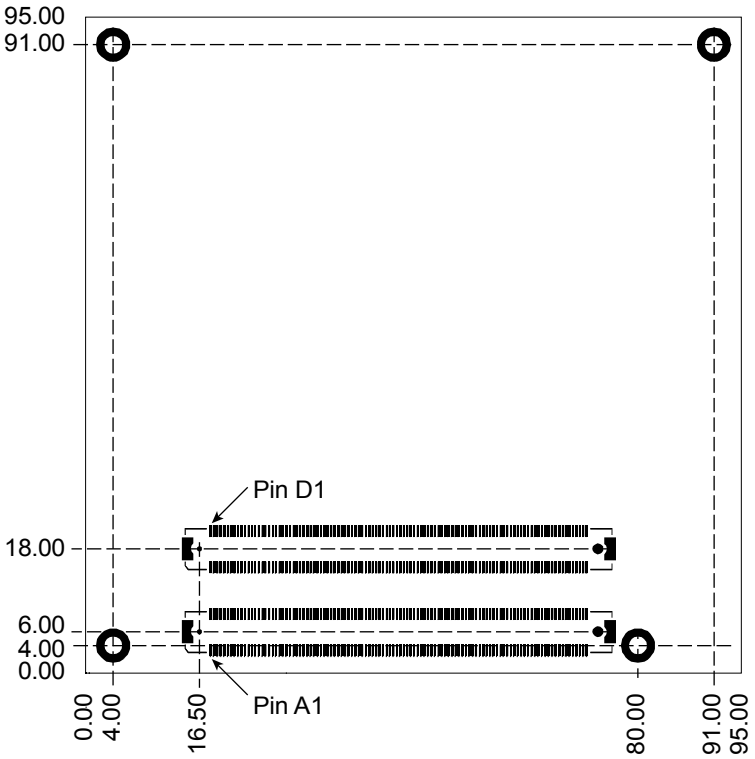
Modules ***shall*** include the 4 mounting holes as shown in Figure 6-1 above. These holes are primarily used to attach the Module to the Carrier.

6.2 Module Size - Compact Module

The PCB size for the Compact Module ***shall*** be 95mm x 95mm. The PCB thickness ***should*** be 2mm to allow high layer count stack-ups and facilitate a standard 'z' dimension between the Carrier Board and the top of the heat-spreader (refer to Section 6.10 "Heat-Spreader").

The holes shown in this drawing are intended for mounting the Module / heat-spreader combination to the Carrier Board. An independent, implementation specific set of holes and spacers ***shall*** be used to attach the heat-spreader to the Module.

Figure 6-2: Compact Module Form Factor



All dimensions are shown in millimeters.

Tolerances ***shall*** be ± 0.25mm [±0.010"], unless noted otherwise.

The 440 pin connector pair ***shall*** be mounted on the backside of the PCB and is seen "through" the board in this view.

The four mounting holes shown ***shall*** use 6 mm diameter pads and have 2.7 mm plated holes, for use with 2.5 mm hardware. The pads ***shall*** be tied to the PCB ground plane.

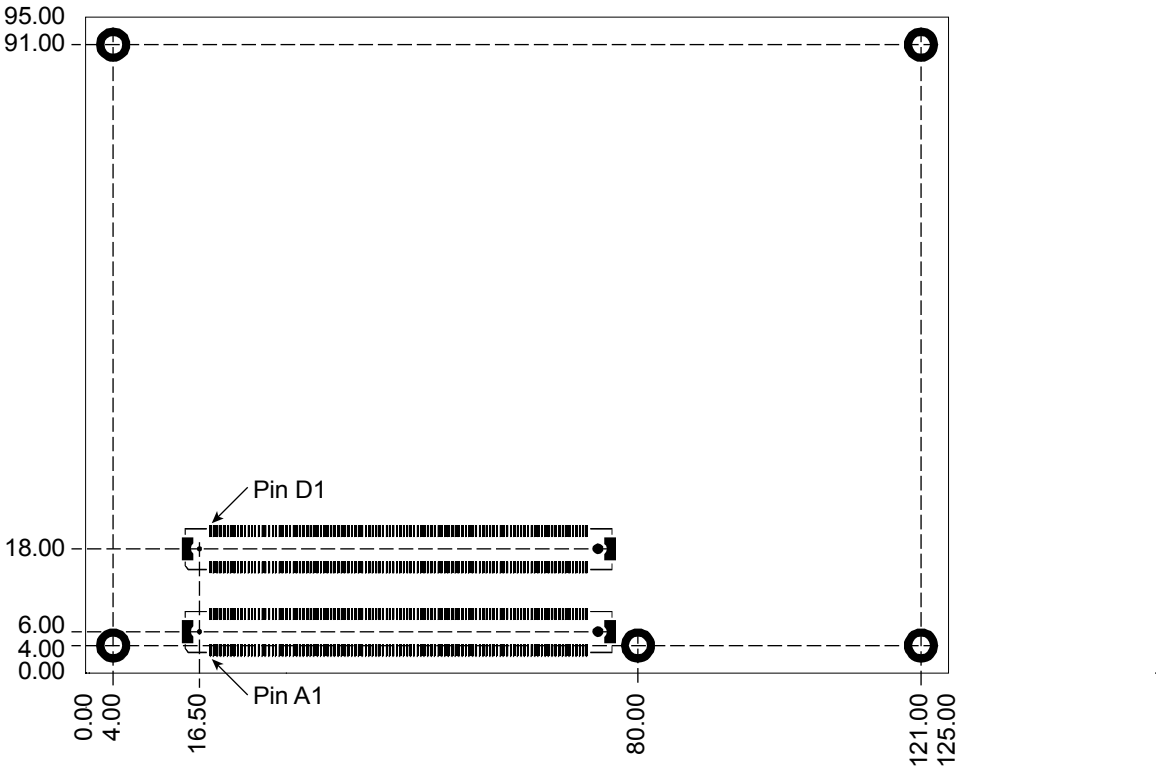
Modules ***shall*** include the 4 mounting holes as shown in Figure 6-2 above. These holes are primarily used to attach the Module to the Carrier.

6.3 Module Size - Basic Module

The PCB size for the Basic Module ***shall*** be 125mm x 95mm. The PCB thickness ***should*** be 2mm to allow high layer count stack-ups and facilitate a standard 'z' dimension between the Carrier Board and the top of the heat-spreader. (refer to Section 6.10 "Heat-Spreader").

The holes shown in this drawing are intended for mounting the Module / heat-spreader combination to the Carrier Board. An independent, implementation specific set of holes and spacers ***shall*** be used to attach the heat-spreader to the Module.

Figure 6-3: Basic Module Form Factor



All dimensions are shown in millimeters.

Tolerances ***shall*** be ± 0.25mm [±0.010"], unless noted otherwise.

The 440 pin connector pair ***shall*** be mounted on the backside of the PCB and is seen "through" the board in this view.

The five mounting holes shown ***shall*** use 6mm diameter pads and ***shall*** have 2.7mm plated holes, for use with 2.5mm hardware. The pads ***shall*** be tied to the PCB ground plane.

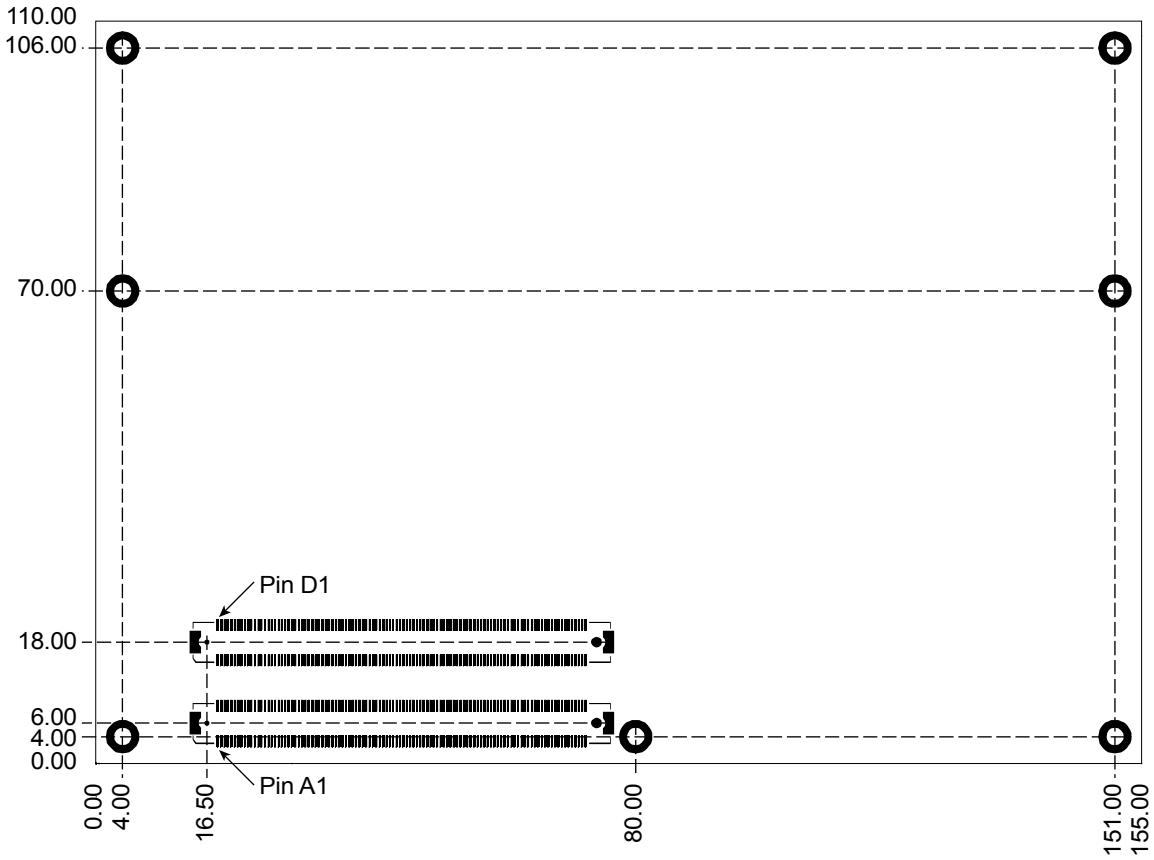
Modules ***shall*** include the 5 mounting holes as shown in Figure 6-3 above. These holes are primarily used to attach the Module to the Carrier.

6.4 Module Size - Extended Module

The PCB size for the Extended Module ***shall*** be 155mm x 110mm. The PCB thickness ***should*** be 2mm to allow high layer count stack-ups and facilitate a standard 'z' dimension between the Carrier Board and the top of the heat-spreader. (refer to Section 6.10 "Heat-Spreader").

The holes shown in this drawing are intended for mounting the Module / heat-spreader combination to the Carrier Board. An independent, implementation specific set of holes and spacers ***shall*** be used to attach the heat-spreader to the Module.

Figure 6-4: Extended Module Form Factor



All dimensions are shown in millimeters.

Tolerances ***shall*** be ± 0.25mm [±0.010"], unless noted otherwise.

The 440 pin connector pair ***shall*** be mounted on the backside of the PCB and is seen "through" the board in this view.

The seven mounting holes shown ***shall*** use 6 mm diameter pads and have 2.7 mm plated holes, for use with 2.5 mm hardware. The pads ***shall*** be tied to the PCB ground plane.

Modules ***shall*** include the 7 mounting holes as shown in Figure 6-4 above. These holes are primarily used to attach the Module to the Carrier.

6.5 Module Connector

The Module connector for Pin-out Types 2 through 6 ***shall*** be a 440-pin receptacle that is composed of 2 pieces of a 220-pin, 0.5 mm pitch receptacle. The pair of connectors ***may*** be held together by a plastic carrier during assembly to allow handling by automated assembly equipment. Module Pin-out Type 1 or 10 ***shall*** use a single 220-pin, 0.5 mm pitch receptacle. The connectors ***shall*** be qualified for LVDS operation up to 6.25GHz, to support PCI Express Generation 2 signaling speeds.

Sources for the individual 220-pin receptacle are

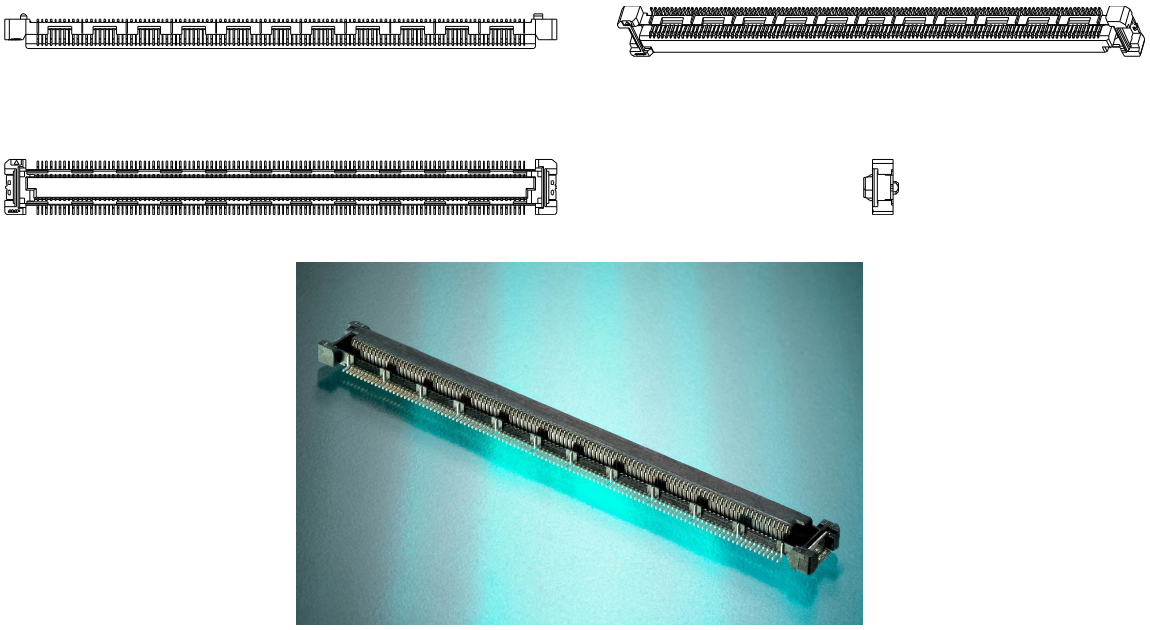
Tyco Electronics	3-6318490-6
Foxconn	QT012206-1031-2H
ept[19]	
or equivalent	0.5 mm pitch Free Height 220 pin 4H Receptacle

Sources for the combined 440-pin receptacle (composed of 2 pieces of the 220 pin receptacle held by a carrier) are:

Tyco Electronics	3-1827231-6
Foxconn	QT012206-1041-3H
ept[19]	
or equivalent	0.5mm pitch Free Height 440 pin 4H Receptacle

The Module connector is a receptacle by virtue of the vendor's technical definition of a receptacle, and to some users it looks like a plug.

Figure 6-5: Module Receptacle



19 *At the time of this writing, EPT is developing a COM Express compatible connector set.*

6.6 Carrier Board Connector

The Carrier Board connector for Module Pin-out Types 2 through 6 ***shall*** be a 440-pin plug that is composed of 2 pieces of a 220-pin, 0.5 mm pitch plug. The pair of connectors ***may*** be held together by a plastic carrier during assembly to allow handling by automated assembly equipment. Carrier Boards intended only for use with Pin-out Type 1 or 10 Modules ***may*** use a single 220-pin, 0.5 mm pitch plug. The connectors ***shall*** be qualified for LVDS operation up to 6.25GHz, to support PCI Express Generation 2 signaling speeds. The Carrier Board plugs are available in a variety of heights. The Carrier Board ***shall*** use either the 5mm or 8mm heights.

Sources for the individual 5 mm stack height 220 pin plug are:

Tyco Electronics	3-1827253-6
Foxconn	QT002206-2131-3H
ept[20]	
or equivalent	0.5 mm pitch Free Height 220 pin 5H Plug

Sources for the combined 5mm stack height 440-pin plug (composed of 2 pieces of the 220 pin plug held by a carrier) are:

Tyco Electronics	3-1827233-6
Foxconn	QT002206-2141-3H
ept[20]	
or equivalent	0.5 mm pitch Free Height 440 pin 5H Plug

Sources for the individual 8 mm stack height 220 pin plug are:

Tyco Electronics	3-6318491-6
Foxconn	QT002206-4131-3H
ept[20]	
or equivalent	0.5 mm pitch Free Height 220 pin 8H Plug

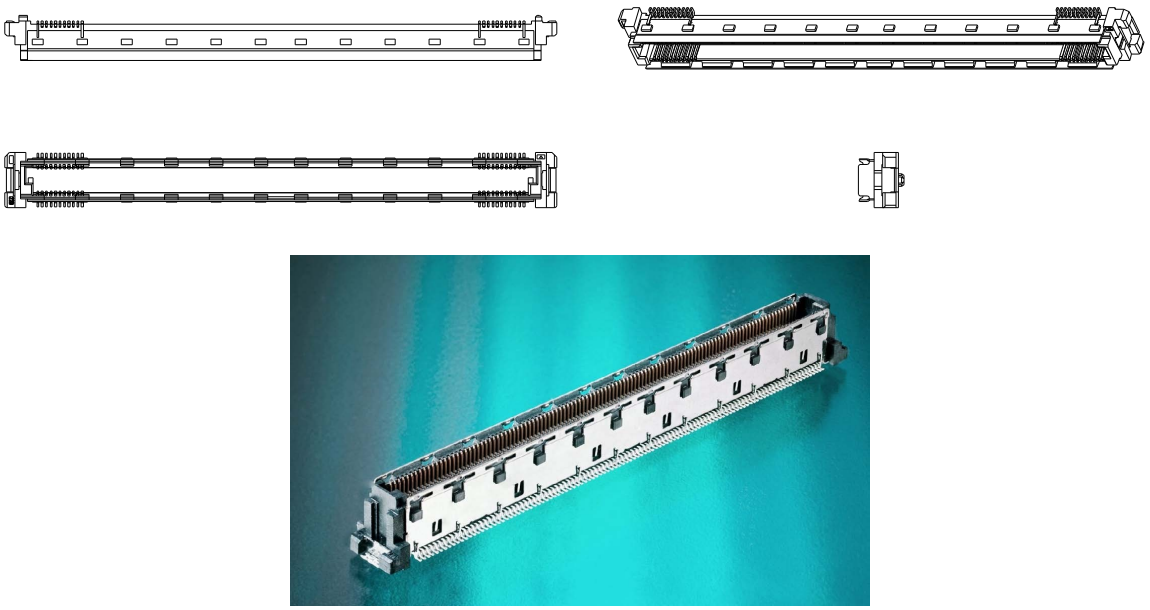
Sources for the combined 8 mm stack height 440 pin plug (composed of 2 pieces of the 220 pin plug held by a carrier) are:

Tyco Electronics	3-5353652-6
Foxconn	QT002206-4141-3H
ept[20]	
or equivalent	0.5 mm Free Height 440 pin 8H Plug or equivalent.

The Carrier Board connector is a plug by virtue of the vendor's technical definition of a plug, and to some users it looks like a receptacle.

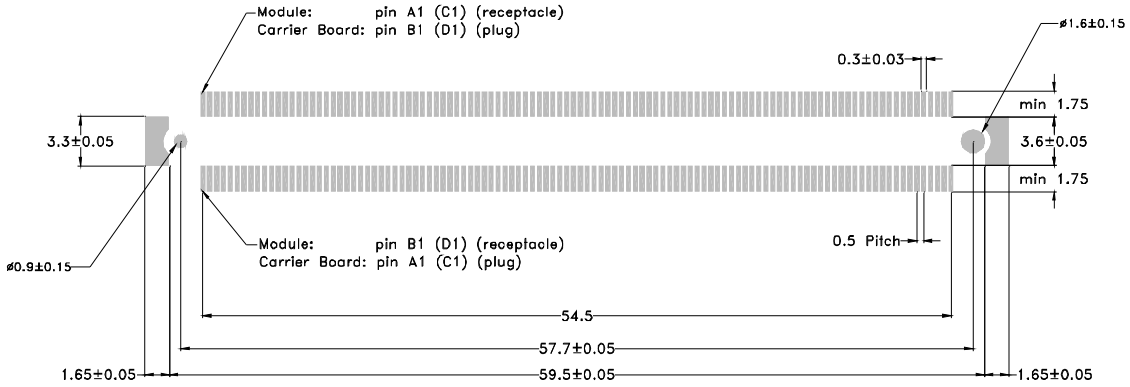
20 *At the time of this writing, EPT is developing a COM Express compatible connector set.*

Figure 6-6: Carrier Board Plug



6.7 Connector PCB Pattern

Figure 6-7: Connector PCB Pattern

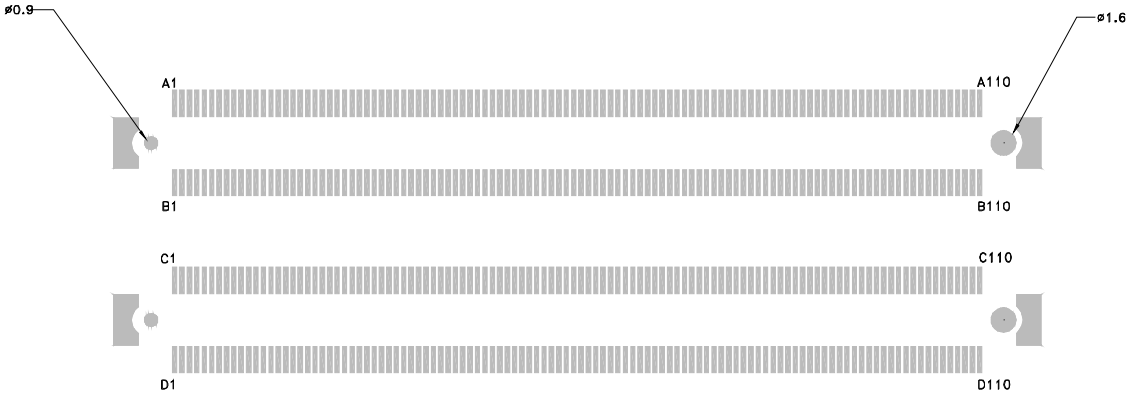


All dimensions in mm.

6.8 Module Connector Pin Numbering

Pin numbering for 440-pin Module receptacle. This is a top view of the receptacle, looking into the receptacle, as mounted on the backside of the Module.

Figure 6-8: Module Connector Pin Numbering

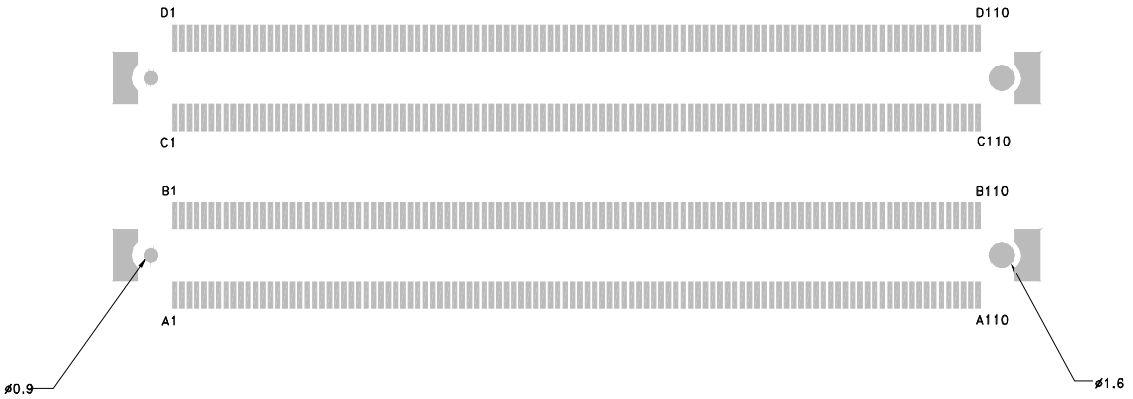


All dimensions in mm.

6.9 Carrier Board Connector Pin Numbering

Pin numbering for 440-pin Carrier Board plug. This is a top view, looking into the plug as mounted on the Carrier Board.

Figure 6-9: Carrier Board Connector Pin Numbering



All dimensions in mm.

6.10 Heat-Spreader

Modules ***should*** be equipped with a heat-spreader. This heat-spreader by it self does not constitute the complete thermal solution for a Module but provides a common interface between Modules and implementation-specific thermal solutions.

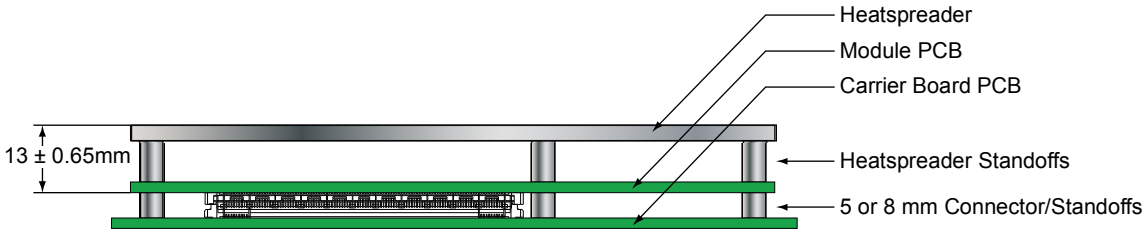
If implemented, a heat-spreader for the Compact, Basic and Extended form factor ***shall*** use and the Mini form factor ***may*** use an implementation specific set of holes and spacers to attach the heat-spreader to the Module. These implementation specific holes are in addition to the Module mounting holes specified in Sections 6.2, 6.3 or 6.4.

For the Compact, Basic and Extended form factor a heat-spreader ***should not*** use the Module mounting holes as the only attachment points to a Module. The intent is to be able to provide a Module and heat-spreader as an assembly that can then be mounted to a Carrier without having to break the thermal interface between the Module components and the heat-spreader.

The standoffs shown in Figure 6-10 ***should*** be mounted on the Carrier Board. The height of the standoff is dependent on the stack height of the Carrier Board connector (5 mm or 8 mm).

The overall Module height from the bottom surface of the Module board to the heat-spreader top surface ***shall*** be 13 mm for the Mini, the Compact, the Basic and the Extended Modules. The Module PCB and heat-spreader plate thickness are vendor implementation specific, however, a 2 mm PCB with a 3 mm heat-spreader ***may*** be used which allows use of readily available standoffs.

Figure 6-10: Overall Height for Heat-Spreader in Mini, Compact, Basic and Extended Modules



All dimensions in mm.

Tolerances (unless otherwise specified):

Z (height) dimensions ***should*** be ± 0.8mm [±0.031”] from top of Carrier Board to top of heat-spreader.

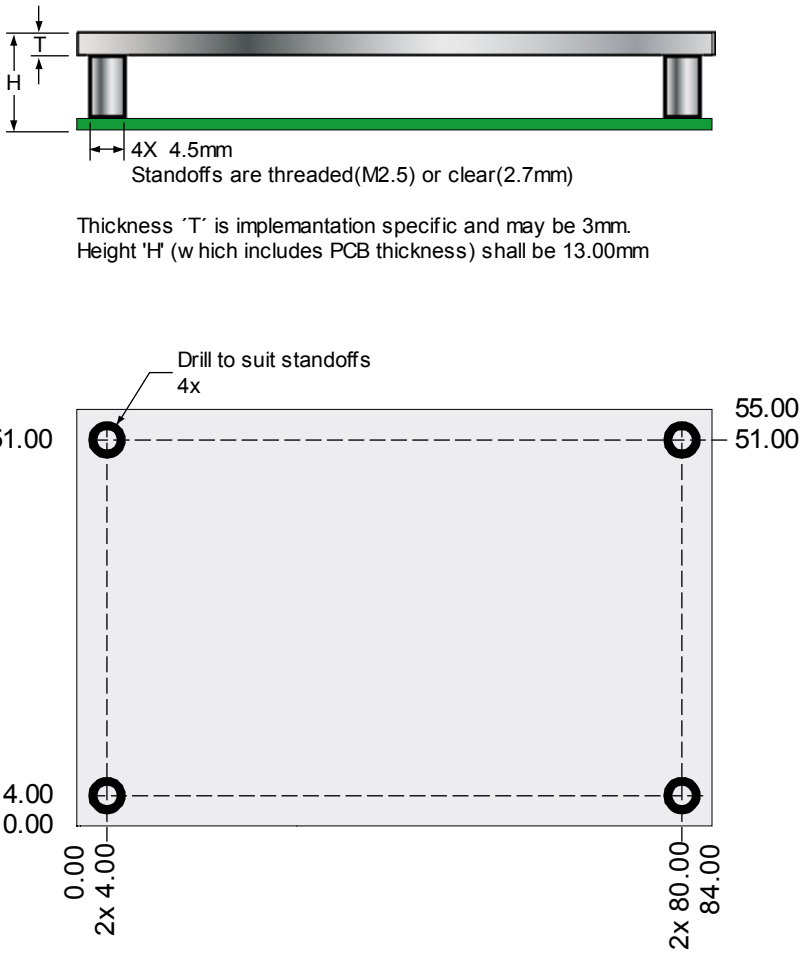
Heat-spreader surface ***should*** be flat within 0.2mm [.008"] after assembly.

Interface surface finish ***should*** have a maximum roughness average (R_a) of 1.6µm [63µin].

The critical dimension in Figure 6-10 is the Module PCB bottom side to heat-spreader top side. This dimension ***shall*** be 13.00mm ± 0.65mm [±0.026”].

Figure 6-10 shows a cross section of a Module and heat-spreader assembled to a Carrier Board using the 5mm stack height option. If 8mm Carrier Board connectors are used, the overall assembly height increases from 18.00mm to 21.00mm.

Figure 6-11: Mini Module Heat-Spreader

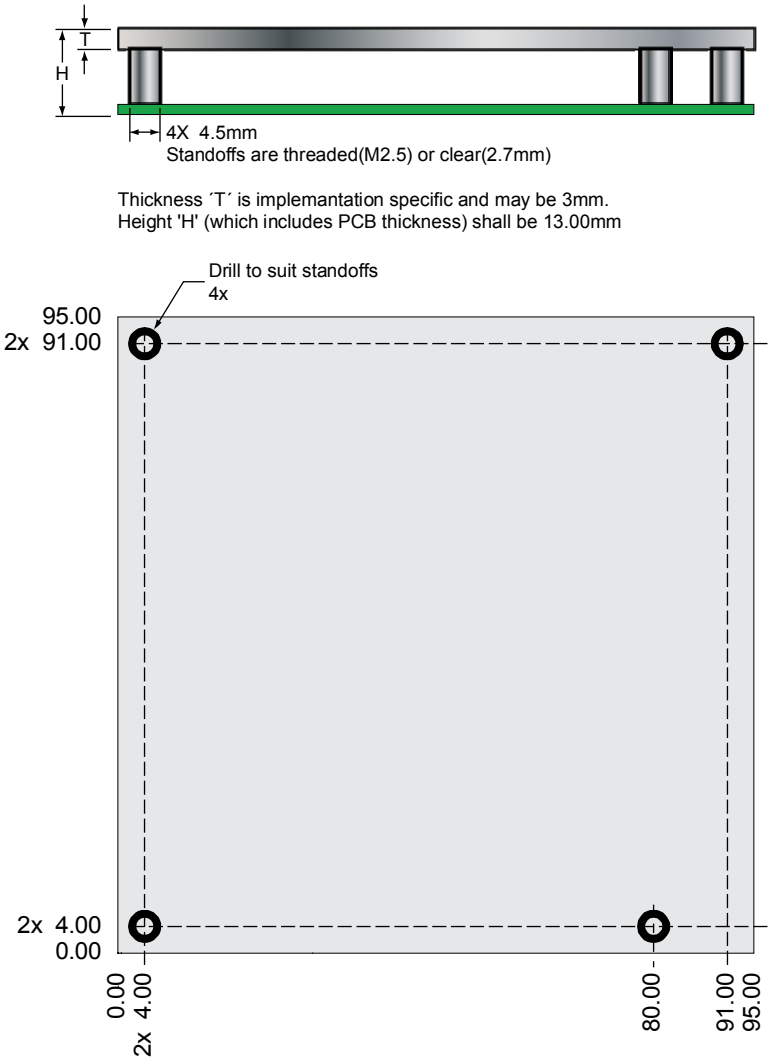


All dimensions are in mm.

X-Y tolerances ***shall*** be ± 0.3mm [±0.012"].

If a heat-spreader is supported, it ***shall*** provide the mounting hole attachment points dimensioned in Figure 6-11.

Figure 6-12: Compact Module Heat-Spreader

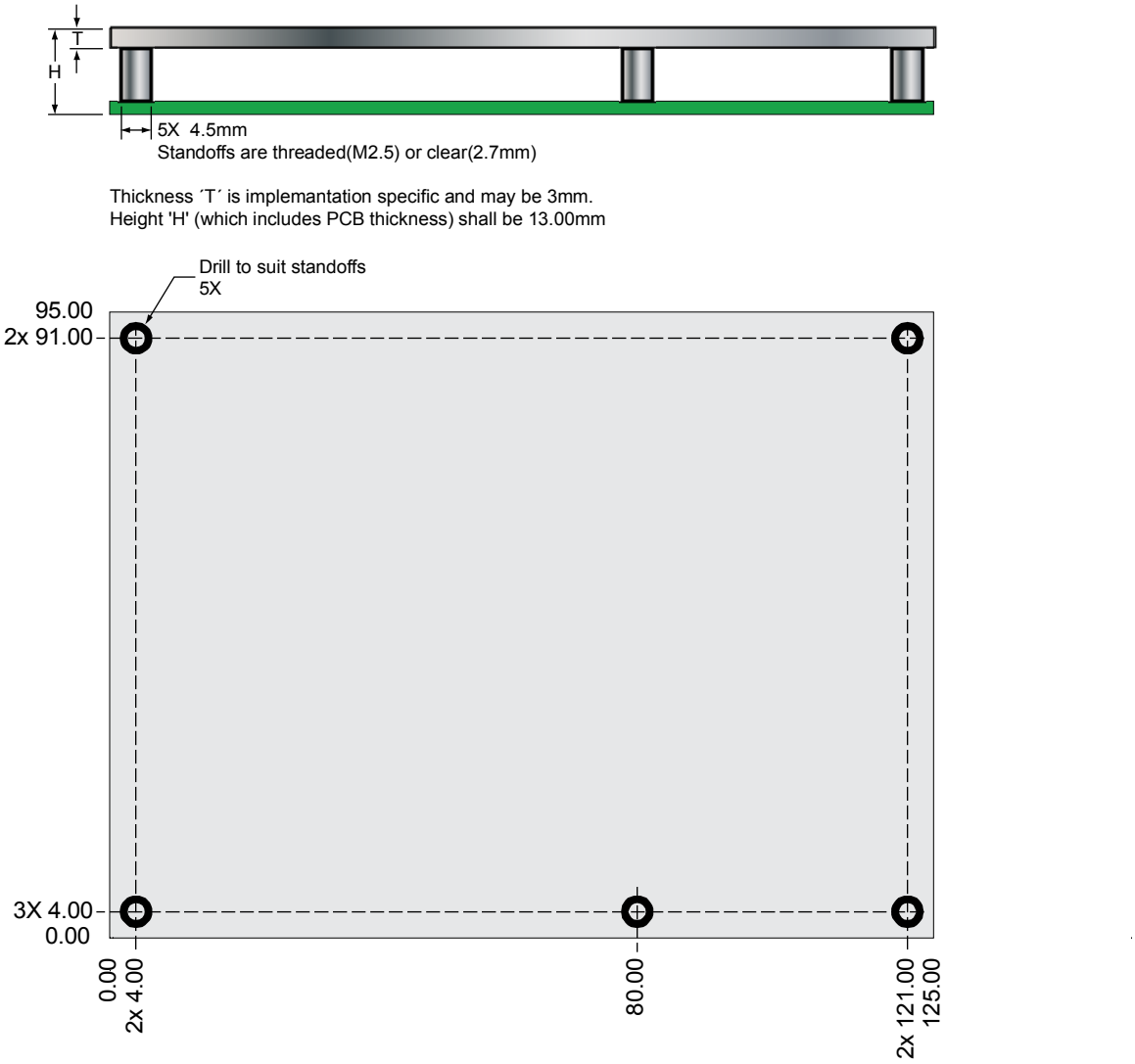


All dimensions are in mm.

X-Y tolerances ***shall*** be ± 0.3mm [±0.012"].

If a heat-spreader is supported, it ***shall*** provide the mounting hole attachment points dimensioned in Figure 6-12.

Figure 6-13: Basic Module Heat-Spreader

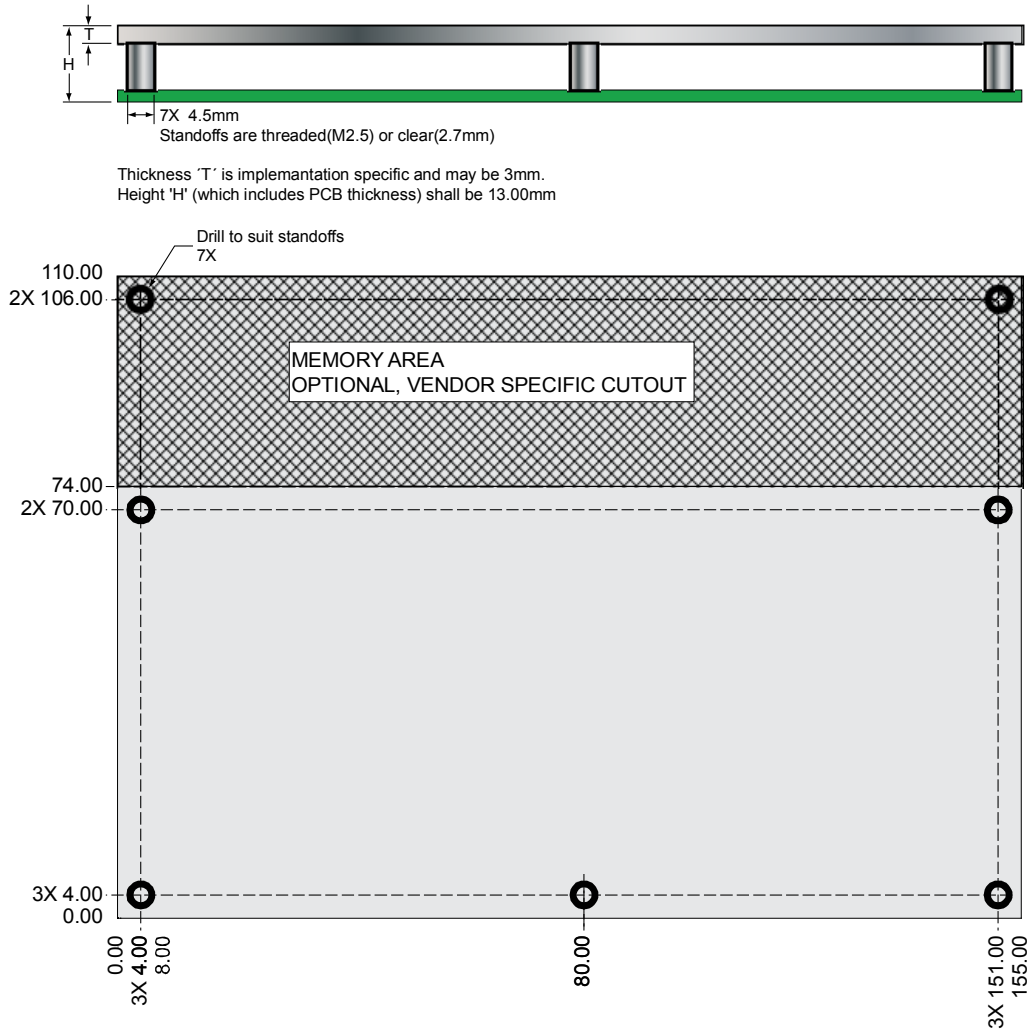


All dimensions are in mm.

X-Y tolerances ***shall*** be ± 0.3mm [±0.012"].

If a heat-spreader is supported, it ***shall*** provide the mounting hole attachment points dimensioned in Figure 6-13.

Figure 6-14: Heat-Spreader Specification for Extended Module



All dimensions are in mm.

X-Y tolerances ***shall*** be ± 0.3mm [±0.012"].

The Extended Module heat-spreader ***shall*** have minimum X-Y dimensions of 155 mm x 74 mm, as per the clear area in the figure above. The hatched area indicates the PCB area that ***may*** be used for memory Modules. The Extended Module heat-spreader ***may*** extend into the memory area. This extension is vendor specific. The maximum X-Y extent of the Extended Module heat-spreader ***shall*** be 155mm x 110mm.

If a heat-spreader is supported, it ***shall*** provide the mounting hole attachment points dimensioned in Figure 6-14.

6.11 Component Height - Module Back and Carrier Board Top

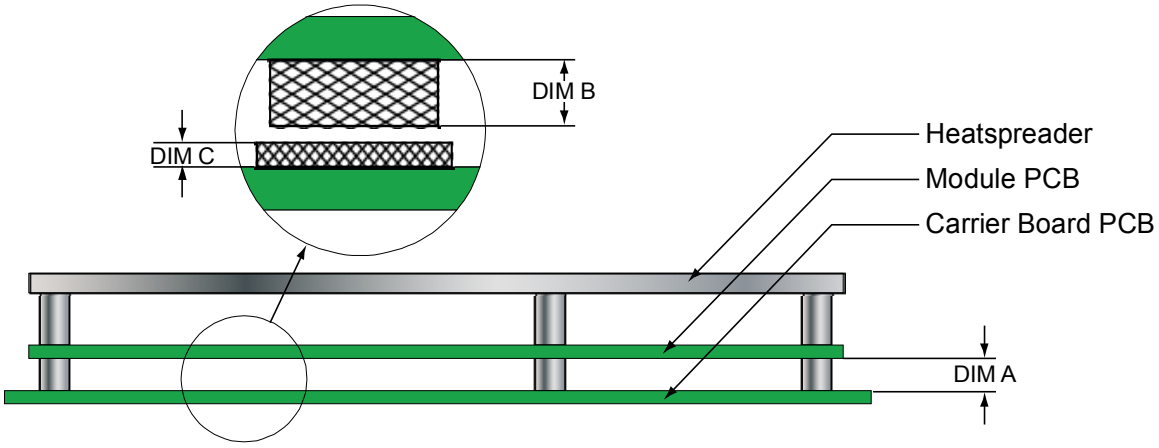
Parts mounted on the backside of the Module (in the space between the bottom surface of the Module PCB and the Carrier Board) ***shall*** have a maximum height of 3.8 mm (dimension 'B' in Figure 6-15).

It is likely that Mini size Modules will be used in space constrained applications such as hand held devices. In these applications the Module is commonly mounted directly to an enclosure without a Heatspreader. These applications would benefit from a reduced height that is possible with the lower power processors used on Mini Modules. The Mini size Modules allow for reduced component height on both the top and bottom of the Module. The Mini Module maximum top side and back side component height ***should*** be 3.0 mm.

With the 5 mm stack option, the clearance between the Carrier Board and the bottom surface of the Module's PCB is 5 mm (dimension 'A' in Figure 6-15). Using the 5 mm stack option, components placed on the Carrier Board topside under the Module envelope ***shall*** be limited to a maximum height of 1 mm (dimension 'C' in Figure 6-15), with the exception of the mating connectors. Using Carrier Board topside components up to 1mm allows a gap of 0.2 mm between Carrier Board Module bottom side components. This may not be sufficient in some situations. In Carrier Board applications in which vibration or board flex is a concern, then the Carrier Board component height ***should*** be restricted to a value less than 1mm that yields a clearance that is sufficient for the application.

If the Carrier Board uses the 8 mm stack option (dimension 'A' in Figure 6-15), then the Carrier Board topside components within the Module envelope ***shall*** be limited to a height of 4 mm (dimension 'C' in Figure 6-15), with the exception of the mating connectors. Using Carrier Board topside components up to 4mm allows a gap of 0.2 mm between Carrier Board topside components and Module bottom side components. This may not be sufficient in some situations. In Carrier Board applications in which vibration or board flex is a concern, then the Carrier Board component height ***should*** be restricted to a value less than 4 mm that yields a clearance that is sufficient for the application.

Figure 6-15: Component Clearances Underneath Module



7 Electrical Specifications

7.1 Input Power - General Considerations

The Compact, Basic and Extended Module Modules ***shall*** use a single main power rail with a nominal value of +12V.

The Mini Module ***shall*** support a wide range power supply of 4.75V to 20.0V.

In addition the Mini Module ***shall*** be optimized for 5V operation and Module vendors ***should*** report Module power figures at 5V, 12V and 18V input voltages.

Two additional rails are specified: a +5V standby power rail and a +3V battery input to power the Module Real-time Clock (RTC) circuit in the absence of other power sources. The +5V standby rail ***may*** be left unconnected on the Carrier Board if the standby functions are not required by the application. Likewise, the +3V battery input ***may*** be left open if the application does not require the RTC to keep time in the absence of the main and standby sources. There ***may*** be Module specific concerns regarding storage of system setup parameters that ***may*** be affected by the absence of the +5V standby and / or the +3V battery.

The rationale for this power-delivery scheme is:

- Module pins are scarce. It is more pin-efficient to bring power in on a higher voltage rail.
- Single supply operation is attractive to many users.
- Lithium ion battery packs for mobile systems are most prevalent with a +14.4V output. This is well suited for the +12V main power rail.
- Contemporary chipsets have no power requirements for +5V other than to provide a reference voltage for +5V tolerant inputs. No COM Express Module pins are allocated to accept +5V except for the +5V standby pins. In the case of an ATX supply, the switched (non standby) +5V line would not be used for the COM Express Module, but it might be used elsewhere on the Carrier Board.

7.2 Input Power - Current Load

The Module connector pins limit the amount of power that can be brought into the COM Express Module. The limits are different for Module Pin-out Types 1 and 10 vs. Pin-out Types 2 through 6, based on the number of 12V power pins as Pin-out Types 1 and 10 have fewer pins available.

Table 7.1: Input Power - Pin-out Type 1/10 Modules (Single Connector, 220 pins)

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max Input Ripple (mV)	Max Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max Load Power (Watts)
VCC_12V	6	12	11.4 - 12.6	11.4	+/- 100	68	85%	58
Wide input (Mini)	6		4.75 – 20.0	4.75	+/-100	28		
VCC_5V_SBY	2	5	4.75 - 5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0 - 3.3		+/- 20			

Table 7.2: Input Power - Pin-out Type 2/3/4/5/6 Modules (Dual Connector, 440 pins)

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max Input Ripple (mV)	Max Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max Load Power (Watts)
VCC_12V	12	12	11.4 - 12.6	11.4	+/- 100	137	85%	116
VCC_5V_SBY	2	5	4.75 - 5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0 - 3.3		+/- 20			

The ripple voltage, if present, must not cause the input voltage range to be exceeded.

7.3 Input Power - Sequencing

COM Express input power sequencing requirements are as follows:

VCC_RTC	***shall*** come up at the same time or before VCC_5V_SBY comes up[21]
VCC_5V_SBY	***shall*** come up at the same time or before VCC_12V comes up[18]
PWR_OK	***shall*** be active at the same time or after VCC_12V comes up[18]
PWR_OK	***shall*** be inactive at the same time or before VCC_12V goes down[18]
VCC_12V	***shall*** go down at the same time or before VCC_5V_SBY goes down
VCC_5V_SBY	***shall*** go down at the same time or before VCC_RTC goes down[18]
Wide input (Mini)	***shall*** follow the power sequencing of the VCC_12V

Figure 7-1: Power Sequencing

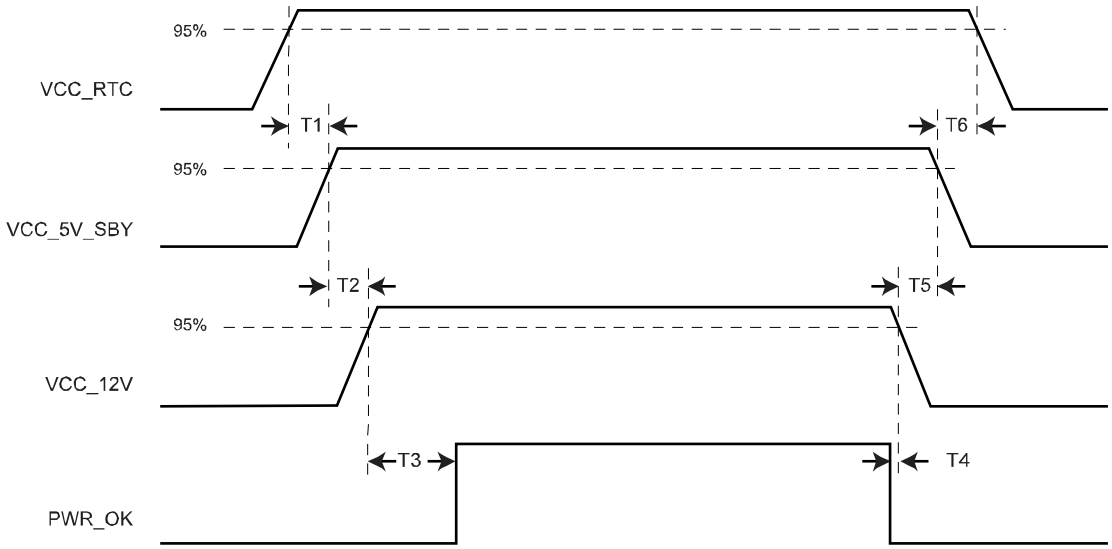


Table 7.3: Power Sequencing

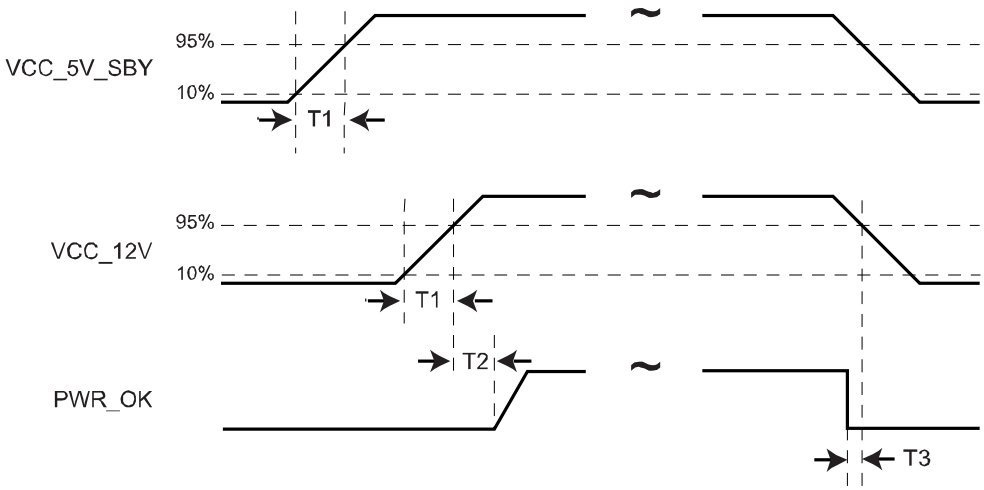
T1	VCC_RTC rise to VCC_5V_SBY rise	≥ 0 ms
T2	VCC_5V_SBY rise to VCC_12V rise	≥ 0 ms
T3	VCC_12V rise to PWROK rise	≥ 0 ms
T4	PWR_OK fall to VCC_12V fall	≥ 0 ms
T5	VCC_12V fall to VCC_5V_SBY fall	≥ 0 ms
T6	VCC_5V_SBY fall to VCC_RTC fall	≥ 0 ms

21 *If used*

7.4 Input Power - Rise Time

The input voltages to the COM Express Module VCC_12V, wide input (Mini) and VCC_5V_SBY if used ***shall*** rise from ≤10% of nominal to within the regulation ranges within 0.1 ms to 20 ms (0.1 ms ≤ T2 ≤ 20 ms). There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of its final set point within the regulation band. The smooth turn-on requires that, during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive and have a value of between 0 V/ms and [Vout, nominal / 0.1] V/ms. Also, for any 5ms segment of the 10% to 90% rise time waveform, a straight line drawn between the end points of the waveform segment must have a slope ≥ [Vout, nominal / 20] V/ms.

Figure 7-2: Input Power Rise Time



- T1,min = 0,1ms
- T1,max = 20ms
- T2 ≥ 0ms
- T3 ≥ 0ms

The values chosen were selected to be compatible and enable use of ATX specification R2.2

7.5 Signal Integrity Requirements

The signal groups listed in the following table have signal-integrity concerns that ***should*** be accounted for in Module and Carrier Board designs. A general description is shown in the table for reference only. The designer ***should*** consult the relevant interface specification documents for complete information.

Table 7.4: Signal Integrity Requirements

Signal Group	General Description	Source Spec Reference
Analog VGA	75Ω single ended ground-referenced lines. Generous isolation recommended.	
Component and Composite video	75Ω single ended ground-referenced lines. Generous isolation recommended.	
Gigabit Ethernet	Differential pairs	IEEE 802.3 Specification
LVDS	100Ω edge coupled differential pairs	National Semiconductor LVDS web site
PCI Bus	Circa 60Ω single-ended	PCI SIG - PCI Local Bus Spec. Rev. 2.3
PCI and LPC clocks	50Ω single ended ground-referenced	
PCI Express	Differential pairs	PCI SIG - PCI Express Specification
PCI Express clocks	100Ω edge couple differential pair, ground-referenced	
Serial ATA	Differential pairs	SATA Specification
USB	Differential pairs	USB 2.0 Specification

8 Environmental Specifications

8.1 Thermal Specification

8.1.1 Objectives

Thermal specification requirements set forth here serve two objectives:

1. To provide a method through which any COM Express Module's thermal performance can be specified and verified against a common reference.
2. To provide a method of thermal specification that is independent of the particular components used on the Module.

These objectives are limited to the Modules' heat-spreader interface, and primary heat sources are limited to the Module itself and ambient air.

8.1.2 Definitions

Tcase. This is the temperature of the outside surface of the Module heat-spreader plate.

Tcase_max. The maxiumum temperature allowed for the heat-spreader of the Module at point M (defined below).

Tcase_min. This is defined as the minimum temperature allowed for the heat-spreader of the Module. This temperature is directly tied to minimum allowed junction temperatures of the chips that are in contact with the heat-spreader.

M. The point on the heat-spreader where the maximum case temperature must be measured.

Tambient_max. This is defined as the maximum temperature of the air directly surrounding the Module, allowed for the operation of the Module.

Tambient_min. This is defined as the minimum temperature of the air directly surrounding the Module, allowed for the operation of the Module.

TDPmax. This is defined as the maximum power dissipation of the Module for design of a thermal solution to guarantee that the Module operates within the manufacturer's specifications. TDP stands for thermal design power.

Tcpu_junction. The junction temperature of the processor. Tcpu_junction can be measured in many processors by accessing an on-die thermal diode. Refer to the manufacturer datasheet for information on how to access the thermal diode. In some instances, software provided by the processor manufacturer or a third party may be used in conjunction with hardware on the Module / Carrier Board assembly to monitor the temperature of the processor. Verification of an internal thermal diode accuracy should be done and certified by the OEM. With verified accuracy of the diode, validation with software can then be done by end users.

Tcpu_junction_max. The maximum junction temperature for the processor as specified in the silicon manufacturer's datasheet. The Module thermal solution (i.e. heat-spreader and heatsink) shall keep the processor junction temperature at or below the Tcpu_junction_max. Note that some manufacturers do not specify maximum junction temperatures but specify maximum case temperatures instead.

Tcpu_case. The CPU package case temperature, as specified in the silicon vendor's data sheet. Note that Tcpu_case and T_case may refer to different locations in the COM Express Module system.

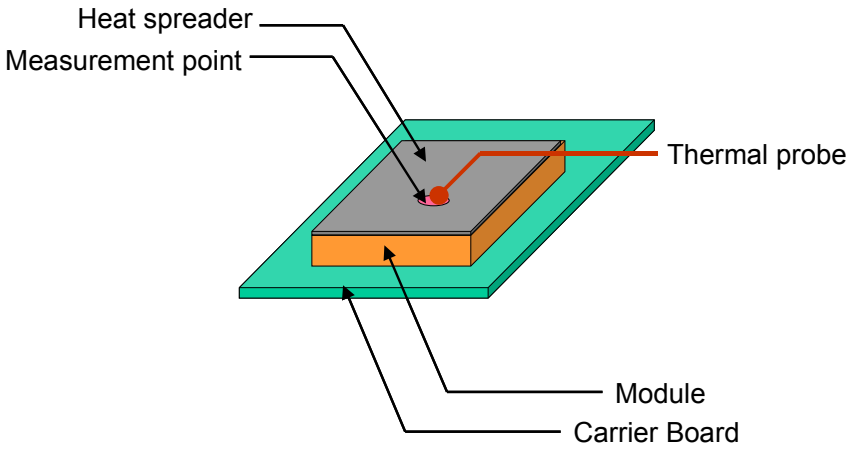
Tcpu_case_max. The maximum CPU package case temperature for the processor as specified in the silicon manufacturer's datasheet. The Module's thermal solution (i.e. heat-spreader and heatsink) shall keep the processor case temperature at or below the Tcpu_case_max. Note that some manufacturers do not specify maximum case temperatures but specify maximum junction temperatures instead.

The ultimate goal of the system thermal solution is to ensure that Tcpu_junction or Tcpu_case, whichever applies to the CPU at hand, remain below the maximum levels specified by the CPU vendor. Similar concerns apply to other high dissipation components in the Module system.

8.1.3 Tcase_max Measurement Setup

Measurements for Tcase_max ***should*** be performed according to a standardized method and under TDPmax conditions. The following figure depicts the standardized measurement setup for Tcase_max measurements.

Figure 8-1: Tcase_Max Measurement Point



Standardized setup for Tcase_max measurements.

This schematic illustration shows the Module heat-spreader, the Module, and the Carrier Board. Not shown is the user-specific cooling solution that shall attach to the heat-spreader. Modules are not normally operated without a cooling solution attached.

The measurement point (M) ***should*** be specified, either through a permanent marker on the Module's heat-spreader, or through a mechanical drawing in the product's support documentation.

8.1.4 Module Thermal Specification Requirements

A Module manufacturer ***should*** specify Tcase_max, Tcase_min, Tambient_max, Tambient_min, TDPmax and M (the Tcase_max measurement point).

A Module manufacturer ***may*** specify Tcpu_junction_max and maximum junction temperatures of other critical chips on the Module. In this case, the Module vendor ***should*** provide software to read the junction temperature of the CPU and ***may*** do the same for the other critical chips. In that case, the Module vendor ***shall*** ensure that the software is properly calibrated and that the junction temperature readings are accurate.

The efficiency of the Module thermal characteristics has an impact on the Module's MTBF (Mean Time Between Failure). Higher junction temperatures result in a shorter silicon life. Module vendors ***should*** provide MTBF information.

8.1.5 Shock and Vibration

The shock and vibration characteristics of a system built with a COM Express Module will vary depending on system-implementation details. These details include size, rigidity, and mounting configuration of the Carrier Board and the thermal solution. There is no explicit shock and vibration specification that COM Express Modules are required to meet.

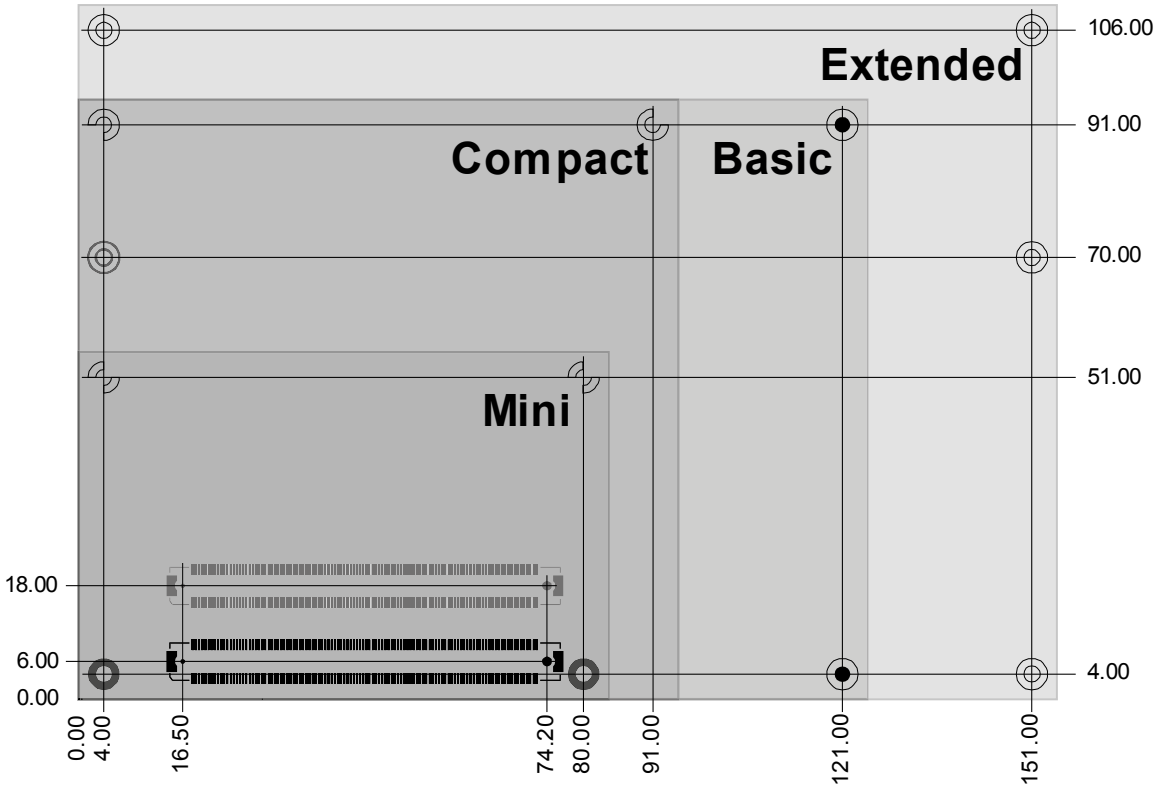
If all available COM Express Module and heat-spreader attachment points are used, then a COM Express based system should be capable of excellent shock and vibration performance.

9 Appendix

9.1 Mounting positions and connector location for Carrier Boards

Figure 9-1: Carrier Board mounting positions

Common for all Form Factors
Extended only
Basic only
Compact only
Compact and Basic only
Mini only



All dimensions are shown in millimeters.

9.2 Comparison of single connector Types 1 and 10

Bold text indicates a difference to the previous listed type.

Table 9.1: Comparison of Type 1 and Type 10 Pin-Out vs. 84X55 (Mini)

	Type 1 Rev. 1.0		Type 1 Rev. 2.0		Type 10 Rev. 2.0		Type 10 Rev. 2.1	
Pin	Row A	Row B	Row A	Row B	Row A	Row B	Row A	Row B
1	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
2	GBE0_MDI3-	GBE0_ACT#	GBE0_MDI3-	GBE0_ACT#	GBE0_MDI3-	GBE0_ACT#	GBE0_MDI3-	**GBE0_ACT#**
3	GBE0_MDI3+	LPC_FRAME#	GBE0_MDI3+	LPC_FRAME#	GBE0_MDI3+	LPC_FRAME#	GBE0_MDI3+	LPC_FRAME#
4	GBE0_LINK100#	LPC_AD0	GBE0_LINK100#	LPC_AD0	GBE0_LINK100#	LPC_AD0	GBE0_LINK100#	LPC_AD0
5	GBE0_LINK1000#	LPC_AD1	GBE0_LINK1000#	LPC_AD1	GBE0_LINK1000#	LPC_AD1	GBE0_LINK1000#	LPC_AD1
6	GBE0_MDI2-	LPC_AD2	GBE0_MDI2-	LPC_AD2	GBE0_MDI2-	LPC_AD2	GBE0_MDI2-	LPC_AD2
7	GBE0_MDI2+	LPC_AD3	GBE0_MDI2+	LPC_AD3	GBE0_MDI2+	LPC_AD3	GBE0_MDI2+	LPC_AD3
8	GBE0_LINK#	LPC_DRQ0#	GBE0_LINK#	LPC_DRQ0#	GBE0_LINK#	LPC_DRQ0#	GBE0_LINK#	LPC_DRQ0#
9	GBE0_MDI1-	LPC_DRQ1#	GBE0_MDI1-	LPC_DRQ1#	GBE0_MDI1-	LPC_DRQ1#	GBE0_MDI1-	LPC_DRQ1#
10	GBE0_MDI1+	LPC_CLK	GBE0_MDI1+	LPC_CLK	GBE0_MDI1+	LPC_CLK	GBE0_MDI1+	LPC_CLK
11	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
12	GBE0_MDI0-	PWRBTN#	GBE0_MDI0-	PWRBTN#	GBE0_MDI0-	PWRBTN#	GBE0_MDI0-	PWRBTN#
13	GBE0_MDI0+	SMB_CK	GBE0_MDI0+	SMB_CK	GBE0_MDI0+	SMB_CK	GBE0_MDI0+	SMB_CK
14	GBE0_CTREF	SMB_DAT	GBE0_CTREF	SMB_DAT	GBE0_CTREF	SMB_DAT	GBE0_CTREF	SMB_DAT
15	SUS_S3#	SMB_ALERT#	SUS_S3#	SMB_ALERT#	SUS_S3#	SMB_ALERT#	SUS_S3#	SMB_ALERT#
16	SATA0_TX+	SATA1_TX+	SATA0_TX+	SATA1_TX+	SATA0_TX+	SATA1_TX+	SATA0_TX+	SATA1_TX+
17	SATA0_TX-	SATA1_TX-	SATA0_TX-	SATA1_TX-	SATA0_TX-	SATA1_TX-	SATA0_TX-	SATA1_TX-
18	SUS_S4#	SUS_STAT#	SUS_S4#	SUS_STAT#	SUS_S4#	SUS_STAT#	SUS_S4#	SUS_STAT#
19	SATA0_RX+	SATA1_RX+	SATA0_RX+	SATA1_RX+	SATA0_RX+	SATA1_RX+	SATA0_RX+	SATA1_RX+
20	SATA0_RX-	SATA1_RX-	SATA0_RX-	SATA1_RX-	SATA0_RX-	SATA1_RX-	SATA0_RX-	SATA1_RX-
21	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
22	SATA2_TX+	SATA3_TX+	SATA2_TX+	SATA3_TX+	**RSVD**	**RSVD**	**USB_SSRX0-**	**USB_SSTX0-**
23	SATA2_TX-	SATA3_TX-	SATA2_TX-	SATA3_TX-	**RSVD**	**RSVD**	**USB_SSRX0+**	**USB_SSTX0+**
24	SUS_S5#	PWR_OK	SUS_S5#	PWR_OK	SUS_S5#	PWR_OK	SUS_S5#	PWR_OK
25	SATA2_RX+	SATA3_RX+	SATA2_RX+	SATA3_RX+	**RSVD**	**RSVD**	**USB_SSRX1-**	**USB-SSTX1-**
26	SATA2_RX-	SATA3_RX-	SATA2_RX-	SATA3_RX-	**RSVD**	**RSVD**	**USB_SSRX1+**	**USB-SSTX1+**
27	BATLOW#	WDT	BATLOW#	WDT	BATLOW#	WDT	BATLOW#	WDT

	Type 1 Rev. 1.0		Type 1 Rev. 2.0		Type 10 Rev. 2.0		Type 10 Rev. 2.1	
Pin	**Row A**	**Row B**	**Row A**	**Row B**	**Row A**	**Row B**	**Row A**	**Row B**
28	ATA_ACT#	AC_SDIN2	**(S)ATA_ACT#**	**AC/HDA_SDIN2**	(S)ATA_ACT#	AC/HDA_SDIN2	(S)ATA_ACT#	AC/HDA_SDIN2
29	AC_SYNC	AC_SDIN1	**AC/HDA_SYNC**	**AC/HDA_SDIN1**	AC/HDA_SYNC	AC/HDA_SDIN1	AC/HDA_SYNC	AC/HDA_SDIN1
30	AC_RST#	AC_SDIN0	**AC/HDA_RST#**	**AC/HDA_SDIN0**	AC/HDA_RST#	AC/HDA_SDIN0	AC/HDA_RST#	AC/HDA_SDIN0
31	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
32	AC_BITCLK	SPKR	**AC/HDA_BITCLK**	SPKR	AC/HDA_BITCLK	SPKR	AC/HDA_BITCLK	SPKR
33	AC_SDOUT	I2C_CK	**AC/HDA_SDOUT**	I2C_CK	AC/HDA_SDOUT	I2C_CK	AC/HDA_SDOUT	I2C_CK
34	BIOS_DISABLE#	I2C_DAT	**BIOS_DIS0#**	I2C_DAT	BIOS_DIS0#	I2C_DAT	BIOS_DIS0#	I2C_DAT
35	THRMTRIP#	THRM#	THRMTRIP#	THRM#	THRMTRIP#	THRM#	THRMTRIP#	THRM#
36	USB6-	USB7-	USB6-	USB7-	USB6-	USB7-	USB6-	USB7-
37	USB6+	USB7+	USB6+	USB7+	USB6+	USB7+	USB6+	USB7+
38	USB_6_7_OC#	USB_4_5_OC#	USB_6_7_OC#	USB_4_5_OC#	USB_6_7_OC#	USB_4_5_OC#	USB_6_7_OC#	USB_4_5_OC#
39	USB4-	USB5-	USB4-	USB5-	USB4-	USB5-	USB4-	USB5-
40	USB4+	USB5+	USB4+	USB5+	USB4+	USB5+	USB4+	USB5+
41	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
42	USB2-	USB3-	USB2-	USB3-	USB2-	USB3-	USB2-	USB3-
43	USB2+	USB3+	USB2+	USB3+	USB2+	USB3+	USB2+	USB3+
44	USB_2_3_OC#	USB_0_1_OC#	USB_2_3_OC#	USB_0_1_OC#	USB_2_3_OC#	USB_0_1_OC#	USB_2_3_OC#	USB_0_1_OC#
45	USB0-	USB1-	USB0-	USB1-	USB0-	USB1-	USB0-	USB1-
46	USB0+	USB1+	USB0+	USB1+	USB0+	USB1+	USB0+	USB1+
47	VCC_RTC	EXCD1_PERST#	VCC_RTC	EXCD1_PERST#	VCC_RTC	EXCD1_PERST#	VCC_RTC	EXCD1_PERST#
48	EXCD0_PERST#	EXCD1_CPPE#	EXCD0_PERST#	EXCD1_CPPE#	EXCD0_PERST#	EXCD1_CPPE#	EXCD0_PERST#	EXCD1_CPPE#
49	EXCD0_CPPE#	SYS_RESET#	EXCD0_CPPE#	SYS_RESET#	EXCD0_CPPE#	SYS_RESET#	EXCD0_CPPE#	SYS_RESET#
50	LPC_SERIRQ	CB_RESET#	LPC_SERIRQ	CB_RESET#	LPC_SERIRQ	CB_RESET#	LPC_SERIRQ	CB_RESET#
51	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
52	PCIE_TX5+	PCIE_RX5+	PCIE_TX5+	PCIE_RX5+	**RSVD**	**RSVD**	RSVD	RSVD
53	PCIE_TX5-	PCIE_RX5-	PCIE_TX5-	PCIE_RX5-	**RSVD**	**RSVD**	RSVD	RSVD
54	GPI0	GPO1	GPI0	GPO1	GPI0	GPO1	GPI0	GPO1
55	PCIE_TX4+	PCIE_RX4+	PCIE_TX4+	PCIE_RX4+	**RSVD**	**RSVD**	RSVD	RSVD
56	PCIE_TX4-	PCIE_RX4-	PCIE_TX4-	PCIE_RX4-	**RSVD**	**RSVD**	RSVD	RSVD
57	GND	GPO2	GND	GPO2	GND	GPO2	GND	GPO2
58	PCIE_TX3+	PCIE_RX3+	PCIE_TX3+	PCIE_RX3+	PCIE_TX3+	PCIE_RX3+	PCIE_TX3+	PCIE_RX3+
59	PCIE_TX3-	PCIE_RX3-	PCIE_TX3-	PCIE_RX3-	PCIE_TX3-	PCIE_RX3-	PCIE_TX3-	PCIE_RX3-
60	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)

	Type 1 Rev. 1.0		Type 1 Rev. 2.0		Type 10 Rev. 2.0		Type 10 Rev. 2.1	
Pin	**Row A**	**Row B**	**Row A**	**Row B**	**Row A**	**Row B**	**Row A**	**Row B**
61	PCIE_TX2+	PCIE_RX2+	PCIE_TX2+	PCIE_RX2+	PCIE_TX2+	PCIE_RX2+	PCIE_TX2+	PCIE_RX2+
62	PCIE_TX2-	PCIE_RX2-	PCIE_TX2-	PCIE_RX2-	PCIE_TX2-	PCIE_RX2-	PCIE_TX2-	PCIE_RX2-
63	GPI1	GPO3	GPI1	GPO3	GPI1	GPO3	GPI1	GPO3
64	PCIE_TX1+	PCIE_RX1+	PCIE_TX1+	PCIE_RX1+	PCIE_TX1+	PCIE_RX1+	PCIE_TX1+	PCIE_RX1+
65	PCIE_TX1-	PCIE_RX1-	PCIE_TX1-	PCIE_RX1-	PCIE_TX1-	PCIE_RX1-	PCIE_TX1-	PCIE_RX1-
66	GND	WAKE0#	GND	WAKE0#	GND	WAKE0#	GND	WAKE0#
67	GPI2	WAKE1#	GPI2	WAKE1#	GPI2	WAKE1#	GPI2	WAKE1#
68	PCIE_TX0+	PCIE_RX0+	PCIE_TX0+	PCIE_RX0+	PCIE_TX0+	PCIE_RX0+	PCIE_TX0+	PCIE_RX0+
69	PCIE_TX0-	PCIE_RX0-	PCIE_TX0-	PCIE_RX0-	PCIE_TX0-	PCIE_RX0-	PCIE_TX0-	PCIE_RX0-
70	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
71	LVDS_A0+	LVDS_B0+	LVDS_A0+	LVDS_B0+	LVDS_A0+	**DDI0_PAIR0+**	**LVDS_A0+**	DDI0_PAIR0+
72	LVDS_A0-	LVDS_B0-	LVDS_A0-	LVDS_B0-	LVDS_A0-	**DDI0_PAIR0-**	**LVDS_A0-**	DDI0_PAIR0-
73	LVDS_A1+	LVDS_B1+	LVDS_A1+	LVDS_B1+	LVDS_A1+	**DDI0_PAIR1+**	**LVDS_A1+**	DDI0_PAIR1+
74	LVDS_A1-	LVDS_B1-	LVDS_A1-	LVDS_B1-	LVDS_A1-	**DDI0_PAIR1-**	**LVDS_A1-**	DDI0_PAIR1-
75	LVDS_A2+	LVDS_B2+	LVDS_A2+	LVDS_B2+	LVDS_A2+	**DDI0_PAIR2+**	**LVDS_A2+**	DDI0_PAIR2+
76	LVDS_A2-	LVDS_B2-	LVDS_A2-	LVDS_B2-	LVDS_A2-	**DDI0_PAIR2-**	**LVDS_A2-**	DDI0_PAIR2-
77	LVDS_VDD_EN	LVDS_B3+	LVDS_VDD_EN	LVDS_B3+	LVDS_VDD_EN	**DDI0_PAIR4+**	**LVDS_VDD_EN**	DDI0_PAIR4+
78	LVDS_A3+	LVDS_B3-	LVDS_A3+	LVDS_B3-	LVDS_A3+	**DDI0_PAIR4-**	**LVDS_A3+**	DDI0_PAIR4-
79	LVDS_A3-	LVDS_BKLT_EN	LVDS_A3-	LVDS_BKLT_EN	LVDS_A3-	LVDS_BKLT_EN	**LVDS_A3-**	**LVDS_BKLT_EN**
80	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
81	LVDS_A_CK+	LVDS_B_CK+	LVDS_A_CK+	LVDS_B_CK+	LVDS_A_CK+	**DDI0_PAIR3+**	LVDS_A_CK+	DDI0_PAIR3+
82	LVDS_A_CK-	LVDS_B_CK-	LVDS_A_CK-	LVDS_B_CK-	LVDS_A_CK-	**DDI0_PAIR3-**	LVDS_A_CK-	DDI0_PAIR3-
83	LVDS_I2C_CK	LVDS_BKLT_CTRL	LVDS_I2C_CK	LVDS_BKLT_CTRL	LVDS_I2C_CK	LVDS_BKLT_CTRL	**LVDS_I2C_CK**	**LVDS_BKLT_CTRL**
84	LVDS_I2C_DAT	VCC_5V_SBY	LVDS_I2C_DAT	VCC_5V_SBY	LVDS_I2C_DAT	VCC_5V_SBY	**LVDS_I2C_DAT**	VCC_5V_SBY
85	GPI3	VCC_5V_SBY	GPI3	VCC_5V_SBY	GPI3	VCC_5V_SBY	GPI3	VCC_5V_SBY
86	KBD_RST#	VCC_5V_SBY	KBD_RST#	VCC_5V_SBY	**RSVD**	VCC_5V_SBY	RSVD	VCC_5V_SBY
87	KBD_A20GATE	VCC_5V_SBY	KBD_A20GATE	VCC_5V_SBY	**RSVD**	VCC_5V_SBY	eDP_HPD	VCC_5V_SBY
88	PCIE_CLK_REF+	RSVD	PCIE_CLK_REF+	**BIOS_DIS1#**	PCIE_CLK_REF+	BIOS_DIS1#	PCIE_CLK_REF+	BIOS_DIS1#
89	PCIE_CLK_REF-	VGA_RED	PCIE_CLK_REF-	VGA_RED	PCIE_CLK_REF-	**DD0_HPD**	PCIE_CLK_REF-	DD0_HPD
90	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
91	RSVD	VGA_GRN	**SPI_POWER**	VGA_GRN	SPI_POWER	**DDI0_PAIR5+**	SPI_POWER	DDI0_PAIR5+
92	RSVD	VGA_BLU	**SPI_MISO**	VGA_BLU	SPI_MISO	**DDI0_PAIR5-**	SPI_MISO	DDI0_PAIR5-
93	GPO0	VGA_HSYNC	GPO0	VGA_HSYNC	GPO0	**DDI0_PAIR6+**	GPO0	DDI0_PAIR6+

	Type 1 Rev. 1.0		Type 1 Rev. 2.0		Type 10 Rev. 2.0		Type 10 Rev. 2.1	
Pin	**Row A**	**Row B**	**Row A**	**Row B**	**Row A**	**Row B**	**Row A**	**Row B**
94	RSVD	VGA_VSYNC	**SPI_CLK**	VGA_VSYNC	SPI_CLK	**DDI0_PAIR6-**	SPI_CLK	DDI0_PAIR6-
95	RSVD	VGA_I2C_CK	**SPI_MOSI**	VGA_I2C_CK	SPI_MOSI	**DDI0_DDC_AUX_SEL**	SPI_MOSI	DDI0_DDC_AUX_SEL
96	GND	VGA_I2C_DAT	GND	VGA_I2C_DAT	**TPM_PP**	**RSVD**	TPM_PP	**USB_HOST_PRSNT**
97	VCC_12V	TV_DAC_A	TYPE10#	**SPI_CS#**	**TYPE10#**	SPI_CS#	TYPE10#	SPI_CS#
98	VCC_12V	TV_DAC_B	**RSVD**	**RSVD**	**SER0_TX**	**DDI0_CTRLCLK_AUX+**	SER0_TX	DDI0_CTRLCLK_AUX+
99	VCC_12V	TV_DAC_C	**RSVD**	**RSVD**	**SER0_RX**	**DDI0_CTRLDATA_AUX-**	SER0_RX	DDI0_CTRLDATA_AUX-
100	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
101	VCC_12V	VCC_12V	**RSVD**	**RSVD**	**SER1_TX**	**FAN_PWMOUT**	SER1_TX	FAN_PWMOUT
102	VCC_12V	VCC_12V	**RSVD**	**RSVD**	**SER1_RX**	**FAN_TACHIN**	SER1_RX	FAN_TACHIN
103	VCC_12V	VCC_12V	**RSVD**	**RSVD**	**LID#**	**SLEEP#**	LID#	SLEEP#
104	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
109	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
110	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)

9.3 Comparison of Types 2 and 6

Bold text indicates a difference to Type 2 Rev. 1.0

Table 9.2: Comparison of Type 2 and Type 6 Pin-Out

	TYPE 2 Rev. 1.0		TYPE 2 Rev. 2.0		TYPE 6 Rev. 2.0		TYPE 6 Rev. 2.1	
Pin	Row A	Row B	Row A	Row B	Row A	Row B	Row A	Row B
1	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
2	GBE0_MDI3-	GBE0_ACT#	GBE0_MDI3-	GBE0_ACT#	GBE0_MDI3-	GBE0_ACT#	GBE0_MDI3-	GBE0_ACT#
3	GBE0_MDI3+	LPC_FRAME#	GBE0_MDI3+	LPC_FRAME#	GBE0_MDI3+	LPC_FRAME#	GBE0_MDI3+	LPC_FRAME#
4	GBE0_LINK100#	LPC_AD0	GBE0_LINK100#	LPC_AD0	GBE0_LINK100#	LPC_AD0	GBE0_LINK100#	LPC_AD0
5	GBE0_LINK1000#	LPC_AD1	GBE0_LINK1000#	LPC_AD1	GBE0_LINK1000#	LPC_AD1	GBE0_LINK1000#	LPC_AD1
6	GBE0_MDI2-	LPC_AD2	GBE0_MDI2-	LPC_AD2	GBE0_MDI2-	LPC_AD2	GBE0_MDI2-	LPC_AD2
7	GBE0_MDI2+	LPC_AD3	GBE0_MDI2+	LPC_AD3	GBE0_MDI2+	LPC_AD3	GBE0_MDI2+	LPC_AD3
8	GBE0_LINK#	LPC_DRQ0#	GBE0_LINK#	LPC_DRQ0#	GBE0_LINK#	LPC_DRQ0#	GBE0_LINK#	LPC_DRQ0#
9	GBE0_MDI1-	LPC_DRQ1#	GBE0_MDI1-	LPC_DRQ1#	GBE0_MDI1-	LPC_DRQ1#	GBE0_MDI1-	LPC_DRQ1#
10	GBE0_MDI1+	LPC_CLK	GBE0_MDI1+	LPC_CLK	GBE0_MDI1+	LPC_CLK	GBE0_MDI1+	LPC_CLK
11	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
12	GBE0_MDI0-	PWRBTN#	GBE0_MDI0-	PWRBTN#	GBE0_MDI0-	PWRBTN#	GBE0_MDI0-	PWRBTN#
13	GBE0_MDI0+	SMB_CK	GBE0_MDI0+	SMB_CK	GBE0_MDI0+	SMB_CK	GBE0_MDI0+	SMB_CK
14	GBE0_CTREF	SMB_DAT	GBE0_CTREF	SMB_DAT	GBE0_CTREF	SMB_DAT	GBE0_CTREF	SMB_DAT
15	SUS_S3#	SMB_ALERT#	SUS_S3#	SMB_ALERT#	SUS_S3#	SMB_ALERT#	SUS_S3#	SMB_ALERT#
16	SATA0_TX+	SATA1_TX+	SATA0_TX+	SATA1_TX+	SATA0_TX+	SATA1_TX+	SATA0_TX+	SATA1_TX+
17	SATA0_TX-	SATA1_TX-	SATA0_TX-	SATA1_TX-	SATA0_TX-	SATA1_TX-	SATA0_TX-	SATA1_TX-
18	SUS_S4#	SUS_STAT#	SUS_S4#	SUS_STAT#	SUS_S4#	SUS_STAT#	SUS_S4#	SUS_STAT#
19	SATA0_RX+	SATA1_RX+	SATA0_RX+	SATA1_RX+	SATA0_RX+	SATA1_RX+	SATA0_RX+	SATA1_RX+
20	SATA0_RX-	SATA1_RX-	SATA0_RX-	SATA1_RX-	SATA0_RX-	SATA1_RX-	SATA0_RX-	SATA1_RX-
21	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
22	SATA2_TX+	SATA3_TX+	SATA2_TX+	SATA3_TX+	SATA2_TX+	SATA3_TX+	SATA2_TX+	SATA3_TX+
23	SATA2_TX-	SATA3_TX-	SATA2_TX-	SATA3_TX-	SATA2_TX-	SATA3_TX-	SATA2_TX-	SATA3_TX-
24	SUS_S5#	PWR_OK	SUS_S5#	PWR_OK	SUS_S5#	PWR_OK	SUS_S5#	PWR_OK

	TYPE 2 Rev. 1.0		TYPE 2 Rev. 2.0		TYPE 6 Rev. 2.0		TYPE 6 Rev. 2.1	
Pin	Row A	Row B	Row A	Row B	Row A	Row B	Row A	Row B
25	SATA2_RX+	SATA3_RX+	SATA2_RX+	SATA3_RX+	SATA2_RX+	SATA3_RX+	SATA2_RX+	SATA3_RX+
26	SATA2_RX-	SATA3_RX-	SATA2_RX-	SATA3_RX-	SATA2_RX-	SATA3_RX-	SATA2_RX-	SATA3_RX-
27	BATLOW#	WDT	BATLOW#	WDT	BATLOW#	WDT	BATLOW#	WDT
28	ATA_ACT#	AC_SDIN2	**(S)ATA_ACT#**	**AC/HDA_SDIN2**	**(S)ATA_ACT#**	**AC/HDA_SDIN2**	**(S)ATA_ACT#**	**AC/HDA_SDIN2**
29	AC_SYNC	AC_SDIN1	**AC/HDA_SYNC**	**AC/HDA_SDIN1**	**AC/HDA_SYNC**	**AC/HDA_SDIN1**	**AC/HDA_SYNC**	**AC/HDA_SDIN1**
30	AC_RST#	AC_SDIN0	**AC/HDA_RST#**	**AC/HDA_SDIN0**	**AC/HDA_RST#**	**AC/HDA_SDIN0**	**AC/HDA_RST#**	**AC/HDA_SDIN0**
31	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
32	AC_BITCLK	SPKR	**AC/HDA_BITCLK**	SPKR	**AC/HDA_BITCLK**	SPKR	**AC/HDA_BITCLK**	SPKR
33	AC_SDOUT	I2C_CK	**AC/HDA_SDOUT**	I2C_CK	**AC/HDA_SDOUT**	I2C_CK	**AC/HDA_SDOUT**	I2C_CK
34	BIOS_DISABLE#	I2C_DAT	**BIOS_DIS0#**	I2C_DAT	**BIOS_DIS0#**	I2C_DAT	**BIOS_DIS0#**	I2C_DAT
35	THRMTRIP#	THRM#	THRMTRIP#	THRM#	THRMTRIP#	THRM#	THRMTRIP#	THRM#
36	USB6-	USB7-	USB6-	USB7-	USB6-	USB7-	USB6-	USB7-
37	USB6+	USB7+	USB6+	USB7+	USB6+	USB7+	USB6+	USB7+
38	USB_6_7_OC#	USB_4_5_OC#	USB_6_7_OC#	USB_4_5_OC#	USB_6_7_OC#	USB_4_5_OC#	USB_6_7_OC#	USB_4_5_OC#
39	USB4-	USB5-	USB4-	USB5-	USB4-	USB5-	USB4-	USB5-
40	USB4+	USB5+	USB4+	USB5+	USB4+	USB5+	USB4+	USB5+
41	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
42	USB2-	USB3-	USB2-	USB3-	USB2-	USB3-	USB2-	USB3-
43	USB2+	USB3+	USB2+	USB3+	USB2+	USB3+	USB2+	USB3+
44	USB_2_3_OC#	USB_0_1_OC#	USB_2_3_OC#	USB_0_1_OC#	USB_2_3_OC#	USB_0_1_OC#	USB_2_3_OC#	USB_0_1_OC#
45	USB0-	USB1-	USB0-	USB1-	USB0-	USB1-	USB0-	USB1-
46	USB0+	USB1+	USB0+	USB1+	USB0+	USB1+	USB0+	USB1+
47	VCC_RTC	EXCD1_PERST#	VCC_RTC	EXCD1_PERST#	VCC_RTC	EXCD1_PERST#	VCC_RTC	EXCD1_PERST#
48	EXCD0_PERST#	EXCD1_CPPE#	EXCD0_PERST#	EXCD1_CPPE#	EXCD0_PERST#	EXCD1_CPPE#	EXCD0_PERST#	EXCD1_CPPE#
49	EXCD0_CPPE#	SYS_RESET#	EXCD0_CPPE#	SYS_RESET#	EXCD0_CPPE#	SYS_RESET#	EXCD0_CPPE#	SYS_RESET#
50	LPC_SERIRQ	CB_RESET#	LPC_SERIRQ	CB_RESET#	LPC_SERIRQ	CB_RESET#	LPC_SERIRQ	CB_RESET#
51	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
52	PCIE_TX5+	PCIE_RX5+	PCIE_TX5+	PCIE_RX5+	PCIE_TX5+	PCIE_RX5+	PCIE_TX5+	PCIE_RX5+
53	PCIE_TX5-	PCIE_RX5-	PCIE_TX5-	PCIE_RX5-	PCIE_TX5-	PCIE_RX5-	PCIE_TX5-	PCIE_RX5-

	TYPE 2 Rev. 1.0		TYPE 2 Rev. 2.0		TYPE 6 Rev. 2.0		TYPE 6 Rev. 2.1	
Pin	Row A	Row B	Row A	Row B	Row A	Row B	Row A	Row B
54	GPI0	GPO1	GPI0	GPO1	GPI0	GPO1	GPI0	GPO1
55	PCIE_TX4+	PCIE_RX4+	PCIE_TX4+	PCIE_RX4+	PCIE_TX4+	PCIE_RX4+	PCIE_TX4+	PCIE_RX4+
56	PCIE_TX4-	PCIE_RX4-	PCIE_TX4-	PCIE_RX4-	PCIE_TX4-	PCIE_RX4-	PCIE_TX4-	PCIE_RX4-
57	GND	GPO2	GND	GPO2	GND	GPO2	GND	GPO2
58	PCIE_TX3+	PCIE_RX3+	PCIE_TX3+	PCIE_RX3+	PCIE_TX3+	PCIE_RX3+	PCIE_TX3+	PCIE_RX3+
59	PCIE_TX3-	PCIE_RX3-	PCIE_TX3-	PCIE_RX3-	PCIE_TX3-	PCIE_RX3-	PCIE_TX3-	PCIE_RX3-
60	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
61	PCIE_TX2+	PCIE_RX2+	PCIE_TX2+	PCIE_RX2+	PCIE_TX2+	PCIE_RX2+	PCIE_TX2+	PCIE_RX2+
62	PCIE_TX2-	PCIE_RX2-	PCIE_TX2-	PCIE_RX2-	PCIE_TX2-	PCIE_RX2-	PCIE_TX2-	PCIE_RX2-
63	GPI1	GPO3	GPI1	GPO3	GPI1	GPO3	GPI1	GPO3
64	PCIE_TX1+	PCIE_RX1+	PCIE_TX1+	PCIE_RX1+	PCIE_TX1+	PCIE_RX1+	PCIE_TX1+	PCIE_RX1+
65	PCIE_TX1-	PCIE_RX1-	PCIE_TX1-	PCIE_RX1-	PCIE_TX1-	PCIE_RX1-	PCIE_TX1-	PCIE_RX1-
66	GND	WAKE0#	GND	WAKE0#	GND	WAKE0#	GND	WAKE0#
67	GPI2	WAKE1#	GPI2	WAKE1#	GPI2	WAKE1#	GPI2	WAKE1#
68	PCIE_TX0+	PCIE_RX0+	PCIE_TX0+	PCIE_RX0+	PCIE_TX0+	PCIE_RX0+	PCIE_TX0+	PCIE_RX0+
69	PCIE_TX0-	PCIE_RX0-	PCIE_TX0-	PCIE_RX0-	PCIE_TX0-	PCIE_RX0-	PCIE_TX0-	PCIE_RX0-
70	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
71	LVDS_A0+	LVDS_B0+	LVDS_A0+	LVDS_B0+	LVDS_A0+	LVDS_B0+	LVDS_A0+	LVDS_B0+
72	LVDS_A0-	LVDS_B0-	LVDS_A0-	LVDS_B0-	LVDS_A0-	LVDS_B0-	LVDS_A0-	LVDS_B0-
73	LVDS_A1+	LVDS_B1+	LVDS_A1+	LVDS_B1+	LVDS_A1+	LVDS_B1+	LVDS_A1+	LVDS_B1+
74	LVDS_A1-	LVDS_B1-	LVDS_A1-	LVDS_B1-	LVDS_A1-	LVDS_B1-	LVDS_A1-	LVDS_B1-
75	LVDS_A2+	LVDS_B2+	LVDS_A2+	LVDS_B2+	LVDS_A2+	LVDS_B2+	LVDS_A2+	LVDS_B2+
76	LVDS_A2-	LVDS_B2-	LVDS_A2-	LVDS_B2-	LVDS_A2-	LVDS_B2-	LVDS_A2-	LVDS_B2-
77	LVDS_VDD_EN	LVDS_B3+	LVDS_VDD_EN	LVDS_B3+	LVDS_VDD_EN	LVDS_B3+	LVDS_VDD_EN	LVDS_B3+
78	LVDS_A3+	LVDS_B3-	LVDS_A3+	LVDS_B3-	LVDS_A3+	LVDS_B3-	LVDS_A3+	LVDS_B3-
79	LVDS_A3-	LVDS_BKLT_EN	LVDS_A3-	LVDS_BKLT_EN	LVDS_A3-	LVDS_BKLT_EN	LVDS_A3-	LVDS_BKLT_EN
80	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
81	LVDS_A_CK+	LVDS_B_CK+	LVDS_A_CK+	LVDS_B_CK+	LVDS_A_CK+	LVDS_B_CK+	LVDS_A_CK+	LVDS_B_CK+
82	LVDS_A_CK-	LVDS_B_CK-	LVDS_A_CK-	LVDS_B_CK-	LVDS_A_CK-	LVDS_B_CK-	LVDS_A_CK-	LVDS_B_CK-

	TYPE 2 Rev. 1.0		TYPE 2 Rev. 2.0		TYPE 6 Rev. 2.0		TYPE 6 Rev. 2.1	
Pin	Row A	Row B	Row A	Row B	Row A	Row B	Row A	Row B
83	LVDS_I2C_CK	LVDS_BKLT_CTRL	LVDS_I2C_CK	LVDS_BKLT_CTRL	LVDS_I2C_CK	LVDS_BKLT_CTRL	LVDS_I2C_CK	LVDS_BKLT_CTRL
84	LVDS_I2C_DAT	VCC_5V_SBY	LVDS_I2C_DAT	VCC_5V_SBY	LVDS_I2C_DAT	VCC_5V_SBY	LVDS_I2C_DAT	VCC_5V_SBY
85	GPI3	VCC_5V_SBY	GPI3	VCC_5V_SBY	GPI3	VCC_5V_SBY	GPI3	VCC_5V_SBY
86	KBD_RST#	VCC_5V_SBY	KBD_RST#	VCC_5V_SBY	**RSVD**	VCC_5V_SBY	**RSVD**	VCC_5V_SBY
87	KBD_A20GATE	VCC_5V_SBY	KBD_A20GATE	VCC_5V_SBY	**RSVD**	VCC_5V_SBY	**eDP_HPD**	VCC_5V_SBY
88	PCIE_CLK_REF+	RSVD	PCIE_CLK_REF+	**BIOS_DIS1#**	PCIE_CLK_REF+	BIOS_DIS1#	PCIE_CLK_REF+	BIOS_DIS1#
89	PCIE_CLK_REF-	VGA_RED	PCIE_CLK_REF-	VGA_RED	PCIE_CLK_REF-	VGA_RED	PCIE_CLK_REF-	VGA_RED
90	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
91	RSVD	VGA_GRN	**SPI_POWER**	VGA_GRN	**SPI_POWER**	VGA_GRN	**SPI_POWER**	VGA_GRN
92	RSVD	VGA_BLU	**SPI_MISO**	VGA_BLU	**SPI_MISO**	VGA_BLU	**SPI_MISO**	VGA_BLU
93	GPO0	VGA_HSYNC	GPO0	VGA_HSYNC	GPO0	VGA_HSYNC	GPO0	VGA_HSYNC
94	RSVD	VGA_VSYNC	**SPI_CLK**	VGA_VSYNC	**SPI_CLK**	VGA_VSYNC	**SPI_CLK**	VGA_VSYNC
95	RSVD	VGA_I2C_CK	**SPI_MOSI**	VGA_I2C_CK	**SPI_MOSI**	VGA_I2C_CK	**SPI_MOSI**	VGA_I2C_CK
96	GND	VGA_I2C_DAT	GND	VGA_I2C_DAT	**TPM_PP**	VGA_I2C_DAT	**TPM_PP**	VGA_I2C_DAT
97	VCC_12V	TV_DAC_A	**TYPE10#**	**SPI_CS#**	**TYPE10#**	**SPI_CS#**	**TYPE10#**	**SPI_CS#**
98	VCC_12V	TV_DAC_B	**RSVD**	**RSVD**	**SER0_TX**	**RSVD**	**SER0_TX**	**RSVD**
99	VCC_12V	TV_DAC_C	**RSVD**	**RSVD**	**SER0_RX**	**RSVD**	**SER0_RX**	**RSVD**
100	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
101	VCC_12V	VCC_12V	**RSVD**	**RSVD**	**SER1_TX**	**FAN_PWMOUT**	**SER1_TX**	**FAN_PWMOUT**
102	VCC_12V	VCC_12V	**RSVD**	**RSVD**	**SER1_RX**	**FAN_TACHIN**	**SER1_RX**	**FAN_TACHIN**
103	VCC_12V	VCC_12V	**RSVD**	**RSVD**	**LID#**	**SLEEP#**	**LID#**	**SLEEP#**
104	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
109	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
110	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)

	TYPE 2 Rev. 1.0		TYPE 2 Rev. 2.0		TYPE 6 Rev. 2.0		TYPE 6 Rev. 2.1	
Pin	Row C	Row D	Row C	Row D	Row C	Row D	Row C	Row D
1	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
2	IDE_D7	IDE_D5	IDE_D7	IDE_D5	**GND**	**GND**	**GND**	**GND**
3	IDE_D6	IDE_D10	IDE_D6	IDE_D10	**USB_SSRX0-**	**USB_SSTX0-**	**USB_SSRX0-**	**USB_SSTX0-**
4	IDE_D3	IDE_D11	IDE_D3	IDE_D11	**USB_SSRX0+**	**USB_SSTX0+**	**USB_SSRX0+**	**USB_SSTX0+**
5	IDE_D15	IDE_D12	IDE_D15	IDE_D12	**GND**	**GND**	**GND**	**GND**
6	IDE_D8	IDE_D4	IDE_D8	IDE_D4	**USB_SSRX1-**	**USB_SSTX1-**	**USB_SSRX1-**	**USB_SSTX1-**
7	IDE_D9	IDE_D0	IDE_D9	IDE_D0	**USB_SSRX1+**	**USB_SSTX1+**	**USB_SSRX1+**	**USB_SSTX1+**
8	IDE_D2	IDE_REQ	IDE_D2	IDE_REQ	**GND**	**GND**	**GND**	**GND**
9	IDE_D13	IDE_IOW#	IDE_D13	IDE_IOW#	**USB_SSRX2-**	**USB_SSTX2-**	**USB_SSRX2-**	**USB_SSTX2-**
10	IDE_D1	IDE_ACK#	IDE_D1	IDE_ACK#	**USB_SSRX2+**	**USB_SSTX2+**	**USB_SSRX2+**	**USB_SSTX2+**
11	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
12	IDE_D14	IDE_IRQ	IDE_D14	IDE_IRQ	**USB_SSRX3-**	**USB_SSTX3-**	**USB_SSRX3-**	**USB_SSTX3-**
13	IDE_IORDY	IDE_A0	IDE_IORDY	IDE_A0	**USB_SSRX3+**	**USB_SSTX3+**	**USB_SSRX3+**	**USB_SSTX3+**
14	IDE_IOR#	IDE_A1	IDE_IOR#	IDE_A1	**GND**	**GND**	**GND**	**GND**
15	PCI_PME#	IDE_A2	PCI_PME#	IDE_A2	**DDI1_PAIR6+**	**DDI1_CTRLCLK_AUX+**	**DDI1_PAIR6+**	**DDI1_CTRLCLK_AUX+**
16	PCI_GNT2#	IDE_CS1#	PCI_GNT2#	IDE_CS1#	**DDI1_PAIR6-**	**DDI1_CTRLDATA_AUX-**	**DDI1_PAIR6-**	**DDI1_CTRLDATA_AUX-**
17	PCI_REQ2#	IDE_CS3#	PCI_REQ2#	IDE_CS3#	**RSVD**	**RSVD**	**RSVD**	**RSVD**
18	PCI_GNT1#	IDE_RESET#	PCI_GNT1#	IDE_RESET#	**RSVD**	**RSVD**	**RSVD**	**RSVD**
19	PCI_REQ1#	PCI_GNT3#	PCI_REQ1#	PCI_GNT3#	**PCIE_RX6+**	**PCIE_TX6+**	**PCIE_RX6+**	**PCIE_TX6+**
20	PCI_GNT0#	PCI_REQ3#	PCI_GNT0#	PCI_REQ3#	**PCIE_RX6-**	**PCIE_TX6-**	**PCIE_RX6-**	**PCIE_TX6-**
21	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
22	PCI_REQ0#	PCI_AD1	PCI_REQ0#	PCI_AD1	**PCIE_RX7+**	**PCIE_TX7+**	**PCIE_RX7+**	**PCIE_TX7+**
23	PCI_RESET#	PCI_AD3	PCI_RESET#	PCI_AD3	**PCIE_RX7-**	**PCIE_TX7-**	**PCIE_RX7-**	**PCIE_TX7-**
24	PCI_AD0	PCI_AD5	PCI_AD0	PCI_AD5	**DDI1_HPD**	**RSVD**	**DDI1_HPD**	**RSVD**
25	PCI_AD2	PCI_AD7	PCI_AD2	PCI_AD7	**DDI1_PAIR4 +**	**RSVD**	**DDI1_PAIR4 +**	**RSVD**
26	PCI_AD4	PCI_C/BE0#	PCI_AD4	PCI_C/BE0#	**DDI1_PAIR4-**	**DDI1_PAIR0+**	**DDI1_PAIR4-**	**DDI1_PAIR0+**
27	PCI_AD6	PCI_AD9	PCI_AD6	PCI_AD9	**RSVD**	**DDI1_PAIR0-**	**RSVD**	**DDI1_PAIR0-**
28	PCI_AD8	PCI_AD11	PCI_AD8	PCI_AD11	**RSVD**	**RSVD**	**RSVD**	**RSVD**
29	PCI_AD10	PCI_AD13	PCI_AD10	PCI_AD13	**DDI1_PAIR5+**	**DDI1_PAIR1+**	**DDI1_PAIR5+**	**DDI1_PAIR1+**

	TYPE 2 Rev. 1.0		TYPE 2 Rev. 2.0		TYPE 6 Rev. 2.0		TYPE 6 Rev. 2.1	
Pin	Row C	Row D	Row C	Row D	Row C	Row D	Row C	Row D
30	PCI_AD12	PCI_AD15	PCI_AD12	PCI_AD15	**DDI1_PAIR5-**	**DDI1_PAIR1-**	**DDI1_PAIR5-**	**DDI1_PAIR1-**
31	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
32	PCI_AD14	PCI_PAR	PCI_AD14	PCI_PAR	**DDI2_CTRLCLK_AUX+**	**DDI1_PAIR2+**	**DDI2_CTRLCLK_AUX+**	**DDI1_PAIR2+**
33	PCI_C/BE1#	PCI_SERR#	PCI_C/BE1#	PCI_SERR#	**DDI2_CTRLDATA_AUX-**	**DDI1_PAIR2-**	**DDI2_CTRLDATA_AUX-**	**DDI1_PAIR2-**
34	PCI_PERR#	PCI_STOP#	PCI_PERR#	PCI_STOP#	**DDI2_DDC_AUX_SEL**	**DDI1_DDC_AUX_SEL**	**DDI2_DDC_AUX_SEL**	**DDI1_DDC_AUX_SEL**
35	PCI_LOCK#	PCI_TRDY#	PCI_LOCK#	PCI_TRDY#	**RSVD**	**RSVD**	**RSVD**	**RSVD**
36	PCI_DEVSEL#	PCI_FRAME#	PCI_DEVSEL#	PCI_FRAME#	**DDI3_CTRLCLK_AUX+**	**DDI1_PAIR3+**	**DDI3_CTRLCLK_AUX+**	**DDI1_PAIR3+**
37	PCI_IRDY#	PCI_AD16	PCI_IRDY#	PCI_AD16	**DDI3_CTRLDATA_AUX-**	**DDI1_PAIR3-**	**DDI3_CTRLDATA_AUX-**	**DDI1_PAIR3-**
38	PCI_C/BE2#	PCI_AD18	PCI_C/BE2#	PCI_AD18	**DDI3_DDC_AUX_SEL**	**RSVD**	**DDI3_DDC_AUX_SEL**	**RSVD**
39	PCI_AD17	PCI_AD20	PCI_AD17	PCI_AD20	**DDI3_PAIR0+**	**DDI2_PAIR0+**	**DDI3_PAIR0+**	**DDI2_PAIR0+**
40	PCI_AD19	PCI_AD22	PCI_AD19	PCI_AD22	**DDI3_PAIR0-**	**DDI2_PAIR0-**	**DDI3_PAIR0-**	**DDI2_PAIR0-**
41	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
42	PCI_AD21	PCI_AD24	PCI_AD21	PCI_AD24	**DDI3_PAIR1+**	**DDI2_PAIR1+**	**DDI3_PAIR1+**	**DDI2_PAIR1+**
43	PCI_AD23	PCI_AD26	PCI_AD23	PCI_AD26	**DDI3_PAIR1-**	**DDI2_PAIR1-**	**DDI3_PAIR1-**	**DDI2_PAIR1-**
44	PCI_C/BE3#	PCI_AD28	PCI_C/BE3#	PCI_AD28	**DDI3_HPD**	**DDI2_HPD**	**DDI3_HPD**	**DDI2_HPD**
45	PCI_AD25	PCI_AD30	PCI_AD25	PCI_AD30	**RSVD**	**RSVD**	**RSVD**	**RSVD**
46	PCI_AD27	PCI_IRQC#	PCI_AD27	PCI_IRQC#	**DDI3_PAIR2+**	**DDI2_PAIR2+**	**DDI3_PAIR2+**	**DDI2_PAIR2+**
47	PCI_AD29	PCI_IRQD#	PCI_AD29	PCI_IRQD#	**DDI3_PAIR2-**	**DDI2_PAIR2-**	**DDI3_PAIR2-**	**DDI2_PAIR2-**
48	PCI_AD31	PCI_CLKRUN#	PCI_AD31	PCI_CLKRUN#	**RSVD**	**RSVD**	**RSVD**	**RSVD**
49	PCI_IRQA#	PCI_M66EN	PCI_IRQA#	PCI_M66EN	**DDI3_PAIR3+**	**DDI2_PAIR3+**	**DDI3_PAIR3+**	**DDI2_PAIR3+**
50	PCI_IRQB#	PCI_CLK	PCI_IRQB#	PCI_CLK	**DDI3_PAIR3-**	**DDI2_PAIR3-**	**DDI3_PAIR3-**	**DDI2_PAIR3-**
51	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
52	PEG_RX0+	PEG_TX0+	PEG_RX0+	PEG_TX0+	PEG_RX0+	PEG_TX0+	PEG_RX0+	PEG_TX0+
53	PEG_RX0-	PEG_TX0-	PEG_RX0-	PEG_TX0-	PEG_RX0-	PEG_TX0-	PEG_RX0-	PEG_TX0-
54	TYPE0#	PEG_LANE_RV#	TYPE0#	PEG_LANE_RV#	TYPE0#	PEG_LANE_RV#	TYPE0#	PEG_LANE_RV#
55	PEG_RX1+	PEG_TX1+	PEG_RX1+	PEG_TX1+	PEG_RX1+	PEG_TX1+	PEG_RX1+	PEG_TX1+
56	PEG_RX1-	PEG_TX1-	PEG_RX1-	PEG_TX1-	PEG_RX1-	PEG_TX1-	PEG_RX1-	PEG_TX1-
57	TYPE1#	TYPE2#	TYPE1#	TYPE2#	TYPE1#	TYPE2#	TYPE1#	TYPE2#
58	PEG_RX2+	PEG_TX2+	PEG_RX2+	PEG_TX2+	PEG_RX2+	PEG_TX2+	PEG_RX2+	PEG_TX2+

	TYPE 2 Rev. 1.0		TYPE 2 Rev. 2.0		TYPE 6 Rev. 2.0		TYPE 6 Rev. 2.1	
Pin	**Row C**	**Row D**	**Row C**	**Row D**	**Row C**	**Row D**	**Row C**	**Row D**
59	PEG_RX2-	PEG_TX2-	PEG_RX2-	PEG_TX2-	PEG_RX2-	PEG_TX2-	PEG_RX2-	PEG_TX2-
60	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
61	PEG_RX3+	PEG_TX3+	PEG_RX3+	PEG_TX3+	PEG_RX3+	PEG_TX3+	PEG_RX3+	PEG_TX3+
62	PEG_RX3-	PEG_TX3-	PEG_RX3-	PEG_TX3-	PEG_RX3-	PEG_TX3-	PEG_RX3-	PEG_TX3-
63	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
64	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
65	PEG_RX4+	PEG_TX4+	PEG_RX4+	PEG_TX4+	PEG_RX4+	PEG_TX4+	PEG_RX4+	PEG_TX4+
66	PEG_RX4-	PEG_TX4-	PEG_RX4-	PEG_TX4-	PEG_RX4-	PEG_TX4-	PEG_RX4-	PEG_TX4-
67	RSVD	GND	**RSVD**	GND	RSVD	GND	RSVD	GND
68	PEG_RX5+	PEG_TX5+	PEG_RX5+	PEG_TX5+	PEG_RX5+	PEG_TX5+	PEG_RX5+	PEG_TX5+
69	PEG_RX5-	PEG_TX5-	PEG_RX5-	PEG_TX5-	PEG_RX5-	PEG_TX5-	PEG_RX5-	PEG_TX5-
70	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
71	PEG_RX6+	PEG_TX6+	PEG_RX6+	PEG_TX6+	PEG_RX6+	PEG_TX6+	PEG_RX6+	PEG_TX6+
72	PEG_RX6-	PEG_TX6-	PEG_RX6-	PEG_TX6-	PEG_RX6-	PEG_TX6-	PEG_RX6-	PEG_TX6-
73	SDVO_DATA	SDVO_CLK	SDVO_DATA	SDVO_CLK	**GND**	**GND**	**GND**	**GND**
74	PEG_RX7+	PEG_TX7+	PEG_RX7+	PEG_TX7+	PEG_RX7+	PEG_TX7+	PEG_RX7+	PEG_TX7+
75	PEG_RX7-	PEG_TX7-	PEG_RX7-	PEG_TX7-	PEG_RX7-	PEG_TX7-	PEG_RX7-	PEG_TX7-
76	GND	GND	GND	GND	GND	GND	GND	GND
77	RSVD	IDE_CBLID#	RSVD	IDE_CBLID#	RSVD	**RSVD**	RSVD	**RSVD**
78	PEG_RX8+	PEG_TX8+	PEG_RX8+	PEG_TX8+	PEG_RX8+	PEG_TX8+	PEG_RX8+	PEG_TX8+
79	PEG_RX8-	PEG_TX8-	PEG_RX8-	PEG_TX8-	PEG_RX8-	PEG_TX8-	PEG_RX8-	PEG_TX8-
80	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
81	PEG_RX9+	PEG_TX9+	PEG_RX9+	PEG_TX9+	PEG_RX9+	PEG_TX9+	PEG_RX9+	PEG_TX9+
82	PEG_RX9-	PEG_TX9-	PEG_RX9-	PEG_TX9-	PEG_RX9-	PEG_TX9-	PEG_RX9-	PEG_TX9-
83	RSVD	RSVD	**RSVD**	RSVD	RSVD	RSVD	RSVD	RSVD
84	GND	GND	GND	GND	GND	GND	GND	GND
85	PEG_RX10+	PEG_TX10+	PEG_RX10+	PEG_TX10+	PEG_RX10+	PEG_TX10+	PEG_RX10+	PEG_TX10+
86	PEG_RX10-	PEG_TX10-	PEG_RX10-	PEG_TX10-	PEG_RX10-	PEG_TX10-	PEG_RX10-	PEG_TX10-
87	GND	GND	GND	GND	GND	GND	GND	GND

	TYPE 2 Rev. 1.0		TYPE 2 Rev. 2.0		TYPE 6 Rev. 2.0		TYPE 6 Rev. 2.1	
Pin	**Row C**	**Row D**	**Row C**	**Row D**	**Row C**	**Row D**	**Row C**	**Row D**
88	PEG_RX11+	PEG_TX11+	PEG_RX11+	PEG_TX11+	PEG_RX11+	PEG_TX11+	PEG_RX11+	PEG_TX11+
89	PEG_RX11-	PEG_TX11-	PEG_RX11-	PEG_TX11-	PEG_RX11-	PEG_TX11-	PEG_RX11-	PEG_TX11-
90	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
91	PEG_RX12+	PEG_TX12+	PEG_RX12+	PEG_TX12+	PEG_RX12+	PEG_TX12+	PEG_RX12+	PEG_TX12+
92	PEG_RX12-	PEG_TX12-	PEG_RX12-	PEG_TX12-	PEG_RX12-	PEG_TX12-	PEG_RX12-	PEG_TX12-
93	GND	GND	GND	GND	GND	GND	GND	GND
94	PEG_RX13+	PEG_TX13+	PEG_RX13+	PEG_TX13+	PEG_RX13+	PEG_TX13+	PEG_RX13+	PEG_TX13+
95	PEG_RX13-	PEG_TX13-	PEG_RX13-	PEG_TX13-	PEG_RX13-	PEG_TX13-	PEG_RX13-	PEG_TX13-
96	GND	GND	GND	GND	GND	GND	GND	GND
97	RSVD	PEG_ENABLE#	RSVD	PEG_ENABLE#	RSVD	**RSVD**	RSVD	**RSVD**
98	PEG_RX14+	PEG_TX14+	PEG_RX14+	PEG_TX14+	PEG_RX14+	PEG_TX14+	PEG_RX14+	PEG_TX14+
99	PEG_RX14-	PEG_TX14-	PEG_RX14-	PEG_TX14-	PEG_RX14-	PEG_TX14-	PEG_RX14-	PEG_TX14-
100	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
101	PEG_RX15+	PEG_TX15+	PEG_RX15+	PEG_TX15+	PEG_RX15+	PEG_TX15+	PEG_RX15+	PEG_TX15+
102	PEG_RX15-	PEG_TX15-	PEG_RX15-	PEG_TX15-	PEG_RX15-	PEG_TX15-	PEG_RX15-	PEG_TX15-
103	GND	GND	GND	GND	GND	GND	GND	GND
104	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
109	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
110	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)

9.4 Comparison of Types 2 to 5

Bold text indicates a difference to Type 2.

Table 9.3: Comparison of Type 2, Type 3, Type 4 and Type 5 Pin-Out

	TYPE 2 Rev. 2.0		TYPE 3 Rev. 2.0		TYPE 4 Rev. 2.0		TYPE 5 Rev. 2.0	
Pin	Row A	Row B	Row A	Row B	Row A	Row B	Row A	Row B
1	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
2	GBE0_MDI3-	GBE0_ACT#	GBE0_MDI3-	GBE0_ACT#	GBE0_MDI3-	GBE0_ACT#	GBE0_MDI3-	GBE0_ACT#
3	GBE0_MDI3+	LPC_FRAME#	GBE0_MDI3+	LPC_FRAME#	GBE0_MDI3+	LPC_FRAME#	GBE0_MDI3+	LPC_FRAME#
4	GBE0_LINK100#	LPC_AD0	GBE0_LINK100#	LPC_AD0	GBE0_LINK100#	LPC_AD0	GBE0_LINK100#	LPC_AD0
5	GBE0_LINK1000#	LPC_AD1	GBE0_LINK1000#	LPC_AD1	GBE0_LINK1000#	LPC_AD1	GBE0_LINK1000#	LPC_AD1
6	GBE0_MDI2-	LPC_AD2	GBE0_MDI2-	LPC_AD2	GBE0_MDI2-	LPC_AD2	GBE0_MDI2-	LPC_AD2
7	GBE0_MDI2+	LPC_AD3	GBE0_MDI2+	LPC_AD3	GBE0_MDI2+	LPC_AD3	GBE0_MDI2+	LPC_AD3
8	GBE0_LINK#	LPC_DRQ0#	GBE0_LINK#	LPC_DRQ0#	GBE0_LINK#	LPC_DRQ0#	GBE0_LINK#	LPC_DRQ0#
9	GBE0_MDI1-	LPC_DRQ1#	GBE0_MDI1-	LPC_DRQ1#	GBE0_MDI1-	LPC_DRQ1#	GBE0_MDI1-	LPC_DRQ1#
10	GBE0_MDI1+	LPC_CLK	GBE0_MDI1+	LPC_CLK	GBE0_MDI1+	LPC_CLK	GBE0_MDI1+	LPC_CLK
11	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
12	GBE0_MDI0-	PWRBTN#	GBE0_MDI0-	PWRBTN#	GBE0_MDI0-	PWRBTN#	GBE0_MDI0-	PWRBTN#
13	GBE0_MDI0+	SMB_CK	GBE0_MDI0+	SMB_CK	GBE0_MDI0+	SMB_CK	GBE0_MDI0+	SMB_CK
14	GBE0_CTREF	SMB_DAT	GBE0_CTREF	SMB_DAT	GBE0_CTREF	SMB_DAT	GBE0_CTREF	SMB_DAT
15	SUS_S3#	SMB_ALERT#	SUS_S3#	SMB_ALERT#	SUS_S3#	SMB_ALERT#	SUS_S3#	SMB_ALERT#
16	SATA0_TX+	SATA1_TX+	SATA0_TX+	SATA1_TX+	SATA0_TX+	SATA1_TX+	SATA0_TX+	SATA1_TX+
17	SATA0_TX-	SATA1_TX-	SATA0_TX-	SATA1_TX-	SATA0_TX-	SATA1_TX-	SATA0_TX-	SATA1_TX-
18	SUS_S4#	SUS_STAT#	SUS_S4#	SUS_STAT#	SUS_S4#	SUS_STAT#	SUS_S4#	SUS_STAT#
19	SATA0_RX+	SATA1_RX+	SATA0_RX+	SATA1_RX+	SATA0_RX+	SATA1_RX+	SATA0_RX+	SATA1_RX+
20	SATA0_RX-	SATA1_RX-	SATA0_RX-	SATA1_RX-	SATA0_RX-	SATA1_RX-	SATA0_RX-	SATA1_RX-
21	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
22	SATA2_TX+	SATA3_TX+	SATA2_TX+	SATA3_TX+	SATA2_TX+	SATA3_TX+	SATA2_TX+	SATA3_TX+
23	SATA2_TX-	SATA3_TX-	SATA2_TX-	SATA3_TX-	SATA2_TX-	SATA3_TX-	SATA2_TX-	SATA3_TX-
24	SUS_S5#	PWR_OK	SUS_S5#	PWR_OK	SUS_S5#	PWR_OK	SUS_S5#	PWR_OK
25	SATA2_RX+	SATA3_RX+	SATA2_RX+	SATA3_RX+	SATA2_RX+	SATA3_RX+	SATA2_RX+	SATA3_RX+
26	SATA2_RX-	SATA3_RX-	SATA2_RX-	SATA3_RX-	SATA2_RX-	SATA3_RX-	SATA2_RX-	SATA3_RX-
27	BATLOW#	WDT	BATLOW#	WDT	BATLOW#	WDT	BATLOW#	WDT
28	(S)ATA_ACT#	AC/HDA_SDIN2	(S)ATA_ACT#	AC/HDA_SDIN2	(S)ATA_ACT#	AC/HDA_SDIN2	(S)ATA_ACT#	AC/HDA_SDIN2
29	AC/HDA_SYNC	AC/HDA_SDIN1	AC/HDA_SYNC	AC/HDA_SDIN1	AC/HDA_SYNC	AC/HDA_SDIN1	AC/HDA_SYNC	AC/HDA_SDIN1
30	AC/HDA_RST#	AC/HDA_SDIN0	AC/HDA_RST#	AC/HDA_SDIN0	AC/HDA_RST#	AC/HDA_SDIN0	AC/HDA_RST#	AC/HDA_SDIN0
31	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
32	AC/HDA_BITCLK	SPKR	AC/HDA_BITCLK	SPKR	AC/HDA_BITCLK	SPKR	AC/HDA_BITCLK	SPKR
33	AC/HDA_SDOUT	I2C_CK	AC/HDA_SDOUT	I2C_CK	AC/HDA_SDOUT	I2C_CK	AC/HDA_SDOUT	I2C_CK
34	BIOS_DIS0#	I2C_DAT	BIOS_DIS0#	I2C_DAT	BIOS_DIS0#	I2C_DAT	BIOS_DIS0#	I2C_DAT
35	THRMTRIP#	THRM#	THRMTRIP#	THRM#	THRMTRIP#	THRM#	THRMTRIP#	THRM#
36	USB6-	USB7-	USB6-	USB7-	USB6-	USB7-	USB6-	USB7-
37	USB6+	USB7+	USB6+	USB7+	USB6+	USB7+	USB6+	USB7+

	TYPE 2 Rev. 2.0		TYPE 3 Rev. 2.0		TYPE 4 Rev. 2.0		TYPE 5 Rev. 2.0	
Pin	Row A	Row B	Row A	Row B	Row A	Row B	Row A	Row B
38	USB_6_7_OC#	USB_4_5_OC#	USB_6_7_OC#	USB_4_5_OC#	USB_6_7_OC#	USB_4_5_OC#	USB_6_7_OC#	USB_4_5_OC#
39	USB4-	USB5-	USB4-	USB5-	USB4-	USB5-	USB4-	USB5-
40	USB4+	USB5+	USB4+	USB5+	USB4+	USB5+	USB4+	USB5+
41	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
42	USB2-	USB3-	USB2-	USB3-	USB2-	USB3-	USB2-	USB3-
43	USB2+	USB3+	USB2+	USB3+	USB2+	USB3+	USB2+	USB3+
44	USB_2_3_OC#	USB_0_1_OC#	USB_2_3_OC#	USB_0_1_OC#	USB_2_3_OC#	USB_0_1_OC#	USB_2_3_OC#	USB_0_1_OC#
45	USB0-	USB1-	USB0-	USB1-	USB0-	USB1-	USB0-	USB1-
46	USB0+	USB1+	USB0+	USB1+	USB0+	USB1+	USB0+	USB1+
47	VCC_RTC	EXCD1_PERST#	VCC_RTC	EXCD1_PERST#	VCC_RTC	EXCD1_PERST#	VCC_RTC	EXCD1_PERST#
48	EXCD0_PERST#	EXCD1_CPPE#	EXCD0_PERST#	EXCD1_CPPE#	EXCD0_PERST#	EXCD1_CPPE#	EXCD0_PERST#	EXCD1_CPPE#
49	EXCD0_CPPE#	SYS_RESET#	EXCD0_CPPE#	SYS_RESET#	EXCD0_CPPE#	SYS_RESET#	EXCD0_CPPE#	SYS_RESET#
50	LPC_SERIRQ	CB_RESET#	LPC_SERIRQ	CB_RESET#	LPC_SERIRQ	CB_RESET#	LPC_SERIRQ	CB_RESET#
51	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
52	PCIE_TX5+	PCIE_RX5+	PCIE_TX5+	PCIE_RX5+	PCIE_TX5+	PCIE_RX5+	PCIE_TX5+	PCIE_RX5+
53	PCIE_TX5-	PCIE_RX5-	PCIE_TX5-	PCIE_RX5-	PCIE_TX5-	PCIE_RX5-	PCIE_TX5-	PCIE_RX5-
54	GPI0	GPO1	GPI0	GPO1	GPI0	GPO1	GPI0	GPO1
55	PCIE_TX4+	PCIE_RX4+	PCIE_TX4+	PCIE_RX4+	PCIE_TX4+	PCIE_RX4+	PCIE_TX4+	PCIE_RX4+
56	PCIE_TX4-	PCIE_RX4-	PCIE_TX4-	PCIE_RX4-	PCIE_TX4-	PCIE_RX4-	PCIE_TX4-	PCIE_RX4-
57	GND	GPO2	GND	GPO2	GND	GPO2	GND	GPO2
58	PCIE_TX3+	PCIE_RX3+	PCIE_TX3+	PCIE_RX3+	PCIE_TX3+	PCIE_RX3+	PCIE_TX3+	PCIE_RX3+
59	PCIE_TX3-	PCIE_RX3-	PCIE_TX3-	PCIE_RX3-	PCIE_TX3-	PCIE_RX3-	PCIE_TX3-	PCIE_RX3-
60	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
61	PCIE_TX2+	PCIE_RX2+	PCIE_TX2+	PCIE_RX2+	PCIE_TX2+	PCIE_RX2+	PCIE_TX2+	PCIE_RX2+
62	PCIE_TX2-	PCIE_RX2-	PCIE_TX2-	PCIE_RX2-	PCIE_TX2-	PCIE_RX2-	PCIE_TX2-	PCIE_RX2-
63	GPI1	GPO3	GPI1	GPO3	GPI1	GPO3	GPI1	GPO3
64	PCIE_TX1+	PCIE_RX1+	PCIE_TX1+	PCIE_RX1+	PCIE_TX1+	PCIE_RX1+	PCIE_TX1+	PCIE_RX1+
65	PCIE_TX1-	PCIE_RX1-	PCIE_TX1-	PCIE_RX1-	PCIE_TX1-	PCIE_RX1-	PCIE_TX1-	PCIE_RX1-
66	GND	WAKE0#	GND	WAKE0#	GND	WAKE0#	GND	WAKE0#
67	GPI2	WAKE1#	GPI2	WAKE1#	GPI2	WAKE1#	GPI2	WAKE1#
68	PCIE_TX0+	PCIE_RX0+	PCIE_TX0+	PCIE_RX0+	PCIE_TX0+	PCIE_RX0+	PCIE_TX0+	PCIE_RX0+
69	PCIE_TX0-	PCIE_RX0-	PCIE_TX0-	PCIE_RX0-	PCIE_TX0-	PCIE_RX0-	PCIE_TX0-	PCIE_RX0-
70	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
71	LVDS_A0+	LVDS_B0+	LVDS_A0+	LVDS_B0+	LVDS_A0+	LVDS_B0+	LVDS_A0+	LVDS_B0+
72	LVDS_A0-	LVDS_B0-	LVDS_A0-	LVDS_B0-	LVDS_A0-	LVDS_B0-	LVDS_A0-	LVDS_B0-
73	LVDS_A1+	LVDS_B1+	LVDS_A1+	LVDS_B1+	LVDS_A1+	LVDS_B1+	LVDS_A1+	LVDS_B1+
74	LVDS_A1-	LVDS_B1-	LVDS_A1-	LVDS_B1-	LVDS_A1-	LVDS_B1-	LVDS_A1-	LVDS_B1-
75	LVDS_A2+	LVDS_B2+	LVDS_A2+	LVDS_B2+	LVDS_A2+	LVDS_B2+	LVDS_A2+	LVDS_B2+
76	LVDS_A2-	LVDS_B2-	LVDS_A2-	LVDS_B2-	LVDS_A2-	LVDS_B2-	LVDS_A2-	LVDS_B2-
77	LVDS_VDD_EN	LVDS_B3+	LVDS_VDD_EN	LVDS_B3+	LVDS_VDD_EN	LVDS_B3+	LVDS_VDD_EN	LVDS_B3+
78	LVDS_A3+	LVDS_B3-	LVDS_A3+	LVDS_B3-	LVDS_A3+	LVDS_B3-	LVDS_A3+	LVDS_B3-
79	LVDS_A3-	LVDS_BKLT_EN	LVDS_A3-	LVDS_BKLT_EN	LVDS_A3-	LVDS_BKLT_EN	LVDS_A3-	LVDS_BKLT_EN
80	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
81	LVDS_A_CK+	LVDS_B_CK+	LVDS_A_CK+	LVDS_B_CK+	LVDS_A_CK+	LVDS_B_CK+	LVDS_A_CK+	LVDS_B_CK+
82	LVDS_A_CK-	LVDS_B_CK-	LVDS_A_CK-	LVDS_B_CK-	LVDS_A_CK-	LVDS_B_CK-	LVDS_A_CK-	LVDS_B_CK-

	TYPE 2 Rev. 2.0		TYPE 3 Rev. 2.0		TYPE 4 Rev. 2.0		TYPE 5 Rev. 2.0	
Pin	**Row A**	**Row B**	**Row A**	**Row B**	**Row A**	**Row B**	**Row A**	**Row B**
83	LVDS_I2C_CK	LVDS_BKLT_CTRL	LVDS_I2C_CK	LVDS_BKLT_CTRL	LVDS_I2C_CK	LVDS_BKLT_CTRL	LVDS_I2C_CK	LVDS_BKLT_CTRL
84	LVDS_I2C_DAT	VCC_5V_SBY	LVDS_I2C_DAT	VCC_5V_SBY	LVDS_I2C_DAT	VCC_5V_SBY	LVDS_I2C_DAT	VCC_5V_SBY
85	GPI3	VCC_5V_SBY	GPI3	VCC_5V_SBY	GPI3	VCC_5V_SBY	GPI3	VCC_5V_SBY
86	KBD_RST#	VCC_5V_SBY	KBD_RST#	VCC_5V_SBY	KBD_RST#	VCC_5V_SBY	KBD_RST#	VCC_5V_SBY
87	KBD_A20GATE	VCC_5V_SBY	KBD_A20GATE	VCC_5V_SBY	KBD_A20GATE	VCC_5V_SBY	KBD_A20GATE	VCC_5V_SBY
88	PCIE_CLK_REF+	BIOS_DIS1#	PCIE_CLK_REF+	BIOS_DIS1#	PCIE_CLK_REF+	BIOS_DIS1#	PCIE_CLK_REF+	BIOS_DIS1#
89	PCIE_CLK_REF-	VGA_RED	PCIE_CLK_REF-	VGA_RED	PCIE_CLK_REF-	VGA_RED	PCIE_CLK_REF-	VGA_RED
90	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
91	SPI_POWER	VGA_GRN	SPI_POWER	VGA_GRN	SPI_POWER	VGA_GRN	SPI_POWER	VGA_GRN
92	SPI_MISO	VGA_BLU	SPI_MISO	VGA_BLU	SPI_MISO	VGA_BLU	SPI_MISO	VGA_BLU
93	GPO0	VGA_HSYNC	GPO0	VGA_HSYNC	GPO0	VGA_HSYNC	GPO0	VGA_HSYNC
94	SPI_CLK	VGA_VSYNC	SPI_CLK	VGA_VSYNC	SPI_CLK	VGA_VSYNC	SPI_CLK	VGA_VSYNC
95	SPI_MOSI	VGA_I2C_CK	SPI_MOSI	VGA_I2C_CK	SPI_MOSI	VGA_I2C_CK	SPI_MOSI	VGA_I2C_CK
96	GND	VGA_I2C_DAT	GND	VGA_I2C_DAT	GND	VGA_I2C_DAT	GND	VGA_I2C_DAT
97	TYPE10#	SPI_CS#	TYPE10#	SPI_CS#	TYPE10#	SPI_CS#	TYPE10#	SPI_CS#
98	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
99	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
100	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
101	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
102	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
103	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
104	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
109	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
110	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)

	TYPE 2 Rev. 2.0		TYPE 3 Rev. 2.0		TYPE 4 Rev. 2.0		TYPE 5 Rev. 2.0	
Pin	**Row C**	**Row D**	**Row C**	**Row D**	**Row C**	**Row D**	**Row C**	**Row D**
1	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
2	IDE_D7	IDE_D5	**GBE1_ACT#**	**GBE2_ACT#**	IDE_D7	IDE_D5	**GBE1_ACT#**	**GBE2_ACT#**
3	IDE_D6	IDE_D10	**GBE1_MDI3-**	**GBE2_MDI3-**	IDE_D6	IDE_D10	**GBE1_MDI3-**	**GBE2_MDI3-**
4	IDE_D3	IDE_D11	**GBE1_MDI3+**	**GBE2_MDI3+**	IDE_D3	IDE_D11	**GBE1_MDI3+**	**GBE2_MDI3+**
5	IDE_D15	IDE_D12	**GBE1_LINK100#**	**GBE2_LINK100#**	IDE_D15	IDE_D12	**GBE1_LINK100#**	**GBE2_LINK100#**
6	IDE_D8	IDE_D4	**GBE1_MDI2-**	**GBE2_MDI2-**	IDE_D8	IDE_D4	**GBE1_MDI2-**	**GBE2_MDI2-**
7	IDE_D9	IDE_D0	**GBE1_MDI2+**	**GBE2_MDI2+**	IDE_D9	IDE_D0	**GBE1_MDI2+**	**GBE2_MDI2+**
8	IDE_D2	IDE_REQ	**GBE1_LINK1000#**	**GBE2_LINK1000#**	IDE_D2	IDE_REQ	**GBE1_LINK1000#**	**GBE2_LINK1000#**
9	IDE_D13	IDE_IOW#	**GBE1_MDI1-**	**GBE2_MDI1-**	IDE_D13	IDE_IOW#	**GBE1_MDI1-**	**GBE2_MDI1-**
10	IDE_D1	IDE_ACK#	**GBE1_MDI1+**	**GBE2_MDI1+**	IDE_D1	IDE_ACK#	**GBE1_MDI1+**	**GBE2_MDI1+**
11	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
12	IDE_D14	IDE_IRQ	**GBE1_MDI0-**	**GBE2_MDI0-**	IDE_D14	IDE_IRQ	**GBE1_MDI0-**	**GBE2_MDI0-**

	TYPE 2 Rev. 2.0		TYPE 3 Rev. 2.0		TYPE 4 Rev. 2.0		TYPE 5 Rev. 2.0	
Pin	Row C	Row D	Row C	Row D	Row C	Row D	Row C	Row D
13	IDE_IORDY	IDE_A0	**GBE1_MDI0+**	**GBE2_MDI0+**	DE_IORDY	DE_A0	**GBE1_MDI0+**	**GBE2_MDI0+**
14	IDE_IOR#	IDE_A1	**GBE1_LINK#**	**GBE2_LINK#**	DE_IOR#	DE_A1	**GBE1_LINK#**	**GBE2_LINK#**
15	PCI_PME#	IDE_A2	PCI_PME#	**GBE2_CTREF**	**RSVD**	DE_A2	**RSVD**	**GBE2_CTREF**
16	PCI_GNT2#	IDE_CS1#	PCI_GNT2#	**RSVD**	**RSVD**	DE_CS1#	**RSVD**	**RSVD**
17	PCI_REQ2#	IDE_CS3#	PCI_REQ2#	**RSVD**	**RSVD**	DE_CS3#	**RSVD**	**RSVD**
18	PCI_GNT1#	IDE_RESET#	PCI_GNT1#	**RSVD**	**RSVD**	DE_RESET#	**RSVD**	**RSVD**
19	PCI_REQ1#	PCI_GNT3#	PCI_REQ1#	PCI_GNT3#	**PCIE_RX6+**	**PCIE_TX6+**	**PCIE_RX6+**	**PCIE_TX6+**
20	PCI_GNT0#	PCI_REQ3#	PCI_GNT0#	PCI_REQ3#	**PCIE_RX6-**	**PCIE_TX6-**	**PCIE_RX6-**	**PCIE_TX6-**
21	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
22	PCI_REQ0#	PCI_AD1	PCI_REQ0#	PCI_AD1	**PCIE_RX7+**	**PCIE_TX7+**	**PCIE_RX7+**	**PCIE_TX7+**
23	PCI_RESET#	PCI_AD3	PCI_RESET#	PCI_AD3	**PCIE_RX7-**	**PCIE_TX7-**	**PCIE_RX7-**	**PCIE_TX7-**
24	PCI_AD0	PCI_AD5	PCI_AD0	PCI_AD5	**RSVD**	**RSVD**	**RSVD**	**RSVD**
25	PCI_AD2	PCI_AD7	PCI_AD2	PCI_AD7	**RSVD**	**RSVD**	**RSVD**	**RSVD**
26	PCI_AD4	PCI_C/BE0#	PCI_AD4	PCI_C/BE0#	**PCIE_RX8+**	**PCIE_TX8+**	**PCIE_RX8+**	**PCIE_TX8+**
27	PCI_AD6	PCI_AD9	PCI_AD6	PCI_AD9	**PCIE_RX8-**	**PCIE_TX8-**	**PCIE_RX8-**	**PCIE_TX8-**
28	PCI_AD8	PCI_AD11	PCI_AD8	PCI_AD11	**RSVD**	**RSVD**	**RSVD**	**RSVD**
29	PCI_AD10	PCI_AD13	PCI_AD10	PCI_AD13	**PCIE_RX9+**	**PCIE_TX9+**	**PCIE_RX9+**	**PCIE_TX9+**
30	PCI_AD12	PCI_AD15	PCI_AD12	PCI_AD15	**PCIE_RX9-**	**PCIE_TX9-**	**PCIE_RX9-**	**PCIE_TX9-**
31	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
32	PCI_AD14	PCI_PAR	PCI_AD14	PCI_PAR	**PCIE_RX10+**	**PCIE_TX10+**	**PCIE_RX10+**	**PCIE_TX10+**
33	PCI_C/BE1#	PCI_SERR#	PCI_C/BE1#	PCI_SERR#	**PCIE_RX10-**	**PCIE_TX10-**	**PCIE_RX10-**	**PCIE_TX10-**
34	PCI_PERR#	PCI_STOP#	PCI_PERR#	PCI_STOP#	**RSVD**	**RSVD**	**RSVD**	**RSVD**
35	PCI_LOCK#	PCI_TRDY#	PCI_LOCK#	PCI_TRDY#	**RSVD**	**RSVD**	**RSVD**	**RSVD**
36	PCI_DEVSEL#	PCI_FRAME#	PCI_DEVSEL#	PCI_FRAME#	**PCIE_RX11+**	**PCIE_TX11+**	**PCIE_RX11+**	**PCIE_TX11+**
37	PCI_IRDY#	PCI_AD16	PCI_IRDY#	PCI_AD16	**PCIE_RX11-**	**PCIE_TX11-**	**PCIE_RX11-**	**PCIE_TX11-**
38	PCI_C/BE2#	PCI_AD18	PCI_C/BE2#	PCI_AD18	**RSVD**	**RSVD**	**RSVD**	**RSVD**
39	PCI_AD17	PCI_AD20	PCI_AD17	PCI_AD20	**PCIE_RX12+**	**PCIE_TX12+**	**PCIE_RX12+**	**PCIE_TX12+**
40	PCI_AD19	PCI_AD22	PCI_AD19	PCI_AD22	**PCIE_RX12-**	**PCIE_TX12-**	**PCIE_RX12-**	**PCIE_TX12-**
41	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
42	PCI_AD21	PCI_AD24	PCI_AD21	PCI_AD24	**PCIE_RX13+**	**PCIE_TX13+**	**PCIE_RX13+**	**PCIE_TX13+**
43	PCI_AD23	PCI_AD26	PCI_AD23	PCI_AD26	**PCIE_RX13-**	**PCIE_TX13-**	**PCIE_RX13-**	**PCIE_TX13-**
44	PCI_C/BE3#	PCI_AD28	PCI_C/BE3#	PCI_AD28	**RSVD**	**RSVD**	**RSVD**	**RSVD**
45	PCI_AD25	PCI_AD30	PCI_AD25	PCI_AD30	**RSVD**	**RSVD**	**RSVD**	**RSVD**
46	PCI_AD27	PCI_IRQC#	PCI_AD27	PCI_IRQC#	**PCIE_RX14+**	**PCIE_TX14+**	**PCIE_RX14+**	**PCIE_TX14+**
47	PCI_AD29	PCI_IRQD#	PCI_AD29	PCI_IRQD#	**PCIE_RX14-**	**PCIE_TX14-**	**PCIE_RX14-**	**PCIE_TX14-**
48	PCI_AD31	PCI_CLKRUN#	PCI_AD31	PCI_CLKRUN#	**RSVD**	**RSVD**	**RSVD**	**RSVD**
49	PCI_IRQA#	PCI_M66EN	PCI_IRQA#	PCI_M66EN	**PCIE_RX15+**	**PCIE_TX15+**	**PCIE_RX15+**	**PCIE_TX15+**
50	PCI_IRQB#	PCI_CLK	PCI_IRQB#	PCI_CLK	**PCIE_RX15-**	**PCIE_TX15-**	**PCIE_RX15-**	**PCIE_TX15-**
51	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
52	PEG_RX0+	PEG_TX0+	PEG_RX0+	PEG_TX0+	**PCIE_RX16+**	**PCIE_TX16+**	**PCIE_RX16+**	**PCIE_TX16+**
53	PEG_RX0-	PEG_TX0-	PEG_RX0-	PEG_TX0-	**PCIE_RX16-**	**PCIE_TX16-**	**PCIE_RX16-**	**PCIE_TX16-**
54	TYPE0#	PEG_LANE_RV#	TYPE0#	PEG_LANE_RV#	TYPE0#	PEG_LANE_RV#	TYPE0#	PEG_LANE_RV#
55	PEG_RX1+	PEG_TX1+	PEG_RX1+	PEG_TX1+	**PCIE_RX17+**	**PCIE_TX17+**	**PCIE_RX17+**	**PCIE_TX17+**
56	PEG_RX1-	PEG_TX1-	PEG_RX1-	PEG_TX1-	**PCIE_RX17-**	**PCIE_TX17-**	**PCIE_RX17-**	**PCIE_TX17-**
57	TYPE1#	TYPE2#	TYPE1#	TYPE2#	TYPE1#	TYPE2#	TYPE1#	TYPE2#

	TYPE 2 Rev. 2.0		TYPE 3 Rev. 2.0		TYPE 4 Rev. 2.0		TYPE 5 Rev. 2.0	
Pin	Row C	Row D	Row C	Row D	Row C	Row D	Row C	Row D
58	PEG_RX2+	PEG_TX2+	PEG_RX2+	PEG_TX2+	**PCIE_RX18+**	**PCIE_TX18+**	**PCIE_RX18+**	**PCIE_TX18+**
59	PEG_RX2-	PEG_TX2-	PEG_RX2-	PEG_TX2-	**PCIE_RX18-**	**PCIE_TX18-**	**PCIE_RX18-**	**PCIE_TX18-**
60	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
61	PEG_RX3+	PEG_TX3+	PEG_RX3+	PEG_TX3+	**PCIE_RX19+**	**PCIE_TX19+**	**PCIE_RX19+**	**PCIE_TX19+**
62	PEG_RX3-	PEG_TX3-	PEG_RX3-	PEG_TX3-	**PCIE_RX19-**	**PCIE_TX19-**	**PCIE_RX19-**	**PCIE_TX19-**
63	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
64	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
65	PEG_RX4+	PEG_TX4+	PEG_RX4+	PEG_TX4+	**PCIE_RX20+**	**PCIE_TX20+**	**PCIE_RX20+**	**PCIE_TX20+**
66	PEG_RX4-	PEG_TX4-	PEG_RX4-	PEG_TX4-	**PCIE_RX20-**	**PCIE_TX20-**	**PCIE_RX20-**	**PCIE_TX20-**
67	RSVD	GND	RSVD	GND	RSVD	GND	RSVD	GND
68	PEG_RX5+	PEG_TX5+	PEG_RX5+	PEG_TX5+	**PCIE_RX21+**	**PCIE_TX21+**	**PCIE_RX21+**	**PCIE_TX21+**
69	PEG_RX5-	PEG_TX5-	PEG_RX5-	PEG_TX5-	**PCIE_RX21-**	**PCIE_TX21-**	**PCIE_RX21-**	**PCIE_TX21-**
70	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
71	PEG_RX6+	PEG_TX6+	PEG_RX6+	PEG_TX6+	**PCIE_RX22+**	**PCIE_TX22+**	**PCIE_RX22+**	**PCIE_TX22+**
72	PEG_RX6-	PEG_TX6-	PEG_RX6-	PEG_TX6-	**PCIE_RX22-**	**PCIE_TX22-**	**PCIE_RX22-**	**PCIE_TX22-**
73	SDVO_DATA	SDVO_CLK	SDVO_DATA	SDVO_CLK	SDVO_DATA	SDVO_CLK	SDVO_DATA	SDVO_CLK
74	PEG_RX7+	PEG_TX7+	PEG_RX7+	PEG_TX7+	**PCIE_RX23+**	**PCIE_TX23+**	**PCIE_RX23+**	**PCIE_TX23+**
75	PEG_RX7-	PEG_TX7-	PEG_RX7-	PEG_TX7-	**PCIE_RX23-**	**PCIE_TX23-**	**PCIE_RX23-**	**PCIE_TX23-**
76	GND	GND	GND	GND	GND	GND	GND	GND
77	RSVD	IDE_CBLID#	FRSVD	**RSVD**	RSVD	IDE_CBLID#	RSVD	**RSVD**
78	PEG_RX8+	PEG_TX8+	PEG_RX8+	PEG_TX8+	**PCIE_RX24+**	**PCIE_TX24+**	**PCIE_RX24+**	**PCIE_TX24+**
79	PEG_RX8-	PEG_TX8-	PEG_RX8-	PEG_TX8-	**PCIE_RX24-**	**PCIE_TX24-**	**PCIE_RX24-**	**PCIE_TX24-**
80	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
81	PEG_RX9+	PEG_TX9+	PEG_RX9+	PEG_TX9+	**PCIE_RX25+**	**PCIE_TX25+**	**PCIE_RX25+**	**PCIE_TX25+**
82	PEG_RX9-	PEG_TX9-	PEG_RX9-	PEG_TX9-	**PCIE_RX25-**	**PCIE_TX25-**	**PCIE_RX25-**	**PCIE_TX25-**
83	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
84	GND	GND	GND	GND	GND	GND	GND	GND
85	PEG_RX10+	PEG_TX10+	PEG_RX10+	PEG_TX10+	**PCIE_RX26+**	**PCIE_TX26+**	**PCIE_RX26+**	**PCIE_TX26+**
86	PEG_RX10-	PEG_TX10-	PEG_RX10-	PEG_TX10-	**PCIE_RX26-**	**PCIE_TX26-**	**PCIE_RX26-**	**PCIE_TX26-**
87	GND	GND	GND	GND	GND	GND	GND	GND
88	PEG_RX11+	PEG_TX11+	PEG_RX11+	PEG_TX11+	**PCIE_RX27+**	**PCIE_TX27+**	**PCIE_RX27+**	**PCIE_TX27+**
89	PEG_RX11-	PEG_TX11-	PEG_RX11-	PEG_TX11-	**PCIE_RX27-**	**PCIE_TX27-**	**PCIE_RX27-**	**PCIE_TX27-**
90	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
91	PEG_RX12+	PEG_TX12+	PEG_RX12+	PEG_TX12+	**PCIE_RX28+**	**PCIE_TX28+**	**PCIE_RX28+**	**PCIE_TX28+**
92	PEG_RX12-	PEG_TX12-	PEG_RX12-	PEG_TX12-	**PCIE_RX28-**	**PCIE_TX28-**	**PCIE_RX28-**	**PCIE_TX28-**
93	GND	GND	GND	GND	GND	GND	GND	GND
94	PEG_RX13+	PEG_TX13+	PEG_RX13+	PEG_TX13+	**PCIE_RX29+**	**PCIE_TX29+**	**PCIE_RX29+**	**PCIE_TX29+**
95	PEG_RX13-	PEG_TX13-	PEG_RX13-	PEG_TX13-	**PCIE_RX29-**	**PCIE_TX29-**	**PCIE_RX29-**	**PCIE_TX29-**
96	GND	GND	GND	GND	GND	GND	GND	GND
97	RSVD	PEG_ENABLE#	RSVD	PEG_ENABLE#	RSVD	PEG_ENABLE#	RSVD	PEG_ENABLE#
98	PEG_RX14+	PEG_TX14+	PEG_RX14+	PEG_TX14+	**PCIE_RX30+**	**PCIE_TX30+**	**PCIE_RX30+**	**PCIE_TX30+**
99	PEG_RX14-	PEG_TX14-	PEG_RX14-	PEG_TX14-	**PCIE_RX30-**	**PCIE_TX30-**	**PCIE_RX30-**	**PCIE_TX30-**
100	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
101	PEG_RX15+	PEG_TX15+	PEG_RX15+	PEG_TX15+	**PCIE_RX31+**	**PCIE_TX31+**	**PCIE_RX31+**	**PCIE_TX31+**
102	PEG_RX15-	PEG_TX15-	PEG_RX15-	PEG_TX15-	**PCIE_RX31-**	**PCIE_TX31-**	**PCIE_RX31-**	**PCIE_TX31-**

	TYPE 2 Rev. 2.0		TYPE 3 Rev. 2.0		TYPE 4 Rev. 2.0		TYPE 5 Rev. 2.0	
Pin	**Row C**	**Row D**	**Row C**	**Row D**	**Row C**	**Row D**	**Row C**	**Row D**
103	GND	GND	GND	GND	GND	GND	GND	GND
104	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
109	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V	VCC_12V
110	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)