# Computer Architecture - Assignment 6

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## 1 Introduction

This assignment presents the implementation and analysis of a cache simulation system. The simulation includes the implementation of a `CacheLine` and a `Cache` object. Furthermore, the `InstructionFetch` and `MemoryAccess` stages of the simulation utilize instances of the Cache object, referred to as `L1iCache` and `L1dCache` respectively. The cache data lines are accessed via discrete event simulation, with varying latencies for different sizes of cache.

## 2 Cache Implementation

The cache simulation system comprises two key components: `CacheLine` and `Cache`.

### 2.1 CacheLine

The `CacheLine` represents a single line in the cache memory. It contains the necessary data fields such as `int lineSize`, `int nWords`, `int tag`, `boolean modifiedBit`, `int[] dataLine`, `int time`,. Each `CacheLine` object is designed to store a portion of the cached memory block.

### 2.2 Cache

The `Cache` object represents the entire cache memory. It consists of multiple `CacheLine` objects organized in an array. The cache type implemented is a fully associative cache with an LRU replacement policy.

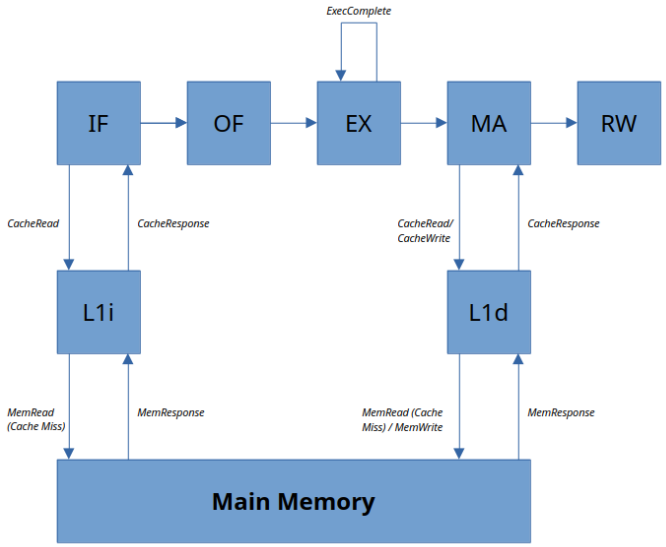


Figure 1: Working of Cache Model

# 3 Simulation Results

| **Program** | **L1i=16B** | **L1i=128B** | **L1i=512B** | **L1i=1KiB** |
|---|---|---|---|---|
| | **Latency=1** | **Latency=2** | **Latency=3** | **Latency=4** |
| descending.asm | 15038 | 4233 | 4371 | 4612 |
| palindrome.asm | 2300 | 874 | 894 | 932 |
| prime.asm | 1358 | 638 | 659 | 690 |
| fibonacci.asm | 3858 | 1717 | 1761 | 1834 |
| evenodd.asm | 258 | 263 | 268 | 273 |

Table 1: Statistics for test cases for L1i cache

| **Program** | **L1d=16B** | **L1d=128B** | **L1d=512B** | **L1d=1KiB** |
|---|---|---|---|---|
| | **Latency=1** | **Latency=2** | **Latency=3** | **Latency=4** |
| descending.asm | 5215 | 4438 | 4525 | 4612 |
| palindrome.asm | 932 | 932 | 932 | 932 |
| prime.asm | 690 | 690 | 690 | 690 |
| fibonacci.asm | 1813 | 1820 | 1827 | 1834 |
| evenodd.asm | 270 | 271 | 272 | 273 |

Table 2: Statistics for test cases for L1d cache

# 4 Performance Graphs

The performance graphs for each program illustrate the relationship between cache size, latency, and IPC.

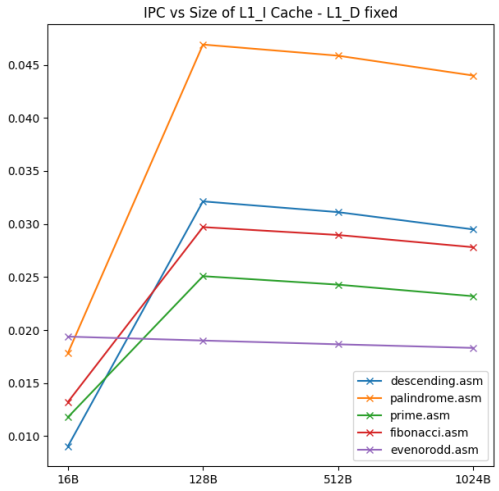


Figure 2: Statistics for varying size of L1i Cache - Size of L1d fixed at 1024B

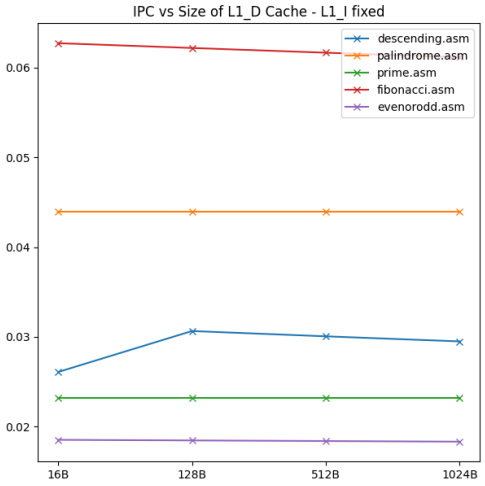


Figure 3: Statistics for varying size of L1d Cache - Size of L1i fixed at 1024B

# 5 Conclusion

The cache simulation system presented in this report demonstrates the effectiveness of cache memory in improving system performance.