Lab-5 Report

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1 Introduction

We use the previously upgraded pipelined model to build a discretized event model.In this model we have a priority queue of events based on the event time which gives us the time at which the operation can occur by also including latencies introduced by memory accesses and ALU latency. The latencies considered in our model are: MainMemory=40 cycles , default ALU latency=1,Multiplier Latency=4,Divider Latency =10. This introduces the situation where a certain unit is taking more than one cycle to get the result from memory or the ALU.This is reflected in the table below where the instructions are more or less the same,but the cycles have hugely differed due to the stalls induced to access and calculation.

AssemblyProgram	**#Instructions**	**#Cycles**	**#Instruction Per Cycle(IPC)**
descending.asm	305	15301	0.019933
evenorodd.asm	5	250	0.02
prime.asm	25	1182	0.0211
fibonacci.asm	96	4369	0.02197
palindrome.asm	42	2109	0.01991465

Table 1: Statistics for test cases