CMOS D Flip Flop   dflipflop
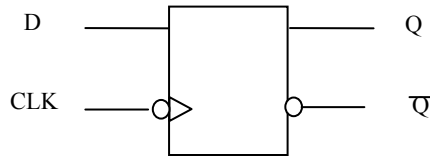
D ————□———— Q

CLK ————▷———□———— Q̄

Description:
This is an Intrinsic Super Element which models a Master-Slave Negative Edge
Triggered D Flip-flop.

Form: dflipflop:<instance name> *n1 n2 n3 n4 n5 n6*

> *n1* is the high voltage source (Vdd) terminal,
> *n2* is D terminal
> *n3* is Clock terminal,
> *n4* is Q terminal,
> *n5* is Q̄ terminal,
> *n6* is the ground or Vss terminal

Parameters:

Parameter	Type	Default Value	Required
ln: Channel Length of NMOS (m)	TR_DOUBLE	1.0e-6	No
wn: Channel Width of NMOS (m)	TR_DOUBLE	1.0e-6	No
lp: Channel Length of PMOS (m)	TR_DOUBLE	1.0e-6	No
wp: Channel Width of PMOS (m)	TR_DOUBLE	1.0e-6	No

Example:
dflipflop: flop 1 2 3 4 5 0

Notes:
This implementation of D flip-flop is based on CMOS nand gate and inverter. This is
master-slave negative edge triggered flip-flop.
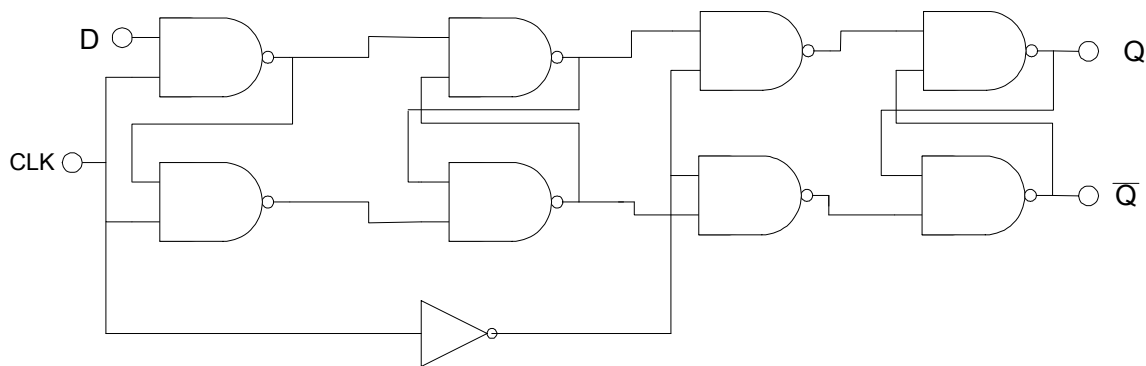

Known Bugs:
No known bugs.

Truth Table

The D flip-flop is based on following truth table:

CLK	D	Q	$\overline{Q}$	Operation
↓	1	1	0	Set
↓	0	0	1	Reset
↑	1	Hold	Hold	Hold Previous Value
↑	0	Hold	Hold	Hold Previous Value

Schematic

Following is the schematic of D Flip Flop

Sample Netlist:
*CMOS Master Slave Negative Edge Triggered D FLIP FLOP
* This netlist is for Transient analysis of D Flip Flop *
.tran2 tstop=12e-6 tstep=1e-9
*********** D and CLK inputs *************
vpulse:Vin2 2 0 v1=0 v2=5 td=0e-6 per=4e-6 pw=2e-6 tr=0.002e-6 tf=0.002e-6
vpulse:Vin3 3 0 v1=5 v2=0 td=0e-6 per=2e-6 pw=1e-6 tr=0.002e-6 tf=0.002e-6
***** Vdd Connection *****
vsource:Vdd 1 0 vdc=5
******* Instantiation************
dflipflop:flop 1 2 3 4 5 0
***********Load Resistances*******
r:R1 4 0 r=1000000
r:R2 5 0 r=1000000
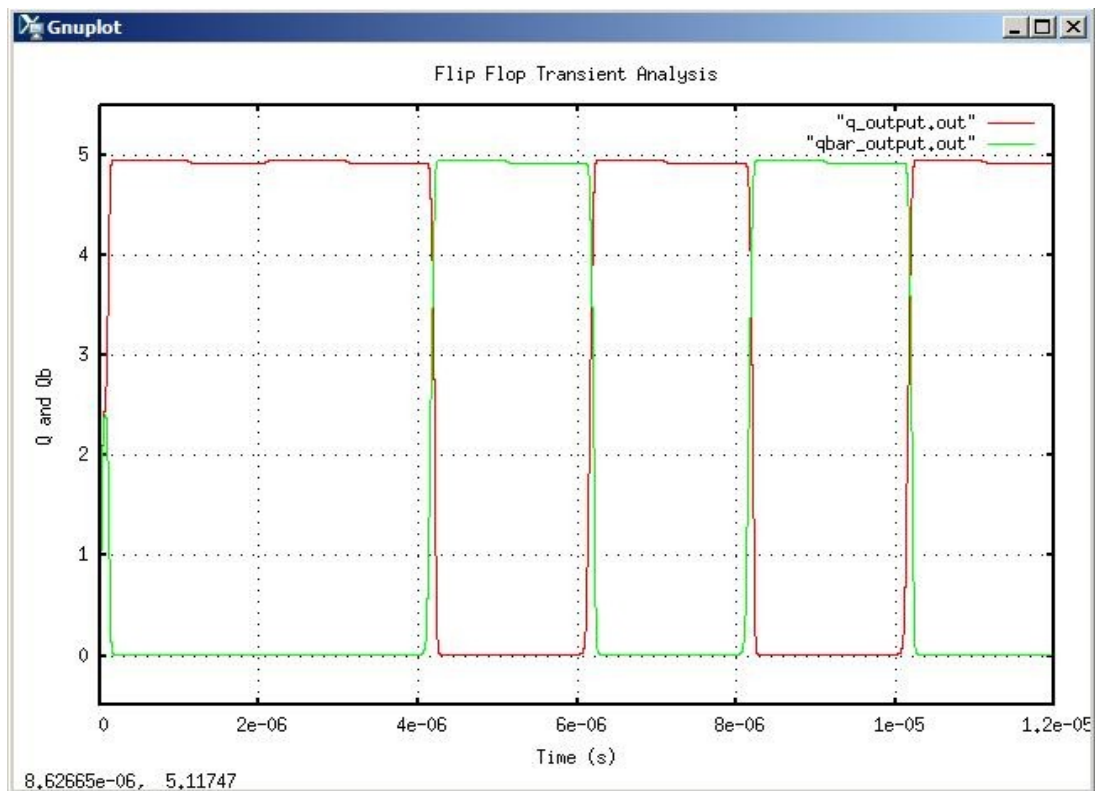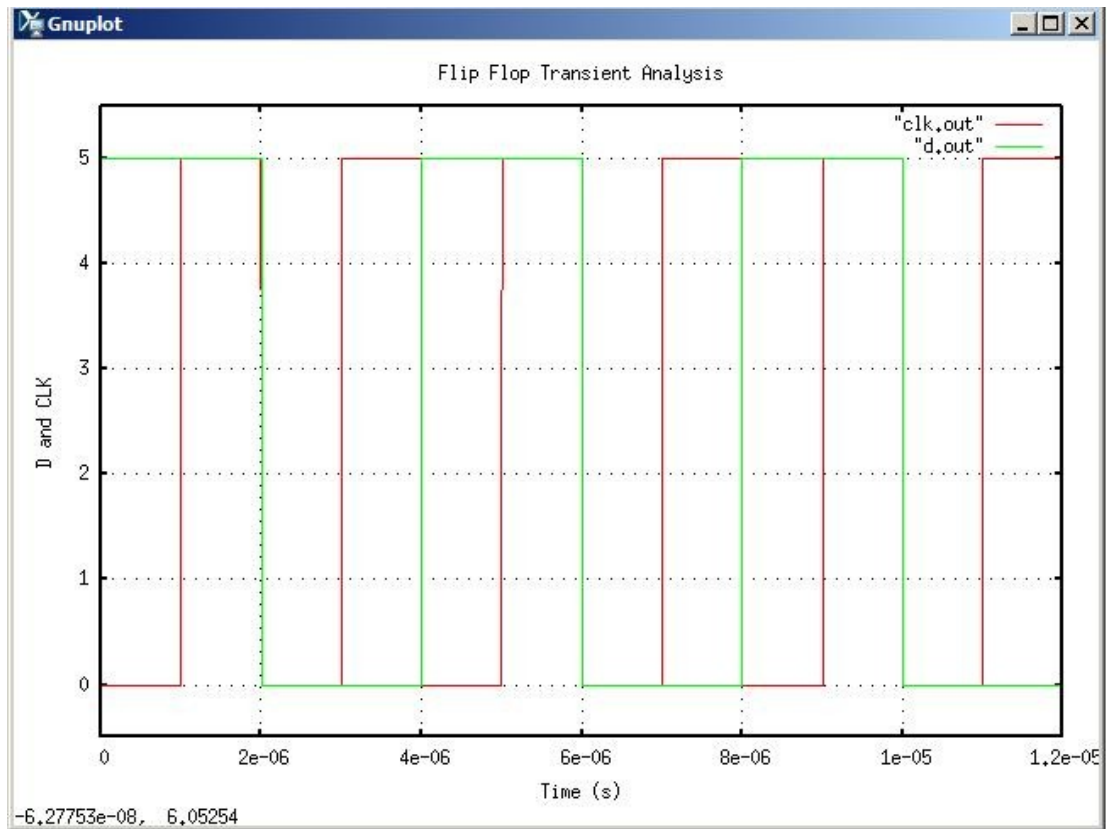*** Plot ******
.options gnuplot
.out plot term 2 vt in "d.out"
.out plot term 3 vt in "clk.out"
.out plot term 4 vt in "Q_output.out"

.out plot term 5 vt in "Qbar_output.out"
.end

Validation:

The output graph from the above netlist is shown below:

Credits:

Name	Affiliation	Date	Links
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