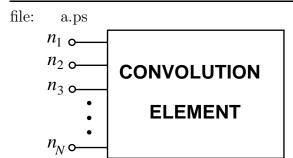
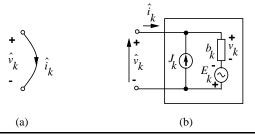
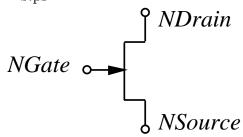
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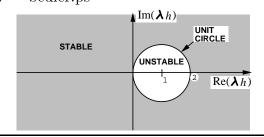
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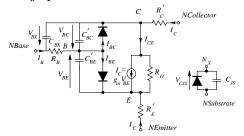
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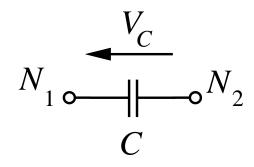
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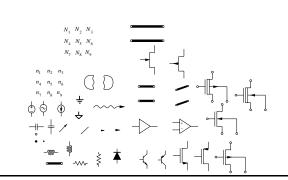
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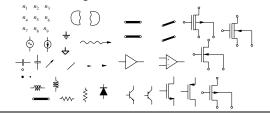
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file: circuit.ps



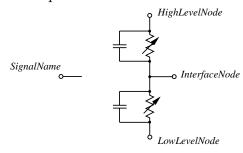
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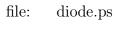


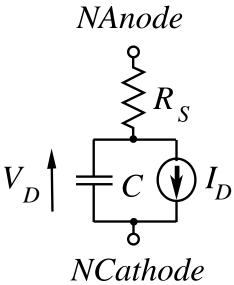
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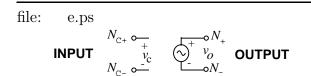


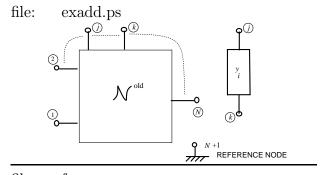
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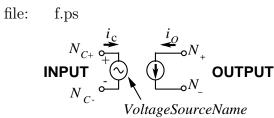


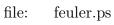


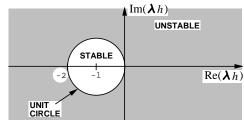


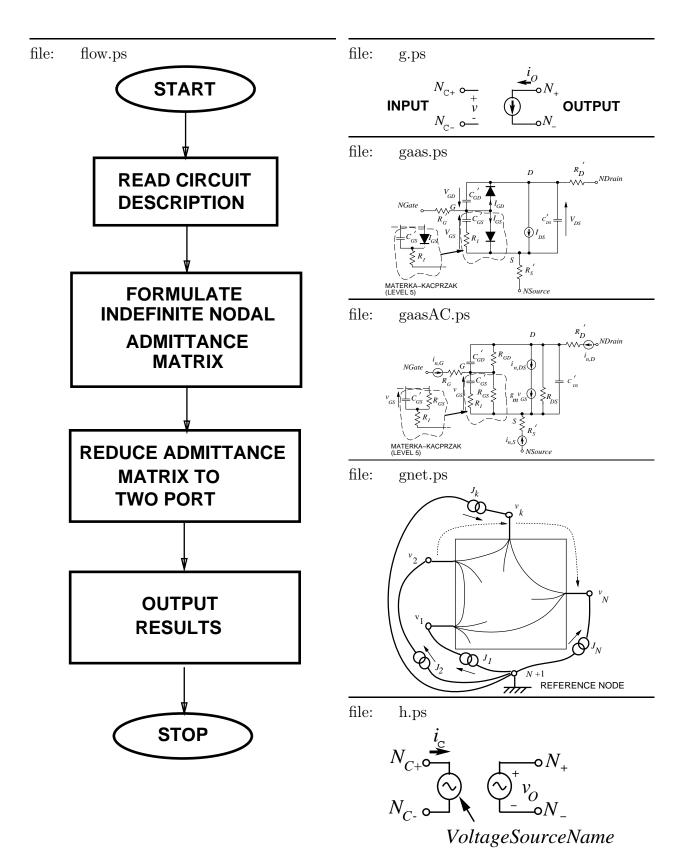




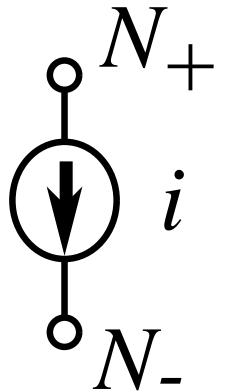




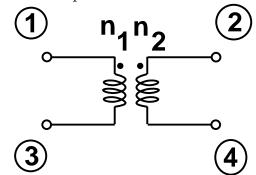




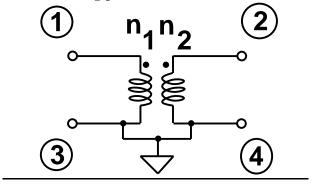




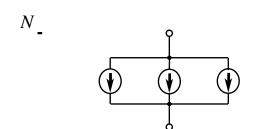
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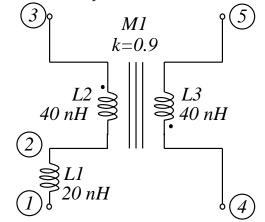
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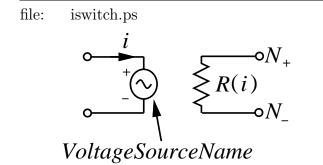


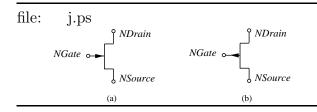
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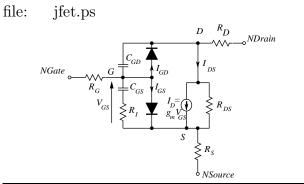


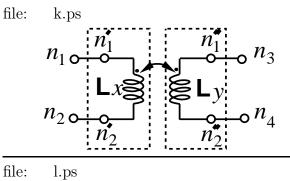
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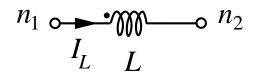


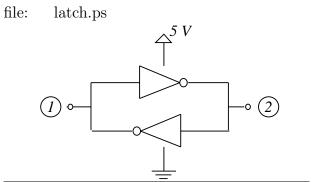


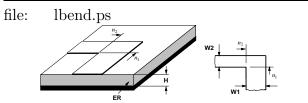


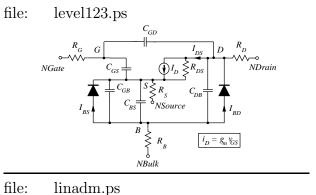


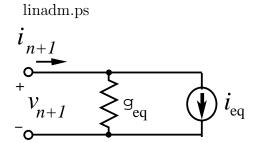


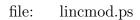


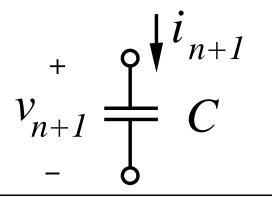




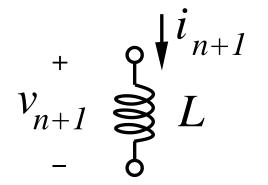




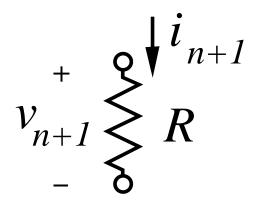




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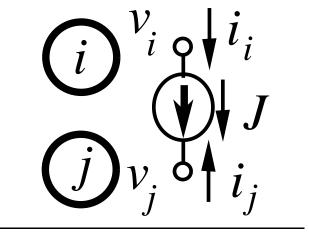


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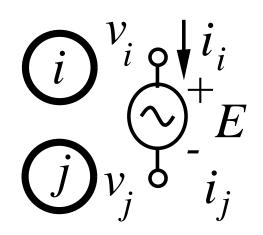


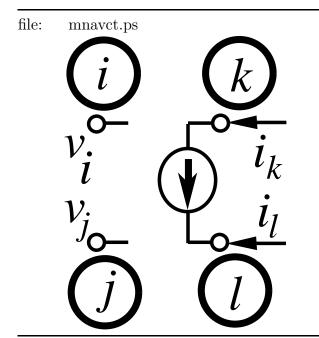
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file: mnai.ps

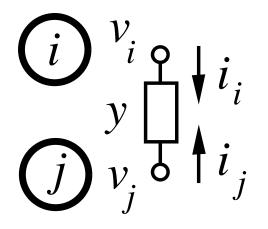


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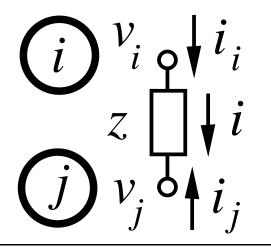


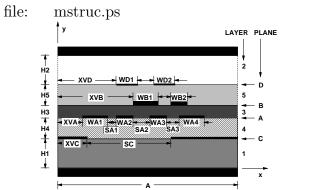


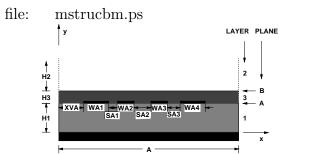
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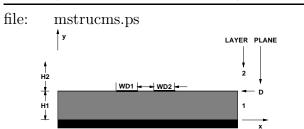


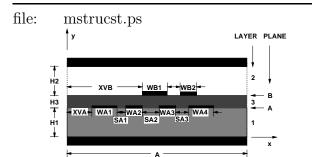
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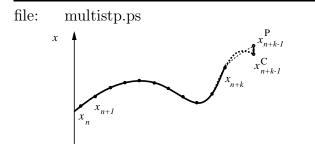


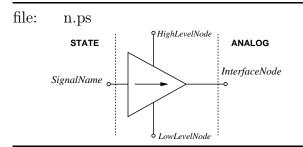


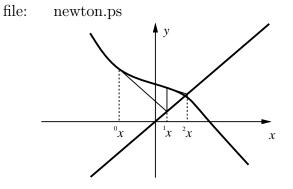




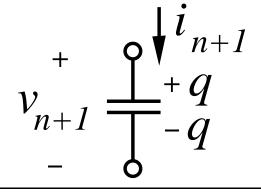




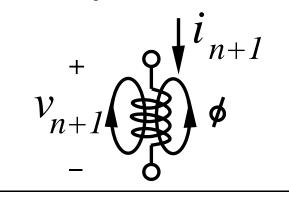




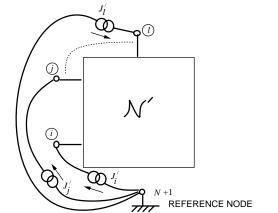
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file: nllmod.ps



file: np.ps

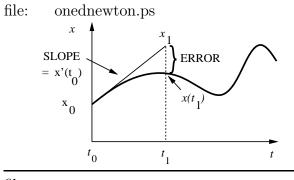


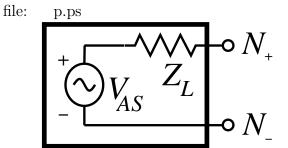
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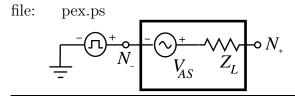
ANALOG
Interface Node

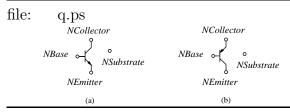
ReferenceNode

SignalName



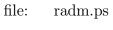


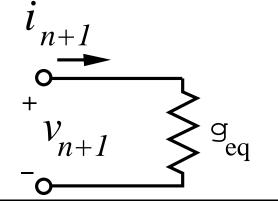




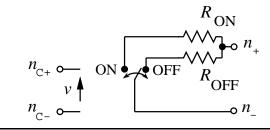
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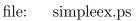


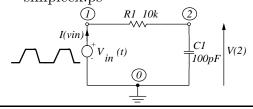




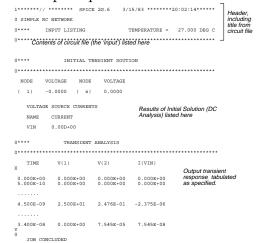
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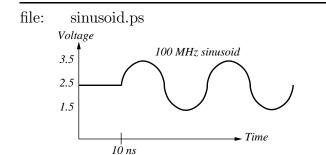


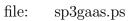


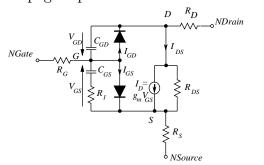


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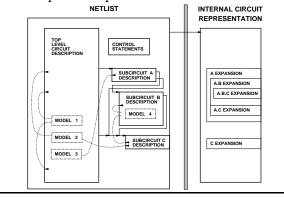




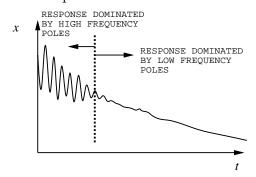




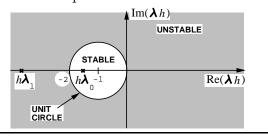
 $\begin{tabular}{ll} file: & spcircuit.ps \\ & & \\ &$ 



file: stiffa.ps

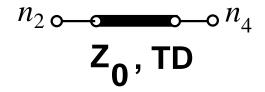


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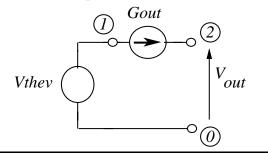


file: t.ps





file: thevnlin.ps



file: timec.ps

