*Description:*

This is an Intrinsic Super Element which models a CMOS inverter utilizing the EKV 2.6 model.

*Form:* cmosinv:<instance name> *n1 n2 n3 n4* <parameter list>

*n1* is the high voltage source (Vdd) terminal,  
*n2* is the input terminal,  
*n3* is the output terminal,  
*n4* is the ground or Vss terminal.

*Parameters:*

Parameter	Type	Default Value	Required
ln: Channel Length of NMOS (m)	TR_DOUBLE	1.0e-6	No
wn: Channel Width of NMOS (m)	TR_DOUBLE	1.0e-6	No
lp: Channel Length of PMOS (m)	TR_DOUBLE	1.0e-6	No
wp: Channel Width of PMOS (m)	TR_DOUBLE	1.0e-6	No
np_n: Parallel multiple device number of NMOS	TR_DOUBLE	1.0	No
np_p: Parallel multiple device number of PMOS	TR_DOUBLE	1.0	No
ns_n: Serial multiple device number of NMOS	TR_DOUBLE	1.0	No
ns_p: Serial multiple device number of PMOS	TR_DOUBLE	1.0	No
cox_n: Gate oxide capacitance per area of NMOS (F/m <sup>2</sup> )	TR_DOUBLE	0.0	No
cox_p: Gate oxide capacitance per area of PMOS (F/m <sup>2</sup> )	TR_DOUBLE	0.0	No
xj_n: Junction depth of NMOS (m)	TR_DOUBLE	1.0e-7	No
xj_p: Junction depth of PMOS (m)	TR_DOUBLE	1.0e-7	No
dw_n: Channel width correction of NMOS (m)	TR_DOUBLE	0.0	No
dw_p: Channel width correction of PMOS (m)	TR_DOUBLE	0.0	No
dl_n: Channel length correction of NMOS (m)	TR_DOUBLE	0.0	No
dl_p: Channel length correction of PMOS (m)	TR_DOUBLE	0.0	No
vto_n: Long_channel threshold voltage of NMOS (V)	TR_DOUBLE	0.0	No
vto_p: Long_channel threshold voltage of PMOS (V)	TR_DOUBLE	0.0	No
gamma_n: Body effect parameter of NMOS (V <sup>1/2</sup> )	TR_DOUBLE	0.0	No
gamma_p: Body effect parameter of PMOS (V <sup>1/2</sup> )	TR_DOUBLE	0.0	No
phi_n: Bulk Fermi potential of NMOS (V)	TR_DOUBLE	0.0	No
phi_p: Bulk Fermi potential of PMOS (V)	TR_DOUBLE	0.0	No
kp_n: Transconductance parameter of NMOS (A/V <sup>2</sup> )	TR_DOUBLE	0.0	No
kp_p: Transconductance parameter of PMOS (A/V <sup>2</sup> )	TR_DOUBLE	0.0	No
eo_n: Mobility reduction coefficient of NMOS (V/m)	TR_DOUBLE	0.0	No

eo_p: Mobility reduction coefficient of PMOS (V/m)	TR_DOUBLE	0.0	No
ucrit_n: Longitudinal critical field of NMOS (V/m)	TR_DOUBLE	0.0	No
ucrit_p: Longitudinal critical field of PMOS (V/m)	TR_DOUBLE	0.0	No
tox_n: Oxide thickness of NMOS (m)	TR_DOUBLE	0.0	No
tox_p: Oxide thickness of PMOS (m)	TR_DOUBLE	0.0	No
nsub: Channel doping of NMOS (1/cm <sup>3</sup> )	TR_DOUBLE	0.0	No
psub: Channel doping of PMOS (1/cm <sup>3</sup> )	TR_DOUBLE	0.0	No
vfb_n: Flat-band voltage of NMOS (V)	TR_DOUBLE	-2003.0	No
vfb_p: Flat-band voltage of PMOS (V)	TR_DOUBLE	-2003.0	No
uo_n: Low-field mobility of NMOS(cm <sup>2</sup> /(V.s))	TR_DOUBLE	500	No
uo_p: Low-field mobility of PMOS(cm <sup>2</sup> /(V.s))	TR_DOUBLE	200	No
vmax_n: Saturation velocity of NMOS (m/s)	TR_DOUBLE	0.0	No
vmax_p: Saturation velocity of PMOS (m/s)	TR_DOUBLE	0.0	No
lambda_n: Channel-length modulation of NMOS	TR_DOUBLE	0.5	No
lambda_p: Channel-length modulation of PMOS	TR_DOUBLE	0.5	No
weta_n: Narrow-channel effect coefficient of NMOS	TR_DOUBLE	0.25	No
weta_p: Narrow-channel effect coefficient of PMOS	TR_DOUBLE	0.25	No
leta_n: Short-channel effect coefficient of NMOS	TR_DOUBLE	0.1	No
leta_p: Short-channel effect coefficient of PMOS	TR_DOUBLE	0.1	No
qo_n: Reverse short channel effect peak charge density of NMOS (A.s/m <sup>2</sup> )	TR_DOUBLE	0.0	No
qo_p: Reverse short channel effect peak charge density of PMOS (A.s/m <sup>2</sup> )	TR_DOUBLE	0.0	No
lk_n: Reverse short channel effect characteristic length of NMOS (m)	TR_DOUBLE	2.9e-7	No
lk_p: Reverse short channel effect characteristic length of PMOS (m)	TR_DOUBLE	2.9e-7	No
iba_n: First impact ionization coefficient of NMOS (1/m)	TR_DOUBLE	0.0	No
iba_p: First impact ionization coefficient of PMOS (1/m)	TR_DOUBLE	0.0	No
ibb_n: Second impact ionization coefficient of NMOS (V/m)	TR_DOUBLE	3.0e8	No
ibb_p: Second impact ionization coefficient of PMOS (V/m)	TR_DOUBLE	3.0e8	No
ibn_n: Saturation voltage factor for impact ionization of NMOS	TR_DOUBLE	1.0	No
ibn_p: Saturation voltage factor for impact ionization of PMOS	TR_DOUBLE	1.0	No
tcv_n: Threshold voltage temperature coefficient of NMOS (V/K)	TR_DOUBLE	1.0e-3	No
tcv_p: Threshold voltage temperature coefficient of PMOS (V/K)	TR_DOUBLE	1.0e-3	No
bex_n: Mobility temperature exponent of NMOS	TR_DOUBLE	-1.5	No
bex_p: Mobility temperature exponent of PMOS	TR_DOUBLE	-1.5	No
ucex_n: Longitudinal critical field temperature exponent of NMOS	TR_DOUBLE	0.8	No

ucex_p: Longitudinal critical field temperature exponent of PMOS	TR_DOUBLE	0.8	No
ibbt_n: Temperature coefficient for IBB of NMOS (1/K)	TR_DOUBLE	9.0e-4	No
ibbt_p: Temperature coefficient for IBB of PMOS (1/K)	TR_DOUBLE	9.0e-4	No
avto_n: Area related threshold voltage mismatch parameter of NMOS (Vm)	TR_DOUBLE	0.0	No
avto_p: Area related threshold voltage mismatch parameter of PMOS (Vm)	TR_DOUBLE	0.0	No
akp_n: Area related gain mismatch parameter of NMOS (m)	TR_DOUBLE	0.0	No
akp_p: Area related gain mismatch parameter of PMOS (m)	TR_DOUBLE	0.0	No
agamma_n: Area related body effect mismatch parameter of NMOS ( $V^{(1/2)}m$ )	TR_DOUBLE	0.0	No
agamma_p: Area related body effect mismatch parameter of PMOS ( $V^{(1/2)}m$ )	TR_DOUBLE	0.0	No
scale: Scale parameter	TR_DOUBLE	1.0	No
tnom: Nominal temperature of model parameters (K)	TR_DOUBLE	300.15	No
tmp: Model simulation temperature (K)	TR_DOUBLE	300.15	No

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*Example:*

cmosinv:inverter 1 2 3 0

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*Notes:*

This implementation of cmos inverter is based on EKV 2.6 [1] mosfet model.

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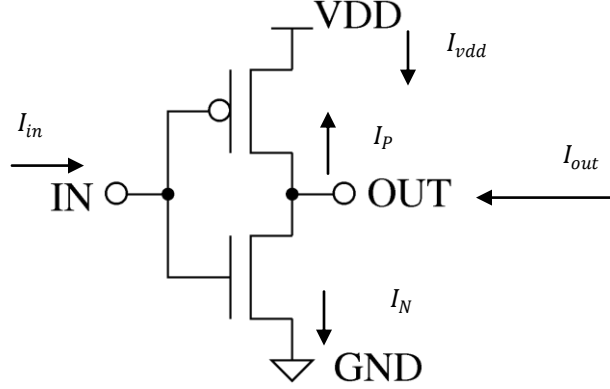
*Known Bugs:*

No known bugs.

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### Implementation Details:

This element is implemented as a fREEDA **Intrinsic Super Element** based on EKV 2.6 MOSFET model [1]. The element has **3 state variables**: Input Voltage (VIN), Output Voltage (VOUT) and Power Supply Voltage (VDD). Following is the schematic of Inverter:



If it would have been implemented as **Extrinsic Super Element**, then there would have been **6 state variables** (3 corresponding to each transistor). Intrinsic implementation has reduced the state variables by factor of two which will lead to faster run time of simulation.

State Variables of Intrinsic Super Element:

$$x[0] = VDD \quad x[1] = VIN \quad x[2] = VOUT$$

State variables of EKV PMOS and NMOS have been represented in terms of these variables. This is charged based model. The current entering in each terminal is sum of corresponding AC and DC current.

$$I_{in} = \frac{dQ_{in}}{dt} \quad \text{--- (1)}$$

In equation (1),  $Q_{in}$  indicates charge at gate. The derivative of this charge will give AC current entering in gate. DC current entering in gate is zero.

$$I_{out} = I_N + I_P + \frac{dQ_{out}}{dt} \quad \text{--- (2)}$$

$I_N$  and  $I_P$  is DC current through nmos and pmos.  $Q_{out}$  is charge stored at output node.

$$I_{vdd} = -I_P + \frac{dQ_{VDD}}{dt} \quad \text{--- (3)}$$

$I_N, I_P, Q_{in}, Q_{out}, Q_{VDD}$  are functions of state variables of Intrinsic Super Element.

$$\{I_N, I_P, Q_{in}, Q_{out}, Q_{VDD}\} = f(x[0], x[1], x[2]) \quad \text{--- (4)} \quad [1]$$

## References:

[1] The EKV 2.6 Documentation: [http://legwww.epfl.ch/ekv/pdf/ekv\\_v262.pdf](http://legwww.epfl.ch/ekv/pdf/ekv_v262.pdf)

## Sample Netlist:

- **DC Analysis**

The following netlist plots the output voltage of the CMOS Inverter for an input voltage range of 0 ~ 5V.

\* CMOS Inverter DC Analysis

\*\* This netlist is for Cmos Inverter DC Analysis. It is based on EKV 2.6

\*\*MOSFET model

.dc sweep="vsource:Vin" start=0 stop=5 step=0.01

\*\*\* Vdd connection

vsource:Vdd 1 0 vdc=5

\*\*\*\* Input DC source

vsource:Vin 2 0

\*\*\*\*\* Instantiation of Inverter

cmosinv:inv 1 2 3 0

\*\*\*\* Load Resistance

r:Rout 3 0 r=1000000

\* Load Capacitance

c:Cout 3 0 c=1e-12

\*\*\*Plot

.options gnuplot

.out plot term 3 vt in "vout.out"

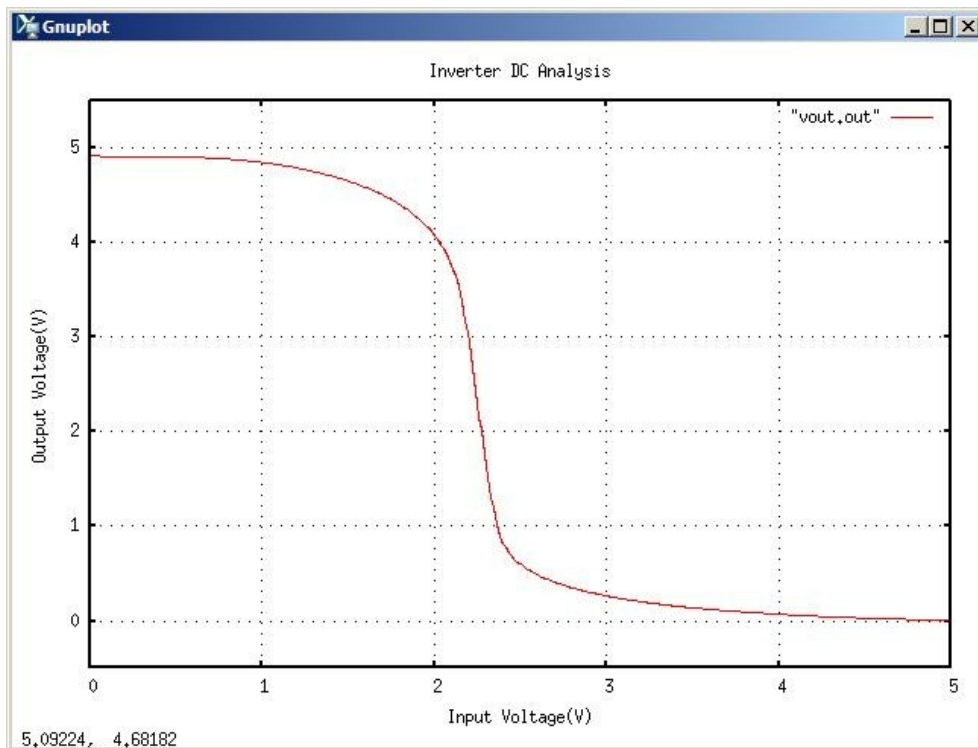
.out plot term 2 vt in "vin.out"

.end

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## Validation:

The output graph from the above netlist is shown below:



- **Transient Analysis**

- \* CMOS Inverter Transient Analysis

- \*This netlist is for Transient Analysis of Cmos Inverter. It is based on EKV

- \*\*MOSFET model.

```
.tran2 tstop=4e-6 tstep=1e-10
```

```
*** Input Pulse
```

```
vpulse:Vin2 22 0 v1=0 v2=5 per=2e-6 pw=1e-6 tr=0.002e-6 tf=0.002e-6
```

```
**** Vdd connection
```

```
vsourc:Vdd 1 0 vdc=5
```

```
*** Instantiation of Inverter
```

```
cmosinv:inv 1 2 3 0
```

```
* Load Resistance
```

```
r:Rout 3 0 r=1000000
```

```
* Load Capacitance
```

```
c:Cout 3 0 c=1e-12
```

```
* Source Resistance
```

```
r:Rsource 22 2 r=10
```

```
* Source Capacitance
```

```
c:Csource 2 0 c=1e-12
```

```
*****Plot
```

```
.options gnuplot
```

```
.out plot term 3 vt in "vout.out"
```

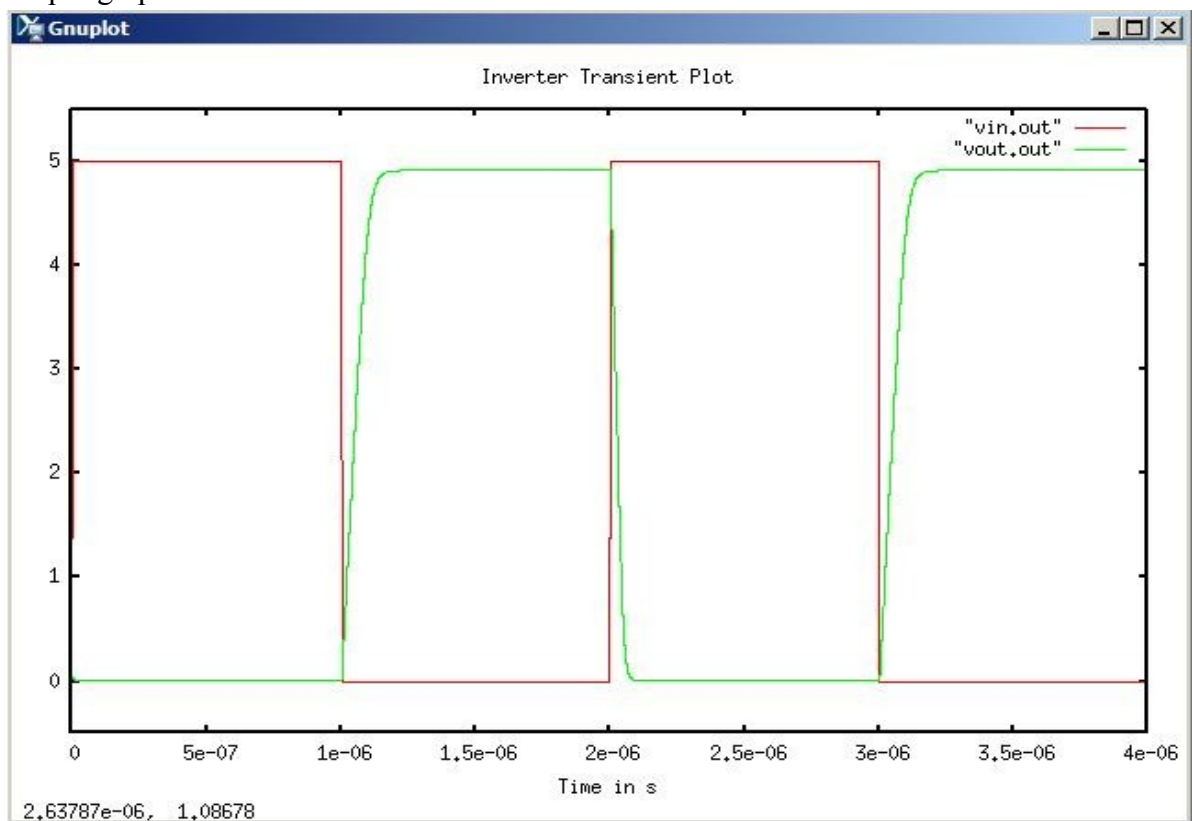
```
.out plot term 22 vt in "vin.out"
```

```
.end
```

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*Validation:*

The output graph from the above netlist is shown below:



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*Version:* 2009.04.27

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*Credits:*

Name	Affiliation	Date	Links
Shivam Priyadarshi <a href="mailto:Shivam.priyadarshi@gmail.com">Shivam.priyadarshi@gmail.com</a>	NCSU	April, 2009	<a href="http://www.ncsu.edu/">http://www.ncsu.edu/</a>
Nikhil Kriplani <a href="mailto:nkriplani@gmail.com">nkriplani@gmail.com</a>	NCSU	April, 2009	<a href="http://www.ncsu.edu/">http://www.ncsu.edu/</a>