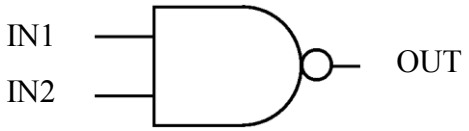
CMOS 2 Input NAND Gate cmos2nand



Description:
This is an Intrinsic Super Element which models a 2 Input CMOS NAND gate utilizing the EKV model.

Form: cmos2nand:<instance name> *n1 n2 n3 n4 n5* <parameter list>

n1 is the high voltage source (Vdd) terminal,
n2 is the first input terminal,
n3 is the second input terminal,
n4 is the output terminal,
n5 is the ground or Vss terminal

Parameters:

Parameter	Type	Default Value	Required
ln: Channel Length of NMOS (m)	TR_DOUBLE	1.0e-6	No
wn: Channel Width of NMOS (m)	TR_DOUBLE	1.0e-6	No
lp: Channel Length of PMOS (m)	TR_DOUBLE	1.0e-6	No
wp: Channel Width of PMOS (m)	TR_DOUBLE	1.0e-6	No
np_n: Parallel multiple device number of NMOS	TR_DOUBLE	1.0	No
np_p: Parallel multiple device number of PMOS	TR_DOUBLE	1.0	No
ns_n: Serial multiple device number of NMOS	TR_DOUBLE	1.0	No
ns_p: Serial multiple device number of PMOS	TR_DOUBLE	1.0	No
cox_n: Gate oxide capacitance per area of NMOS (F/m^2)	TR_DOUBLE	0.0	No
cox_p: Gate oxide capacitance per area of PMOS (F/m^2)	TR_DOUBLE	0.0	No
xj_n: Junction depth of NMOS (m)	TR_DOUBLE	1.0e-7	No
xj_p: Junction depth of PMOS (m)	TR_DOUBLE	1.0e-7	No
dw_n: Channel width correction of NMOS (m)	TR_DOUBLE	0.0	No
dw_p: Channel width correction of PMOS (m)	TR_DOUBLE	0.0	No
dl_n: Channel length correction of NMOS (m)	TR_DOUBLE	0.0	No
dl_p: Channel length correction of PMOS (m)	TR_DOUBLE	0.0	No
vto_n: Long_channel threshold voltage of NMOS (V)	TR_DOUBLE	0.0	No
vto_p: Long_channel threshold voltage of PMOS (V)	TR_DOUBLE	0.0	No
gamma_n: Body effect parameter of NMOS (V^1/2)	TR_DOUBLE	0.0	No
gamma_p: Body effect parameter of PMOS (V^1/2)	TR_DOUBLE	0.0	No
phi_n: Bulk Fermi potential of NMOS (V)	TR_DOUBLE	0.0	No
phi_p: Bulk Fermi potential of PMOS (V)	TR_DOUBLE	0.0	No

kp_n: Transconductance parameter of NMOS (A/V^2)	TR_DOUBLE	0.0	No
kp_p: Transconductance parameter of PMOS (A/V^2)	TR_DOUBLE	0.0	No
eo_n: Mobility reduction coefficient of NMOS (V/m)	TR_DOUBLE	0.0	No
eo_p: Mobility reduction coefficient of PMOS (V/m)	TR_DOUBLE	0.0	No
ucrit_n: Longitudinal critical field of NMOS (V/m)	TR_DOUBLE	0.0	No
ucrit_p: Longitudinal critical field of PMOS (V/m)	TR_DOUBLE	0.0	No
tox_n: Oxide thickness of NMOS (m)	TR_DOUBLE	0.0	No
tox_p: Oxide thickness of PMOS (m)	TR_DOUBLE	0.0	No
nsub: Channel doping of NMOS (1/cm^3)	TR_DOUBLE	0.0	No
psub: Channel doping of PMOS (1/cm^3)	TR_DOUBLE	0.0	No
vfb_n: Flat-band voltage of NMOS (V)	TR_DOUBLE	-2003.0	No
vfb_p: Flat-band voltage of PMOS (V)	TR_DOUBLE	-2003.0	No
uo_n: Low-field mobility of NMOS(cm^2/(V.s))	TR_DOUBLE	500	No
uo_p: Low-field mobility of PMOS(cm^2/(V.s))	TR_DOUBLE	200	No
vmax_n : Saturation velocity of NMOS (m/s)	TR_DOUBLE	0.0	No
vmax_p: Saturation velocity of PMOS (m/s)	TR_DOUBLE	0.0	No
lambda_n: Channel-length modulation of NMOS	TR_DOUBLE	0.5	No
lambda_p: Channel-length modulation of PMOS	TR_DOUBLE	0.5	No
weta_n: Narrow-channel effect coefficient of NMOS	TR_DOUBLE	0.25	No
weta_p: Narrow-channel effect coefficient of PMOS	TR_DOUBLE	0.25	No
leta_n: Short-channel effect coefficient of NMOS	TR_DOUBLE	0.1	No
leta_p: Short-channel effect coefficient of PMOS	TR_DOUBLE	0.1	No
qo_n: Reverse short channel effect peak charge density of NMOS (A.s/m^2)	TR_DOUBLE	0.0	No
qo_p: Reverse short channel effect peak charge density of PMOS (A.s/m^2)	TR_DOUBLE	0.0	No
lk_n: Reverse short channel effect characteristic length of NMOS (m)	TR_DOUBLE	2.9e-7	No
lk_p: Reverse short channel effect characteristic length of PMOS (m)	TR_DOUBLE	2.9e-7	No
iba_n: First impact ionization coefficient of NMOS (1/m)	TR_DOUBLE	0.0	No
iba_p: First impact ionization coefficient of PMOS (1/m)	TR_DOUBLE	0.0	No
ibb_n: Second impact ionization coefficient of NMOS (V/m)	TR_DOUBLE	3.0e8	No
ibb_p: Second impact ionization coefficient of PMOS (V/m)	TR_DOUBLE	3.0e8	No
ibn_n: Saturation voltage factor for impact ionization of NMOS	TR_DOUBLE	1.0	No
ibn_p: Saturation voltage factor for impact ionization of PMOS	TR_DOUBLE	1.0	No
tcv_n: Threshold voltage temperature coefficient of NMOS (V/K)	TR_DOUBLE	1.0e-3	No
tcv_p: Threshold voltage temperature coefficient of PMOS (V/K)	TR_DOUBLE	1.0e-3	No
bex_n: Mobility temperature exponent of NMOS	TR_DOUBLE	-1.5	No

bex_p: Mobility temperature exponent of PMOS	TR_DOUBLE	-1.5	No
ucex_n: Longitudinal critical field temperature exponent of NMOS	TR_DOUBLE	0.8	No
ucex_p: Longitudinal critical field temperature exponent of PMOS	TR_DOUBLE	0.8	No
ibbt_n: Temperature coefficient for IBB of NMOS (1/K)	TR_DOUBLE	9.0e-4	No
ibbt_p: Temperature coefficient for IBB of PMOS (1/K)	TR_DOUBLE	9.0e-4	No
avto_n: Area related threshold voltage mismatch parameter of NMOS (Vm)	TR_DOUBLE	0.0	No
avto_p: Area related threshold voltage mismatch parameter of PMOS (Vm)	TR_DOUBLE	0.0	No
akp_n: Area related gain mismatch parameter of NMOS (m)	TR_DOUBLE	0.0	No
akp_p: Area related gain mismatch parameter of PMOS (m)	TR_DOUBLE	0.0	No
agamma_n: Area related body effect mismatch parameter of NMOS (V^(1/2)m)	TR_DOUBLE	0.0	No
agamma_p: Area related body effect mismatch parameter of PMOS (V^(1/2)m)	TR_DOUBLE	0.0	No
scale: Scale parameter	TR_DOUBLE	1.0	No
tnom: Nominal temperature of model parameters (K)	TR_DOUBLE	300.15	No
tmp: Model simulation temperature (K)	TR_DOUBLE	300.15	No

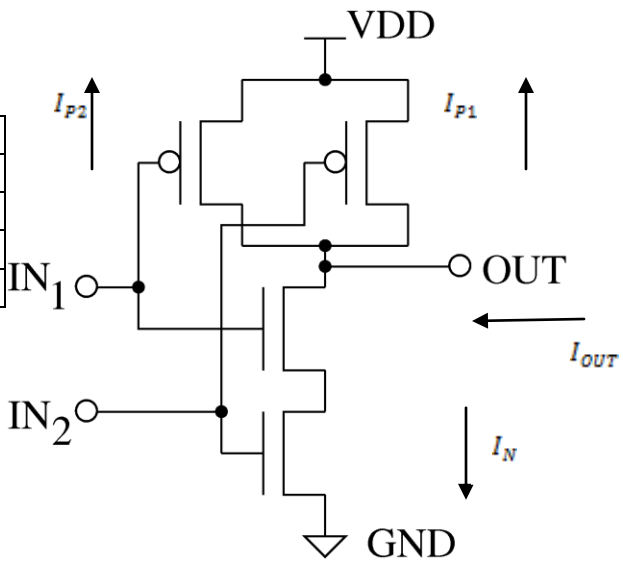
Example:
cmos2nand:nand 1 2 3 4 0

Notes:
This implementation of cmos nand gate is based on EKV 2.6 [1] mosfet model.

Known Bugs:
No known bugs.

Implementation Details:
This element is implemented as a fREEDA **Intrinsic Super Element** based on EKV 2.6 MOSFET model [1]. The element has **4 state variables:** Input Voltage-1(VIN_1), Input Voltage-2(VIN_2), Output Voltage (VOUT) and Power Supply Voltage (VDD). Following is the schematic and truth table of 2-input nand gate:

IN1	IN2	OUT
0	0	0
0	1	0
1	0	0
1	1	1



If it would have been implemented as **Extrinsic Super Element,** then there would have been **12 state variables** (3 corresponding to each transistor). Intrinsic implementation has reduced the state variables by factor of 3 which will lead to faster run time of simulation

State Variables of Intrinsic Super Element:
$x[0] = VDD$ $x[1] = VIN1$ $x[2] = VIN2$ $x[3] = VOUT$

State variables of EKV PMOS and NMOS have been represented in terms of these variables. This is charged based model. The current entering in each terminal is sum of corresponding AC and DC current.

$$I_{in1} = \frac{dQ_{in1}}{dt} \quad ---(1) \qquad I_{in2} = \frac{dQ_{in2}}{dt} \quad ---(2)$$

In equation (1) and equation (2), Q_{in1} and Q_{in2} indicates charge at gate. The derivative of these charges will give AC current entering in gates. DC current entering in gate is zero.

$$I_{out} = I_N + I_{P1} + I_{P2} + \frac{dQ_{out}}{dt} \quad ---(3)$$

I_N, I_{P1} and I_{P2} are DC currents through nmos and pmos. Q_{out} is charge stored at output node.

Current entering in VDD terminal can be given as:

$$I_{vdd} = -I_{P1} - I_{P2} + \frac{dQ_{VDD}}{dt} \quad ---(4)$$

$I_N, I_{P1}, I_{P2}, Q_{in1}, Q_{in2}, Q_{out}, Q_{VDD}$ are functions of state variables of Intrinsic Super Element.

$$\{I_N, I_{P1}, I_{P2}, Q_{in1}, Q_{in2}, Q_{out}, Q_{VDD}\} = f(x[0], x[1], x[2], x[3]) \quad ---(5) \qquad [1]$$

References:

[1] The EKV 2.6 Documentation: http://legwww.epfl.ch/ekv/pdf/ekv_v262.pdf

***Sample Netlist**:*

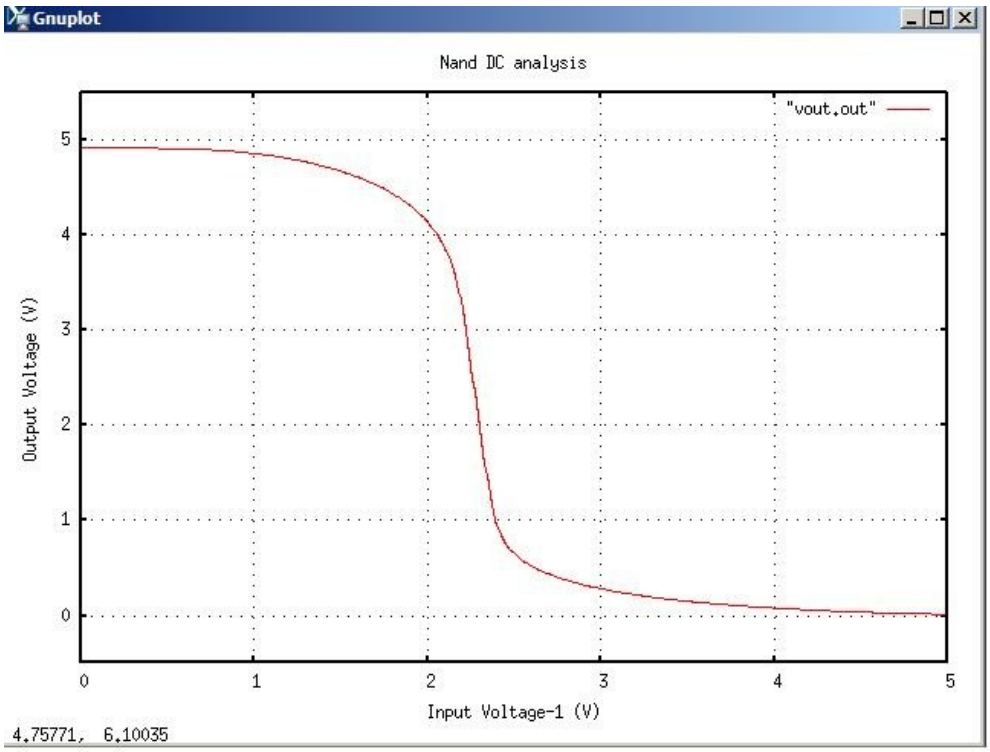
- **DC Analysis**

The following netlist plots the output voltage of the CMOS gate for an input voltage range of 0 ~ 5V for V_{in1} and constant V_{in2} = 5V.

```
* CMOS Nand DC Analysis
***This netlist is for  DC Analysis of 2 input Cmos Nand Gate ***
.dc sweep="vsource:Vin1" start=0 stop=5 step=0.01
*** DC Sweep First input
vsource:Vin1 22 0
*** Tie Second input to Vdd
vsource:Vin2 33 0 vdc=5
*** Vdd connection
vsource:Vdd 1 0 vdc=5
***Nand Instantiation
cmos2nand:nand 1 2 3 4 0
**  Source Resistance and Capacitance
r:in2 22 2 r=10
r:in3 33 3 r=10
c:in2 2 0 c=1e-12
c:in3 3 0 c=1e-12
****Output Resistance and Capacitance
r:R 4 0 r=1000000
c:C 4 0 c=1e-12
.options gnuplot
.out plot term 4 vt in "vout.out"
.out plot term 22 vt in "vin1.out"
.out plot term 33 vt in "vin2.out"
.end
```

Validation:

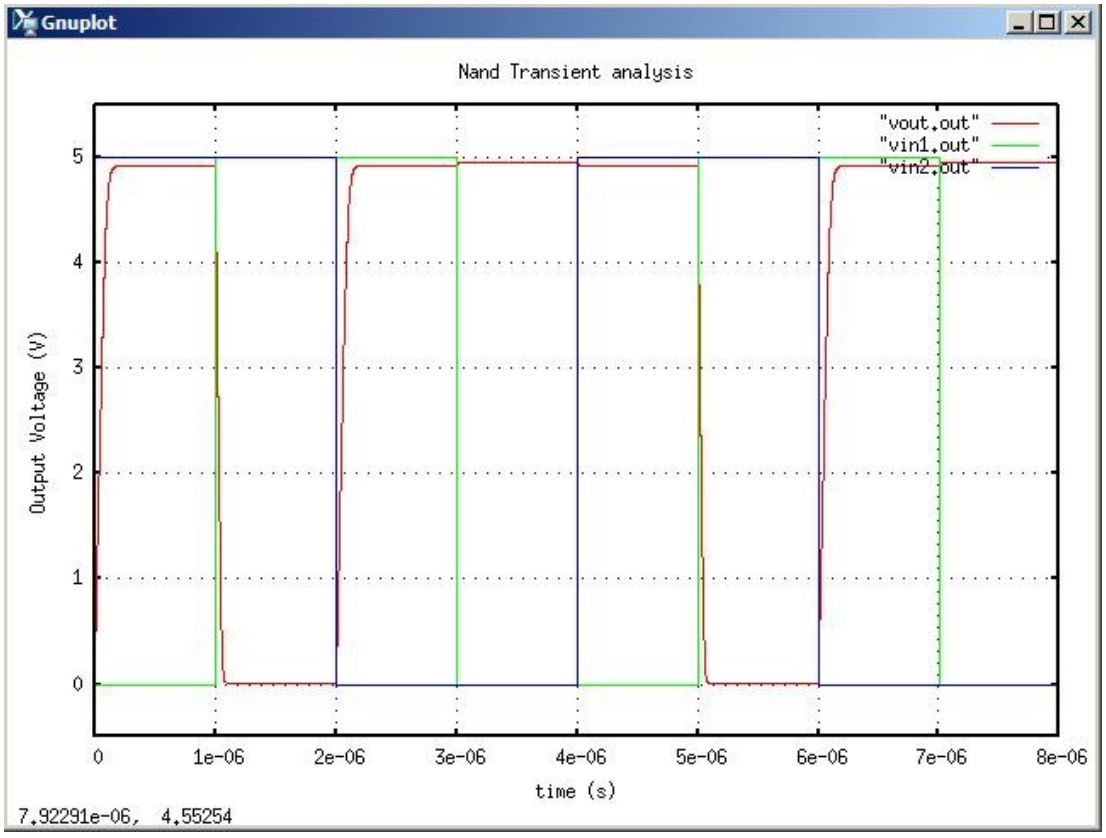
The output graph from the above netlist is shown below:



- **Transient Analysis**
  * CMOS Nand Transient Analysis

  *** This netlist is for Transient analysis of Cmos 2 input Nand Gate***
  .tran2 tstop=8e-6 tstep=1e-9 out_steps=1
  vpulse:Vin2 22 0 v1=0 v2=5 td=1e-6 per=4e-6 pw=2e-6 tr=0.002e-6 tf=0.002e-6
  vpulse:Vin3 33 0 v1=0 v2=5 per=4e-6 pw=2e-6 tr=0.002e-6 tf=0.002e-6
  **** Vdd connection
  vsource:Vdd 1 0 vdc=5
  ***** Nand instantiation
  cmos2nand:nand 1 2 3 4 0
  ** Source Resistance and Capacitance
  r:in2 22 2 r=10
  r:in3 33 3 r=10
  c:in2 2 0 c=1e-12
  c:in3 3 0 c=1e-12
  *** Load Resistance and Capacitance
  r:R 4 0 r=1000000
  c:C 4 0 c=1e-12
  .options gnuplot
  .out plot term 4 vt in "vout.out"
  .out plot term 22 vt in "vin1.out"
  .out plot term 33 vt in "vin2.out"
  .end

Validation:
The output graph from the above netlist is shown below:



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Credits:

Name	Affiliation	Date	Links
Shivam Priyadarshi shivam.priyadarshi@gmail.com	NCSU	April, 2009	http://www.ncsu.edu/
Nikhil Kriplani nkriplani@gmail.com	NCSU	April, 2009	http://www.ncsu.edu/