Description:
MOS Capacitor with gate tunneling current

Form: capacitorMos: <instance name> n_1 n_2 n_3

n_1 is the gate terminal
n_2 is dummy terminal left open
n_3 is the body terminal (reference)

Parameters:

Parameter	Type	Default value	Required?
w: Width of the device (cm)	TR_DOUBLE	1e-4	Yes
l: Length of the gate (cm)	TR_DOUBLE	1e-4	Yes
tox: Oxide thickness (cm)	TR_DOUBLE	2.48e-7	No
t: Temperature (Kelvin)	TR_DOUBLE	300	No
npoly: Poly Doping (1/cm3)	TR_DOUBLE	9e19	No
nsub: Substrate Doping(1/cm3)	TR_DOUBLE	4.7e17	No
moxecb: Oxide Mass for ECB(kg)	TR_DOUBLE	3.64e-31	No
moxevb: Oxide Mass for EVB(kg)	TR_DOUBLE	2.73e-31	No
moxhvb: Oxide Mass for HVB(kg)	TR_DOUBLE	2.91e-31	No
phibecb: Electron Tunneling Barrier Height for ECB(eV)	TR_DOUBLE	3.1	No
phibevb: Electron Tunneling Barrier Height for EVB(eV)	TR_DOUBLE	4.2	No
phibhvb: Electron Tunneling Barrier Height for HVB(eV)	TR_DOUBLE	4.5	No
phib0ecb: Si/SiO2 Barrier Height for ECB (eV)	TR_DOUBLE	3.1	No
phib0evb: Si/SiO2 Barrier Height for EVB (eV)	TR_DOUBLE	3.1	No
phib0hvb: Si/SiO2 Barrier Height for HVB (eV)	TR_DOUBLE	4.5	No
vfb: Flat-Band Voltage (V)	TR_DOUBLE	-0.9	No
Parameter	Type	Default value	Required?
epsrox: Relative Permittivity of	TR_DOUBLE	3.9	No

Oxide			
S: subthreshold swing (v/dec)	TR_DOUBLE	75e-3	No

Example:
capacitorMos:c1 1 2 0 w=5e-4 l=10e-4 tox=1e-7

Description:
This model includes the different tunneling components in a $Si/SiO_2/Si$ structure:
ECB   electron tunneling from the conduction band (Dominant Current in NMOS)
EVB   electron tunneling from the valence band
HVB   hole tunneling from the valence band
<u>Tunneling model:</u>

$$J_n = \frac{q^3}{8\pi\phi_b\varepsilon_{ox}} \cdot C(V_g, V_{ox}, T_{ox}, \phi_b) \cdot \exp\left(\frac{-8\pi\sqrt{2m_{ox}}\phi_b^{3/2}\left[1-\left(1-\frac{|V_{ox}|}{\phi_b}\right)^{3/2}\right]}{3hq|E_{ox}|}\right)$$

where:
$E_{ox} = V_{ox}/T_{ox}$
T_{ox}: the oxide thickness
m_{ox}: effective mass in the oxide
Developed by empirical fitting, $C(V_g, V_{ox}, T_{ox}, \phi_b)$ can be expressed as

$$C(V_g, V_{ox}, T_{ox}, \phi_b) = \exp\left[\frac{20}{\phi_b}\left(\frac{|V_{ox}|-\phi_b}{\phi_{b0}}+1\right)^{\alpha} \cdot \left(1-\frac{|V_{ox}|}{\phi_b}\right)\right] \cdot \left(\frac{V_g}{T_{ox}}\right) \cdot N$$

where:
α : fitting parameter depending on the tunneling process (0.6 for ECB, 1 for EVB, 0.4 for HVB)
ϕ_{b0} : Si/SiO_2 barrier height (e.g., 3.1ev for electron and 4.5 ev for hole)
ϕ_b : actual tunneling barrier height(e.g., 3.1ev for ECB, 4.2ev for EVB, and 4.5ev for HVB with Si electrode)

N for ECB and HVB:

$$N = \frac{\varepsilon_{ox}}{T_{ox}}\left\{n_{inv}v_t \cdot \ln\left[1+\exp\left(\frac{V_{ge}-V_{th}}{n_{inv}v_t}\right)\right] + n_{acc}v_t \cdot \ln\left[1+\exp\left[-\left(\frac{V_g-V_{FB}}{n_{acc}v_t}\right)\right]\right]\right\}$$

where:
n_{inv} and n_{acc}:   swing parameter;
V_{th}:   threshold voltage;

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V_{FB}:   flat-band voltage;

$V_t(=kT/q)$:   thermal voltage;

V_{ge}:   gate voltage minus the gate-depletion voltage (V_g-V_{poly})

$$V_{ge} = V_{FB} + \phi_{s0} + \frac{q\varepsilon_{Si}N_{poly}T_{ox}^2}{\varepsilon_{ox}^2} \cdot \left(\sqrt{1 + \frac{2\varepsilon_{ox}^2\left(V_g - V_{FB} - \phi_{s0}\right)}{q\varepsilon_{Si}N_{poly}T_{ox}^2}} - 1 \right)$$

where:

ε_{Si} and ε_{ox} : dielectric constants of Si and SiO$_2$, respectively

N_{poly}:   poly gate doping concentration

ϕ_{s0} :   surface potential equaling twice the Fermi potential ϕ_f

N for EVB

$$N = \frac{\varepsilon_{ox}}{T_{ox}} \cdot \left\{ n_{EVB}v_t \cdot \ln\left[1 + \exp\left(\frac{|V_{ox}| - \phi_g}{n_{EVB}v_t} \right) \right] \right\}$$

where: ϕ_g =E$_g$/q

$$V_{ox} = V_{ge} - \phi_s - V_{FB}$$

$$\phi_s = \left[\frac{\gamma}{2}\left(-1 + \sqrt{1 + \frac{4\left(V_g - V_{ge} - V_{FB}\right)}{\gamma^2}} \right) \right]^2$$

$$\gamma = \frac{\sqrt{2\varepsilon_{Si}qN_{sub}}}{C_{ox}}$$

where:

ϕ_s :   surface band bending of the substrate

N_{sub} : channel doping concentration

γ :   body-effect parameter

References:

[1].   Wen-Chin Lee, Chenming Hu, "Modeling CMOS Tunneling Currents Through Ultrathin Gate Oxide Due to Conduction- and Valence-Band Electron and Hole Tunneling", *IEEE Trans. Electron Devices*, Vol. 48, No. 7,pp. 1366-1372, 2001

[2].   Kingsuk Maitra, Navakanta Bhat, "Analytical approach to integrate the different components of direct tunneling current through ultrathin gate oxides in n-channel metal-oxide-semiconductor field-effect transistors, *Journal of Applied Physics*, Vol. 93, No. 2, pp. 1064-1068, 2003.

[3].   V. Rizzoli, A. Lipparini, A. Costanzo, F. Mastri, C. Ceccetti, A. Neri and D. Masotti, "State-of-the-art harmonic balance simulation of forced nonlinear microwave circuits by the piecewise technique", *IEEE Trans. On Microwave Theory and Techniques,* Vol. 40, No. 1, pp 12-28, 1992.

Sample Netlist:
This netlist incorporates all the common types of analyses – ac, dc and transient.

```
.options f0=5.1e9 method=1 jupdm=1
*** DC Analysis
*.dc sweep="vsource:vgate" start=-2 stop=3 step=.01
*.dc

*** AC Analysis
*.ac start = 0 stop = 500e6 n_freqs = 10

*** Transient Analysis
.tran2 tstop = 2E-9 tstep = 1E-11 out_steps=1
*.SVtran2 tstop = 1e-6 tstep = 10e-9 out_steps = 1

*** Sources
*vsource:vgate 1 0 vdc=1.5
vpulse:v1 1 0 v1=0 v2=4 td=0 tr=50e-12 tf=50e-12 pw=100e-12 per=200e-12
*vsource:vgate 1 0 vdc=1.5 vac=0.5 f=1Ghz delay=0

*** Network description
res:r1 1 2 r=1000
res:r2 2 0 r=1000
res:r3 3 0 r=1000000
capacitorMos:c1 2 3 0 w=1e-4 l=1e-4

***Transient and DC plotting
.out plot term 1 vt in "node1.out"
.out plot term 2 vt in "node2.out"
.out plot element "moscap1:c1" 0 it in "itunn.out"

*** plots from ac analysis
*.out plot term 1 vf mag  in "node1.out"
*.out plot term 2 vf mag  in "node2.out"
*.out plot element "moscap1:c1" 0 if mag in "itunn.out"
```
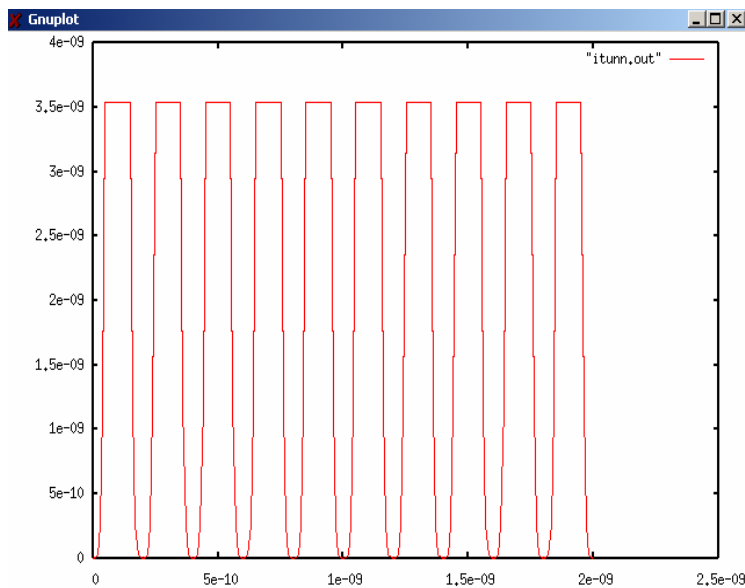

Validation:
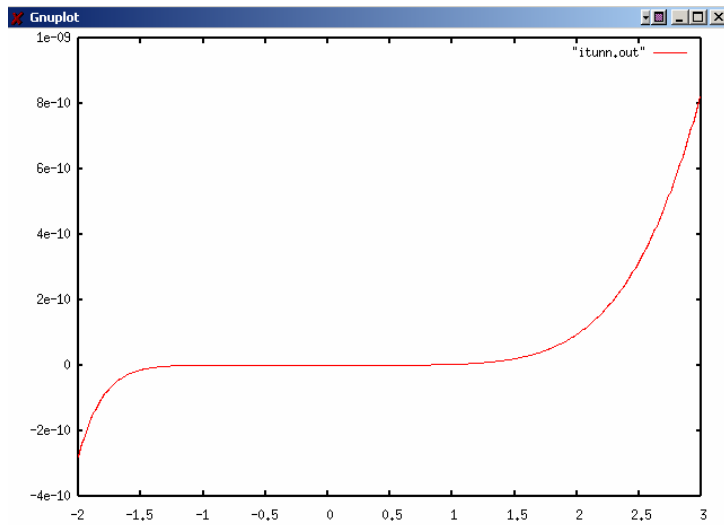
Figure 1: Results from a dc run on the model showing the tunneling current through the capacitor.

Figure 2: The current through the capacitor during a transient analysis. The input was a pulse waveform of period 200 ps from 0 to 4V.

Known Bugs:
No known bugs.

Credits:

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Model Documentation

The goal of our project was to model the tunneling currents through a MOS gate-stack. To accomplish this we chose to model a MOS capacitor with tunneling. The capacitor is a two terminal device as shown in the figure 1 and on applying a voltage to the gate current flows from the gate to the substrate because of the tunneling effect and effectively reduces the capacitor to a nonlinear resistor. This is a highly non-linear process and is described by the equations listed on the next page.
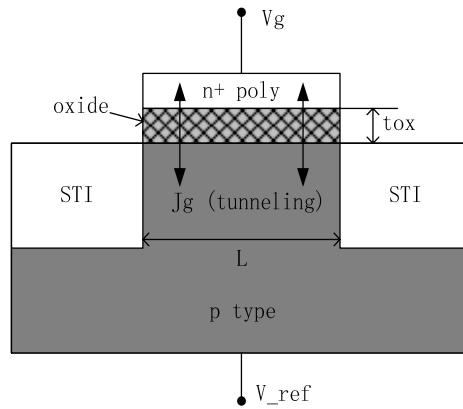

Figure 1 Cross section of a MOS Capacitor

Achievements
- We have come up with a method to reduce the non-linear and complex equations describing tunneling into a more tractable form. The process will be discussed in detail in the following sections. The accuracy of the modified equations can be increased by simply taking a larger number of terms in the power series.
- These modified equations were parameterized based on Rizzolli's equations [3]. We also developed a method to use the parameterization when the function inside the exponential is non-linear.
- Following this, we developed a model in *fReeda* and successfully tested it for *ac, dc* and *transient* analyses. The results from the dc analysis are attached in appendix A.

We have developed a circuit model for tunneling based on a physical model instead of using empirically fitted equations. Hence, this model is scalable and can be easily integrated with a full MOS transistor model to include gate tunneling.

Tunneling has become an issue of major concern in present day CMOS devices. As gate oxide dimensions are scaled down, leakage due to gate tunneling has started to make an impact on the static power consumption in VLSI circuits. The model below presents an accurate analytical description of the direct tunneling currents through ultrathin gate oxides.
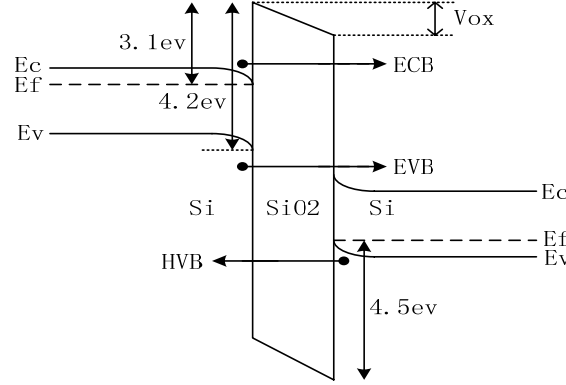
Figure 2: Tunneling Components

As shown in the figure 2, there are three different tunneling components in a Si/SiO₂/Si structure:

ECB: electron tunneling from the conduction band;
EVB: electron tunneling from the valence band;
HVB: hole tunneling from the valence band;
From [1,2] the current is given as:

$$J_n = \frac{q^3}{8\pi\phi_b\varepsilon_{ox}}\cdot C(V_g,V_{ox},T_{ox},\phi_b)\cdot \exp\left(\frac{-8\pi\sqrt{2m_{ox}}\phi_b^{3/2}\left[1-\left(1-\frac{|V_{ox}|}{\phi_b}\right)^{3/2}\right]}{3hq|E_{ox}|}\right) \qquad eqn.(1)$$

where, $C(V_g,V_{ox},T_{ox},\phi_b) = \exp\left[\frac{20}{\phi_b}\left(\frac{|V_{ox}|-\phi_b}{\phi_{b0}}+1\right)^{\alpha}\cdot\left(1-\frac{|V_{ox}|}{\phi_b}\right)\right]\cdot\left(\frac{V_g}{T_{ox}}\right)\cdot N \qquad eqn.(2)$

α, ϕ_{b0}, ϕ_b, m_{ox}, N are different for ECB,EVB and HVB.

For ECB and HVB,

$$N = \frac{\varepsilon_{ox}}{T_{ox}}\left\{n_{inv}v_t\cdot\ln\left[1+\exp\left(\frac{V_{ge}-V_{th}}{n_{inv}v_t}\right)\right]+n_{acc}v_t\cdot\ln\left[1+\exp\left[-\left(\frac{V_g-V_{FB}}{n_{acc}v_t}\right)\right]\right]\right\} \qquad eqn.(3)$$

For EVB,

$$N = \frac{\varepsilon_{ox}}{T_{ox}}\cdot\left\{n_{EVB}v_t\cdot\ln\left[1+\exp\left(\frac{|V_{ox}|-\phi_g}{n_{EVB}v_t}\right)\right]\right\} \qquad eqn.(4)$$

ECB, EVB and HVB currents are modeled separately and the gate current is the total of these three currents.

2.1 Parameterization and Modeling

The first step in our modeling process was to investigate the behavior of the various equations describing the tunneling currents. To do this, we used MATLAB to generate the $J_g - V_g$ curves. As can be seen from figure 3, the current behaves in a non-linear fashion. Following this, we looked into the variation of $C(V_g,V_{ox},T_{ox},\phi_b)$, N and the

exponential term (E1) in the equation for J_n (eqn. 1). The behavior of C and N was not highly non-linear and hence we decided to model the equations as they were. However E1 was highly non-linear and could not be modeled directly because it could lead to convergence problems in the simulator.
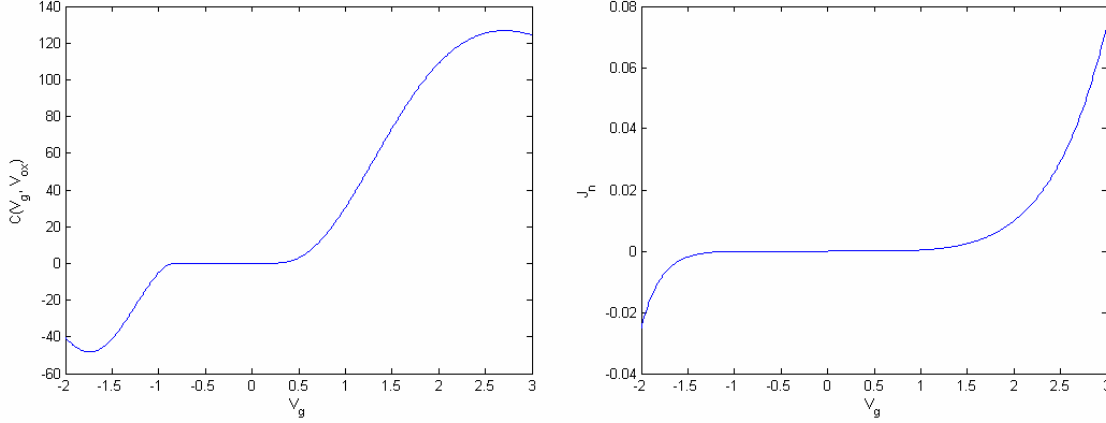
Fig. 3 C (V$_g$, V$_{ox}$) vs. V$_g$ and J$_g$ vs. V$_g$

After having identified the term determining the non-linear behavior we looked for ways

to parameterize it. Because $\left(1 - \dfrac{|V_{ox}|}{\phi_b}\right)^{3/2}$ is not easy to parameterize, we use the best

fitting function in Matlab to expand it into a power series. As we identified, a quadratic expansion gives us a reasonably accurate fit over most of the region and hence we decided to go ahead with it.

$$(1-\chi)^{3/2} \cong 0.58 \cdot \chi^2 - 1.6 \cdot \chi + 1 \quad \text{where: } \chi = \frac{|V_{ox}|}{\phi_b} \quad (0 \leq \chi \leq 1)$$

So the current reduces to:

$J_g = A_1 \cdot C(V_g, V_{ox}, T_{ox}, \phi_b) \cdot \exp(K' \cdot (1.6 - 0.58 \cdot \chi))$. This can be further reduced to

$J_g = i_{decb} \cdot C(V_g, V_{ox}, T_{ox}, \phi_b)$ where, $i_{decb} = K_{0ecb} \cdot \exp(\alpha_{ecb} \cdot |V_{ox}|)$. HVB and EVB currents can be expressed similarly.

We parameterized the above equation using the method suggested by Rizzoli. Choosing *x(t)* as a State Variable gives us:

$$|V_{ox}(t)| = \begin{cases} x(t) & if \quad x(t) \leq V_1 \\ V_1 + \dfrac{1}{\alpha_{ecb}} \ln(1 + \alpha_{ecb}(x(t) - V_1)) & if \quad x(t) > V_1 \end{cases}$$

$$i_{decb}(t) = \begin{cases} K_{oecb} \cdot \exp(\alpha_{ecb} x(t)) & if \quad x(t) \leq V_1 \\ K_{oecb} \cdot \exp(\alpha_{ecb} V_1)(1 + \alpha_{ecb}(x(t) - V_1)) & if \quad x(t) > V_1 \end{cases}$$

V$_1$ calculated by setting the slope of the i_{decb} w.r.t. /V$_{ox}$/ equal to 1. This gives us:

$$V_1 = \frac{1}{\alpha_{ecb}} \ln\left(\frac{1}{K_{0ecb}\alpha_{ecb}}\right)$$

We calculated i$_{devb}$ and i$_{dhvb}$ from i$_{decb}$ by accounting for the difference in proportionality constants.

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$$\text{HVB: } i_{dhvb} = K_{0hvb} \cdot \left(\frac{i_{decb}}{K_{oecb}} \right)^{\frac{\alpha_{hvb}}{\alpha_{ecb}}} \qquad \text{EVB: } i_{devb} = K_{0evb} \cdot \left(\frac{i_{decb}}{K_{oecb}} \right)^{\frac{\alpha_{evb}}{\alpha_{ecb}}}$$

Finally,

$$J_g = i_{decb} . C_{ecb} + i_{dhvb} . C_{hvb} + i_{devb} . C_{evb}$$

2.2 Implementation in fReeda

After getting the parameterized equations we developed a methodology to implement these equations in fReeda. As can be seen from the development above, even though V_g is the external gate voltage applied to the system, the currents are determined by $|V_{ox}|$. For a given value of the state variable $x(t)$ we get a certain value of $|V_{ox}|$. Now we have to relate this $|V_{ox}|$ with the external gate voltage, V_g in order to solve the system of equations. We could think of two possible ways to do this.

The first way would be to calculate a value for V_g from the $|V_{ox}|$ calculated using $x(t)$. However, from the equation below, finding an inverse function relating the two is a complex task. Also, we have the absolute value of V_{ox} and that will give us two possible values for V_g. Since we do not have any other information available, we cannot pick the correct value.

A more practical way of modeling this set of equations would be to choose two state variables: V_g and $x(t)$. The two state variables can be used to calculate two different values of $|V_{ox}|$ and the error term between these two values can be minimized to arrive at a solution for the system of equations. $|V_{ox}|$ obtained from $x(t)$ is used to calculate the currents in the system.

We decided to implement this procedure in our model by creating an extra dummy terminal which would be left open in the circuit. The error function is assigned as a current through this terminal. Since the terminal is left open, the current flowing into it from the linear part of the circuit is zero and hence the error term is solved to reach zero.

2.3 Improving Accuracy

Here we demonstrated a model for the tunneling currents using a quadratic expansion of the term in the exponential. However, depending on the accuracy required, a higher order series can be selected. For example, if we use a cubic form, the term inside the exponential will be quadratic. Hence, Rizzoli's parameterization cannot be used as it is. We can choose the whole term in exponential as a state variable, and then find the relationship between this state variable and $|V_{ox}|$.

APPENDIX A
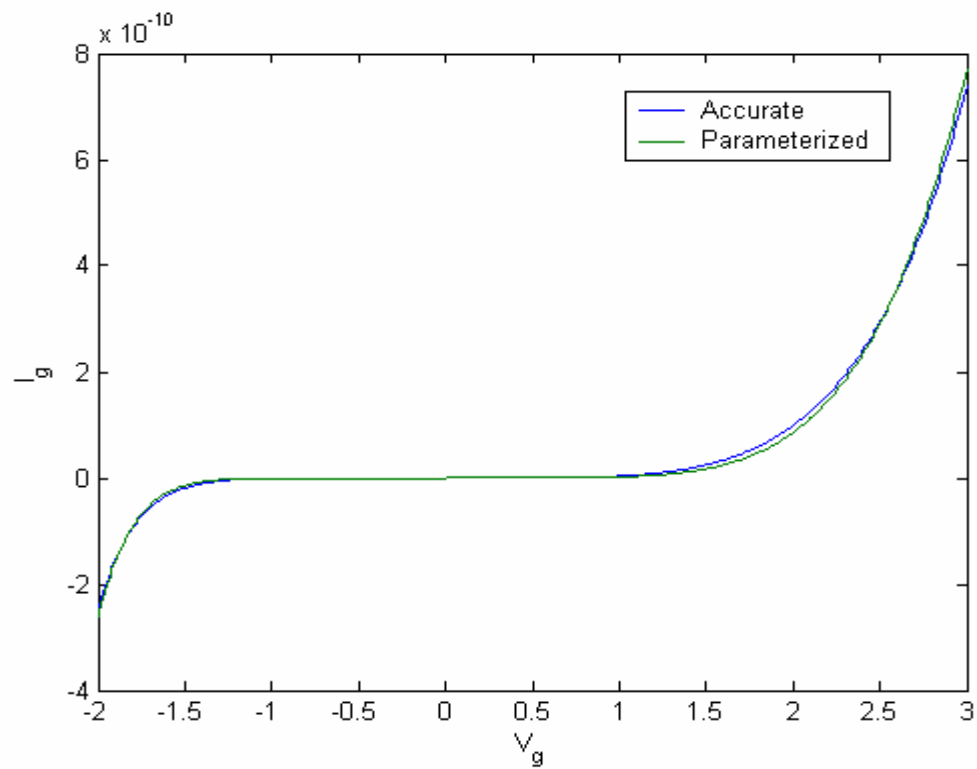
Fig. 4 Comparison of accurate and parameterized current equations obtained from MATLAB
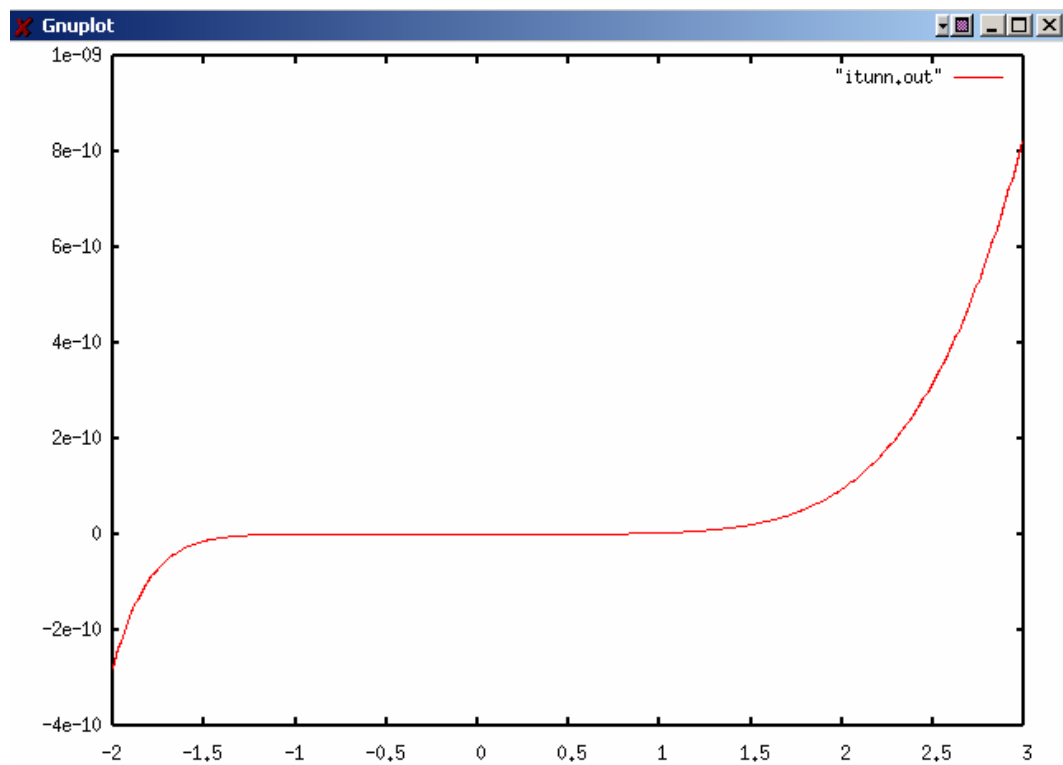
Fig. 5 Tunneling Current obtained using DC analysis in Freeda

References:

[1]. Wen-Chin Lee, Chenming Hu, "Modeling CMOS Tunneling Currents Through Ultrathin Gate Oxide Due to Conduction- and Valence-Band Electron and Hole Tunneling", *IEEE Trans. Electron Devices*, Vol. 48, No. 7,pp. 1366-1372, 2001

[2]. Kingsuk Maitra, Navakanta Bhat, "Analytical approach to integrate the different components of direct tunneling current through ultrathin gate oxides in n-channel metal-oxide-semiconductor field-effect transistors, *Journal of Applied Physics*, Vol. 93, No. 2, pp. 1064-1068, 2003.

[3]. V. Rizzoli, A. Lipparini, A. Costanzo, F. Mastri, C. Ceccetti, A. Neri and D. Masotti, "State-of-the-art harmonic balance simulation of forced nonlinear microwave circuits by the piecewise technique", *IEEE Trans. On Microwave Theory and Techniques,* Vol. 40, No. 1, pp 12-28, 1992.