Philips MOS9 (P – channel) MOSFET model **mosp9**

Description:

This element implements a Philips MOS9 (P – channel) Model.

Form:

mosp9 :(instance name) n₁ n₂ n₃ n₄ <parameter list>

Instance name is the model name,

n_1 is the drain node,
n_2 is the gate node,
n_3 is the source node,
n_4 is the bulk node.

Parameters:

Parameters	Type	Default value	Required?
level: Level of this model. Must be set to 1	Double	903	no
VT0:Threshold voltage at zero back-bias for the actual transistor at the actual temperature(volts)	Double	1.082125	no
K0:low back-bias body factor for the actual transistor($V^{1/2}$)	Double	4.280174e-01	no
K: high back-bias body factor for the actual transistor($V^{1/2}$)	Double	4.280174e-1	no
PHIB: Surface potential at strong inversion for the actual transistor at the actual temperature(volts)	Double	6.225999e-01	no
VSBX: Transition voltage for the dual-k-factor model for the actual transistor(volts)	Double	1.000000e-12	no
BET: gain factor for the actual transistor at the actual temperature(A/V^2)	Double	4.841498e-04	no
THE1:coefficient of the mobility reduction due to the gate induced field for the actual transistor at the actual temperature(1/V)	Double	2.046809e-01	no
THE2:coefficient of the mobility reduction due to the back-biased for the actual transistor at the actual temperature($1/V^{0.5}$)	Double	1.492490e-01	no
THE3:coefficient of the mobility reduction due to the lateral field for the actual transistor at the actual temperature(1/V)	Double	3.267633e-02	no
GAM1:coefficient for the drain induced threshold shift for large gate drive for the actual transistor ($V^{(1-ETADS)}$)	Double	9.905701e-01	no

ETADS: Exponent of the vds depedence of GAM1 for the actual transistor	Double	6.000000e-01	no
ALP: factor of the channel length modulation for the actual transistor	Double	4.766925e-02	no
VP: characteristic voltage of the channel length modulation for the actual transistor (V)	Double	1.861200e-01	no
GAM00: coefficient for the drain induced threshold shift at zero gate drive for the actual transistor	Double	1.118334e-02	no
ETAGAM: exponent of the back-bias dependence of gam0 for the actual transistor	Double	1.0	no
M0:factor of the subthreshold slope for the actual transistor at the actual temperature	Double	3.801987e-01	no
ETAM: exponent of the back-bias dependence of m for the actual transistor	Double	1.0	no
PHIT: thermal voltage at the actual temperature(volts	Double	2.662680e-02	no
ZET1: weak inversion correction factor for the actual transistor	Double	1.270446	no
VSBT: limiting voltage of vsb dependence of m and gam0 for the actual transistor(volts)	Double	1.000000e02	no
A1: factor of the weak avalanche current for the actual transistor	Double	6.858299	no
A2: exponent of the weak avalanche current for the actual transistor(volts)	Double	5.732410e01	no
A3: factor of the drain source voltage above which weak avalanche occurs for the actual transistor	Double	4.254087e-01	no
COX: gate to channel capacitance for the actual transistor(farads)",	Double	2.717113e-014	no
CGDO: gate drain overlap capacitance for the actual transistor(farads)"	Double	6.358400e-15	no
CGSO: gate source overlap capacitance for the actual transistor(farads)",	Double	6.358400e-15	no
Geometrical Parameters			
TOX: thickness of gate oxide layer (meters)"	Double	25e-9	no
MULT: number of devices operating in parallel	Double	1.0	no
LER: Effective channel length of the reference transistor (m)	Double	1.25e-6	no
WER: Effective channel width of the reference transistor (m)	Double	20e-6	no
LVAR: Difference between the actual and the programmed poly-silicon gate length (m)	Double	-0.460e-6	no
LAP: Effective channel length reduction per side due to the lateral diffusion of the source/drain dopant ions (m)	Double	0.025e-6	no
WVAR: Difference between the actual and the programmed field-oxide opening (m)",	Double	-0.130e-6	no
WOT: Effective reduction of the channel width per side due to the lateral diffusion of the channel-stop dopant ions (m)	Double	0.000e-6	no

TR: Temperature at which the parameters for the reference transistor have been determined (0C)	Double	21	no
VT0R: Threshold voltage at zero back-bias for the reference transistor at the reference temperature (V)	Double	1.1	no
STVT0: Coefficient of the temperature dependence VT0 (VK-1)	Double	-1.70e-3	no
SLVT0: Coefficient of the length dependence of VT0 (Vm)	Double	-0.035e-6	no
SL2VT0: Second coefficient of the length dependence of VT0 (Vm2)	Double	0.0	no
SL3VT0: Third coefficient of the length dependence of VT0 (V)	Double	0.0	no
SWVT0: Coefficient of the width dependence of VT0 (Vm)	Double	0.050e-6	no
K0R: Low-backbias body factor for the reference transistor (V1/2)	Double	0.47	no
SLK0: Coefficient of the length dependence of K0 (V1/2m)	Double	-0.200e-6	no
SL2K0: Second coefficient of the length dependence of K0 (V1/2m2)	Double	0.0	no
SWK0: Coefficient of the width dependence of K0 (V1/2m)	Double	0.115e-6	no
KR: High-backbias body factor for the reference transistor (V1/2)	Double	0.47	no
SLK: Coefficient of the length dependence of K (V1/2m)	Double	-0.200e-6	no
SL2K: Second coefficient of the length dependence of K (V1/2m2)	Double	0.0	no
SWK: Coefficient of the width dependence of K (V1/2m)	Double	0.115e-6	no
PHIBR: Surface potential at strong inversion for the reference transistor at the reference temperature (V)	Double	0.65	no
VSBXR: Transition voltage for the dual-k-factor model for the reference transistor (V)	Double	1.0e-12	no
SLVSBX: Coefficient of the length dependence of VSBX (Vm)	Double	0.0	no
SWVSBX: Coefficient of the width dependence VSBX (Vm)	Double	0.0	no
BETSQ: Gain factor for an infinite square transistor at the reference temperature (AV-2)	Double	26.1e-6	no
ETABET: Exponent of the temperature dependence of the gain factor (-	Double	1.6	no
LP1: Characteristic length of first profile (m)	Double	1e-06	no
FBET1: Relative mobility decrease due to first profile (-)	Double	0.0	no
LP2:Characteristic length of second profile (m)	Double	1e-8	no
FBET2: Relative mobility decrease due to second profile (-)	Double	0.0	no
THE1R: Coefficient of the mobility reduction due to the gate-induced field for the reference transistor at the reference temperature (V-1)	Double	0.190	no

STTHE1R: Coefficient of the temperature dependence of THE1 for the reference transistor (V-1K-1)	Double	0.000e-3	no
SLTHE1R: Coefficient of the length dependence of THE1 at the reference temperature (V-1m)	Double	0.45e-6	no
STLTHE1: Coefficient of the temperature dependence of the length dependence of THE 1 (V-1mK-1)	Double	0.000e-3	no
GTHE1: Parameter that selects either the old ( ) or the new ( ) scaling gTHE0 = gTHE1 = rule of THE 1 (-)	Double	0.0	no
SWTHE1: Coefficient of the width dependence of THE1 (V-1m)	Double	-0.08e-6	no
WDOG: Characteristic drawn gate width, below which dogboning appears (m)	Double	0.0	no
FTHE1: Coefficient describing the geometry dependence of THE1 for W < WDOG (-)	Double	0.0	no
THE2R: Coefficient of the mobility reduction due to the back-bias for the reference transistor at the reference temperature (V-1/2)	Double	0.165	no
STTHE2R: Coefficient of the temperature dependence of THE2 for the reference transistor (V-1/2K-1)	Double	0.000e-9	no
SLTHE2R: Coefficient of the length dependence of THE2 at the reference temperature (V-1/2m)	Double	-0.075e-6	no
STLTHE2: Coeffient of the temperature dependence of the length dependence of THE2 (V-1/2mK-1)	Double	0.000e-3	no
SWTHE2: Coefficient of the width dependence of THE2 (V-1/2m)	Double	0.020e-6	no
THE3R: Coefficient of the mobility reduction due to the lateral field for the reference transistor at the reference temperature (V-1)	Double	0.027	no
STTHE3R: Coefficient of the temperature dependence of THE3 for the reference temperature (V-1K-1)	Double	0.000e-9	no
SLTHE3R: Coefficient of the length dependence of THE3 at the reference temperature (V)	Double	0.027e-6	no
STLTHE3: Coefficient of the temperature dependence of the length dependence of THE3 (V-1mK-1)	Double	0.000e-3	no
SWTHE3: Coefficient of the width dependence of THE3 (V-1m)	Double	0.011e-6	no
GAM1R: Coefficient for the drain induced threshold shift for large gate drive for the reference transistor (V(1-ETADS))	Double	0.12	no
SLGAM1: Coefficient of the length dependence of GAM1 (V^1-ETADS)m	Double	0.105e-6	no
SWGAM1: Coefficient of the width dependence of GAM1 (V^1-ETADS)m)	Double	-0.011e-6	no
ETADSR: Exponent of the VDS dependence of GAM1 for the reference transistor	Double	0.6	no
ALPR: Factor of the channel-length modulation for the reference transistor (-)	Double	0.044	no
ETAALP: Exponent of the length dependence of ALP (-)	Double	0.17	no
SLALP: Coefficient of the length dependence of ALP (mETAALP)	Double	9e-3	no
SWALP: Coefficient of the width dependence of ALP (m)	Double	0.180e-9	no

VPR: Characteristic voltage of the channellength modulation for the reference transistor (V)	Double	0.235	no
GAM00R: Coefficient of the drain induced threshold shift at zero gate drive for the reference transistor (-)	Double	0.007	no
SLGAM00: Coefficient of the length dependence of GAM00 (m2)	Double	11e-15	no
SL2GAM00: Second coefficient of the length dependence of GAM00 (-)	Double	0.0	no
ETAGAMR: Exponent of the back-bias dependence of GAM0 for the reference transistor (-)	Double	1.0	no
M0R: Factor of the subthreshold slope for the reference transistor at the reference temperature (-)	Double	0.375	no
STM0: Coefficient of the temperature dependence of m0 (K-1)	Double	0.000	no
SLM0: Coefficient of the length dependence of m0 (m1/2)	Double	0.047e-3	no
ETAMR: Exponent of the back-bias dependence of m for the reference transistor (-)	Double	1.0	no
ZET1R: Weak-inversion correction factor for the reference transistor (-)	Double	1.3	no
ETAZET: Exponent of the length dependence of ZET1 (-)	Double	0.03	no
SLZET1: Coefficient of the length dependence of ZET1 (mETAZET)	Double	-2.8	no
VSBTR: Limiting voltage of the VSB dependence of m and GAM0 for the reference transistor (V)	Double	100.0	no
SLVSBT: Coefficient of the length dependence of VSBT (Vm)	Double	-0e-6	no
A1R: Factor of the weak-avalanche current for the reference transistor at the reference temperature (-)	Double	10.00	no
STA1: Coefficient of the temperature dependence of a1 (K-1)	Double	0.000	no
SLA1: Coefficient of the length dependence of a1 (m)	Double	-15e-6	no
SWA1: Coefficient of the width dependence of a1 (m)	Double	30.00e-6	no
A2R: Exponent of the weak-avalanche current for the reference transistor (V)	Double	59.0	no
SLA2: Coefficient of the length dependence of a2 (Vm)	Double	-8e-6	no
SWA2: Coefficient of the width dependence of a2 (Vm)	Double	15.00e-6	no
A3R: Factor of the drain-source voltage above which weak-avalanche occurs, for the reference transistor (-)	Double	0.52	no
SLA3: Coefficient of the length dependence of a3 (m)	Double	-0.450e-6	no
SWA3: Coefficient of the width dependence of a3 (m)	Double	-0.14e-6	no
COL: Gate overlap capacitance per unit channel width (Fm-1)	Double	0.320e-9	no

Example:

mosp9: m1 1 2 3 4 l=1.5e-6 w=20e-6

Model Documentation:

Documentation is same as NMOS 9 model. Please refer to mosn9 model documentation.

References:

- Philips document :
  http://www.semiconductors.philips.com/Philips_Models/mos_models/model9/index.html
- fREEDA Element Manual & Programmer's manual :
  http://freeda.org/
- "The operation and modeling of The MOS Transistor", Yannis. P. Tsividis.

Sample Netlist:

*****Test netlist for mosp9 level 903 model******
*****DC Analysis************

* D G S B

mosp9:m9 1 3 0 4
vsource:vds 1 0 vdc=-0.1v
vsource:vsb 0 4 vdc=0
vsource:vgs 3 0

.dc sweep="vsource:vgs" start=-0.6 stop=-6.2 step=-0.6
.out plot element "mosp9:m9" 0 it in "mosp9_id.dc"

.end

Validation:

- **DC Analysis:**

In order to show the accuracy of the model, we discuss here the simulated results and the results given in the Philips document. The size chosen for the reference transistor is W=20 micron and L=1.5 micron.

Fig 1 gives the drain current of the p-channel device as a function of the gate-bias voltage. The drain-bias voltage is fixed at -0.10 volts for p-channel devices, the back bias and gate voltages have been varied as shown below.

Back-bias Vsb :   0➔-4.5 volts for n channel at steps of -1.5 volts.

Gate Vgs : 0➔-6 volts for p channel at steps of -0.6 volts.
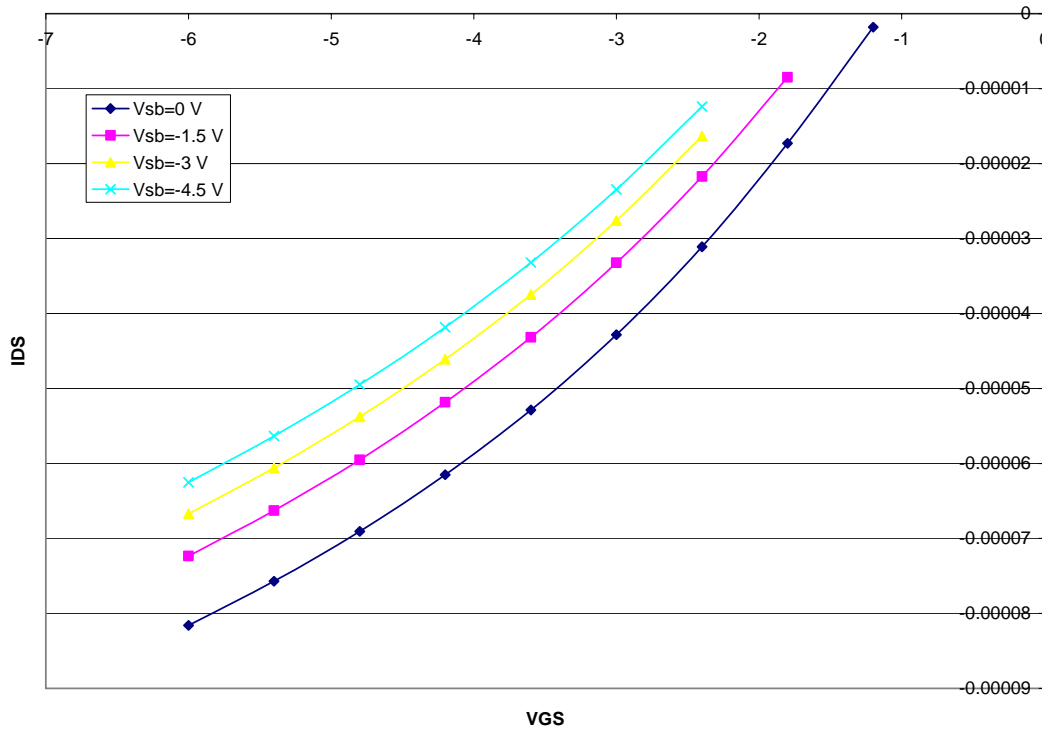
Figure 1 :   Drain Current Vs. gate-bias voltage for P-channel MOS

Figure 2 gives Ids versus Vds for several values of Vgs. In addition for each Vgs three

values of Vsb were taken (0, -2 and -5 volts).

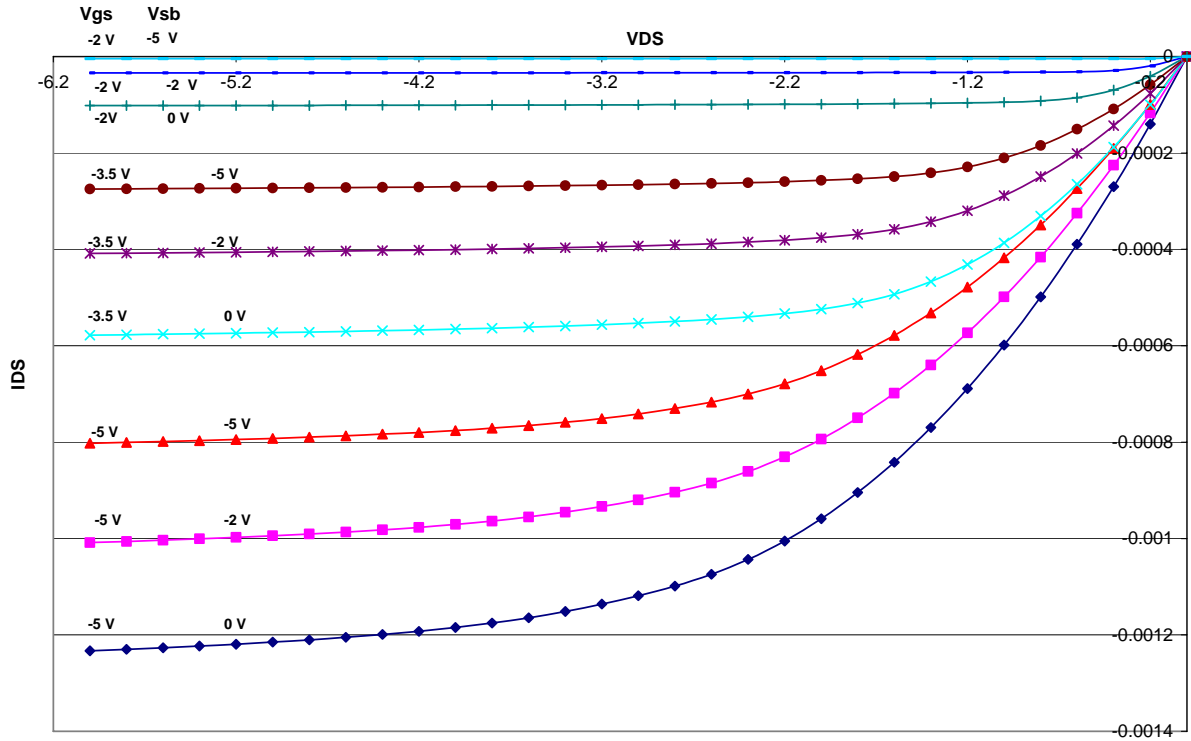**Figure 2:   Ids vs. Vds for P-channel MOS**

For Vds > - 2 Volts the average error is 7.2%.
For - 2 > Vds > - 4 Volts the average error is 9.2%.
For Vds < - 4 Volts the average error is 9.1%.

- **Transient Analysis:**

Transient analysis is done by giving pulse of 4.0 volt amplitude with rise time & fall time of 0.1 ns. The width and period of the pulse are 2 ns and 4 ns respectively. Figure 3 shows the .tran2 analysis of P- channel MOS.
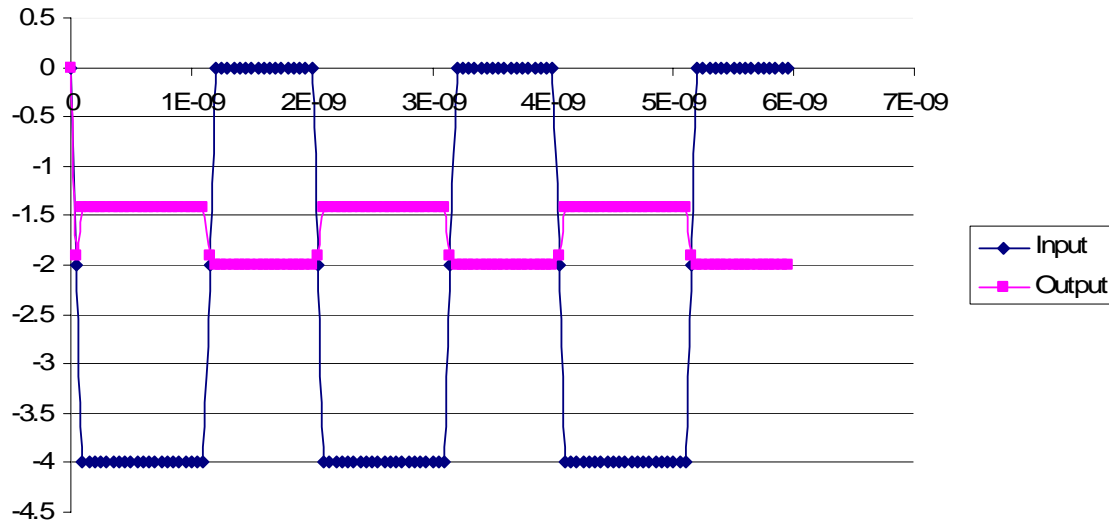

Figure 3: **.tran2 analysis for P-channel MOS**

Known Bugs:

None.

Credits:

Name	Affiliation	Date	Links
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