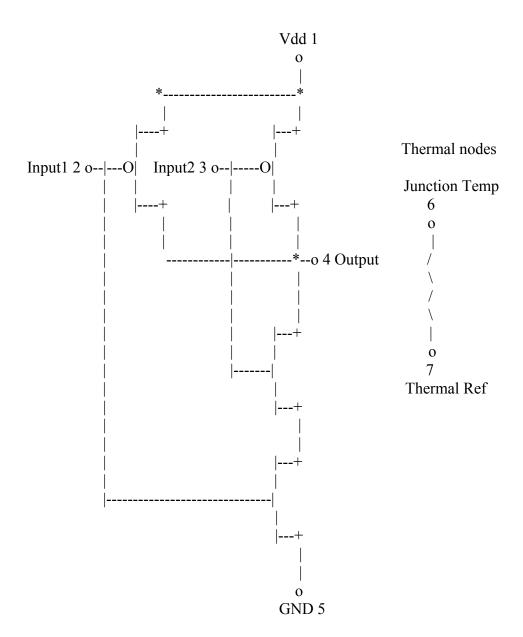
CMOS NAND Gate with Junction temperature



Authors:

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Description:

This element implements a generic CMOS NAND gate and calculates junction temperature.

Form: moscnandt: <instance name> n_1 n_2 n_3 n_4 n_5 n_6 n_7 <parameter list> instance name is the model name

 n_1 is the NAND element Vdd node,

 n_2 is the NAND element input 1 node,

 n_3 is the NAND element input 2 node,

 n_4 is the NAND element output node,

 n_5 is the NAND element Ground node,

 n_6 is the NAND element Junction temperature node,

 n_7 is the NAND element Thermal Reference node.

Parameters:

| Parameter | Type | Default value | Required? |
|--------------------------------------|--------|---------------|-----------|
| vtn: NMOS threshold | DOUBLE | 1 | no |
| voltage (V) | | | |
| vtp: PMOS threshold | DOUBLE | -1 | no |
| voltage (V) | | | |
| un: effective mobility of | DOUBLE | 500 | no |
| electrons in NMOS | | | |
| (cm ²)/(V-sec) | | | |
| up: effective mobility of | DOUBLE | 200 | no |
| holes in PMOS (cm ²)/(V- | | | |
| sec) | | | |
| en: permittivity of gate | DOUBLE | 34.515e-14 | no |
| insulator in NMOS (F/cm) | | | |
| ep: permittivity of gate | DOUBLE | 34.515e-14 | no |
| insulator in PMOS (F/cm) | | | |
| tox: thickness of gate | DOUBLE | 2e-6 | no |
| insulator (cm) | | | |
| wn: channel width of | DOUBLE | 50e-6 | no |
| NMOS (cm) | | | |
| ln: channel length of | DOUBLE | 2e-6 | no |
| NMOS (cm) | | | |
| wp: channel width of | DOUBLE | 100e-6 | no |
| PMOS (cm) | | | |
| lp: channel length of | DOUBLE | 2e-6 | no |
| PMOS (cm) | | | |
| td: response delay time | DOUBLE | 0 | no |
| (sec) | | | |

| thermal: thermal element | BOOLEAN | False | no |
|----------------------------|---------|-------|----|
| flag | DOLIDLE | 200 | |
| tnom: nominal temperature | DOUBLE | 300 | no |
| (K) | | | |
| zt: thermal impedance | DOUBLE | 310 | no |
| summation (K/W) | | | |
| c1: PMOS GS capacitance | DOUBLE | 1e-12 | no |
| (F) | | | |
| c2: NMOS GS capacitance | DOUBLE | 1e-12 | no |
| (F) | | | |
| c3: output GS (Miller) | DOUBLE | 1e-12 | no |
| capacitance (F) | | | |
| c4: parasitic diode | DOUBLE | 1e-12 | no |
| capacitance from output to | | | |
| Vdd (F) | | | |
| C5: parasitic diode | DOUBLE | 1e-12 | no |
| capacitance from output to | | | |
| Ground (F) | | | |
| freq: operating frequency | DOUBLE | 1e6 | no |
| (Hz) | | | |
| lk: leakage current (A) | DOUBLE | 8e-6 | no |

Example: moscnandt:nand 1 2 3 4 0 1000 "tref"

Model Documentation: (Start on a new page, Include English and make sure font sizes are consistent. Use figures if necessary. Please avoid using scanned image.)

MOSFET cutoff current I_{ds} , for $V_{gs} < V_t$:

$$I_{ds} = 0$$

MOSFET current factor β:

$$\beta = \mu * C_{ox} * (W/L)$$

MOSFET linear current I_{ds} , for $V_{gs} - V_t > V_{ds} > 0$:

$$I_{ds} = \beta * (V_{gs} - V_t - (V_{ds}/2)) * V_{ds}$$

MOSFET saturation current I_{ds} , for $V_{ds} > V_{gs}$ - $V_t > 0$:

$$I_{ds} = (\beta/2) * (V_{gs} - V_t)^2$$

Power dissipation P_D:

$$P_D = (V_{sd,pmos} * I_{sd,pmos}) + (V_{ds,nmos} * I_{ds,nmos}) + (2 * freq * C * V_{dd}) + leakage$$

Junction temperature T_j:

$$T_i = T_{ambient} + (P_D * \theta_{iA})$$

References:

1. Mazen M Kharbutli. fREEDA element moscnand. DEFAULT ADDRESS"elements/Moscnand.h.html"

Sample Netlist:

- * DC thermal CMOS NAND Test
- * DC sweep input voltage from 0 to 5V

.dc sweep="vsource:Vin" start=0 stop=5 step=0.1

.options iniTmp=300

.ref "tref"

vsource:Vdd 1 0 vdc=5

vsource:Vin 2 0

vsource:Vdd2 3 0 vdc=5

moscnandt:nand 1 2 3 4 0 1000 "tref" thermal=1

res:R 4 0 r=1000000

***thermal circuit

res:R1 1000 1001 r=6e3

vsource:t1 1001 "tref" vdc=iniTmp cap:c1 1000 1001 c=1e-12

.out plot term 4 vt in "nand_voltage.out"
.out plot element "moscnandt:nand" 4 ut in "nand_temperature.out"
.out plot element "moscnandt:nand" 0 it in "nand_current.out"

.end

Validation:

This thermal CMOS NAND model adds thermal junction temperature calculation to the existing electrical CMOS NAND model (moscnand). Simulations were performed using the existing moscnand model in a netlist with a DC sweep from 0 to 5 Volts at the one input terminal. The second input terminal was connected to a DC voltage source of 5V. The resulting output voltage and current was recorded. The thermal CMOS NAND model (moscnandt) was validated by making a new netlist with the moscnandt model. The resulting moscnandt voltage output and current output was compared to those of the original moscnand model and identical electrical results were obtained. The resulting moscnandt junction temperature data was empirically verified by correlating junction temperature data points with manually calculated results.

The original moscnand model uses a default parameter of wp = 50e-6 cm (channel width of PMOS). If this default parameter is used an erroneous element current output results. The moscnandt model uses a default parameter of wp = 100e-6 cm, resulting in an expected element current output.

Known Bugs:

None.

Credits:

Name Affiliation Date Links

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