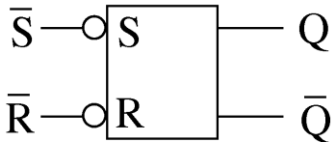
CMOS S-R Nand Latch cmoslatchsrnand



Description:
This is an Intrinsic Super Element which models a nand gate based S-R latch.

Form: cmoslatchsrnand:<instance name> *n1 n2 n3 n4 n5 n6* <parameter list>

n1 is the high voltage source (Vdd) terminal,
n2 is $\overline{S}$ terminal
n3 is $\overline{R}$ terminal,
n4 is Q terminal,
n5 is $\overline{Q}$ terminal,
n6 is the ground or Vss terminal

Parameters:

Parameter	Type	Default Value	Required
ln: Channel Length of NMOS (m)	TR_DOUBLE	1.0e-6	No
wn: Channel Width of NMOS (m)	TR_DOUBLE	1.0e-6	No
lp: Channel Length of PMOS (m)	TR_DOUBLE	1.0e-6	No
wp: Channel Width of PMOS (m)	TR_DOUBLE	1.0e-6	No

Example:
cmoslatchsrnand: srlatch 1 2 3 4 5 0

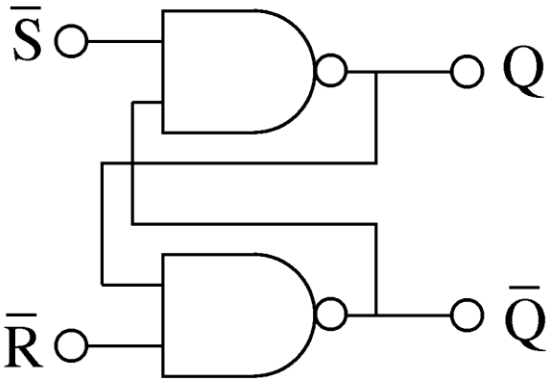
Notes:
This implementation of SR latch is based on nand gate

Known Bugs:
No known bugs.

Truth Table
The latch is based on following truth table:

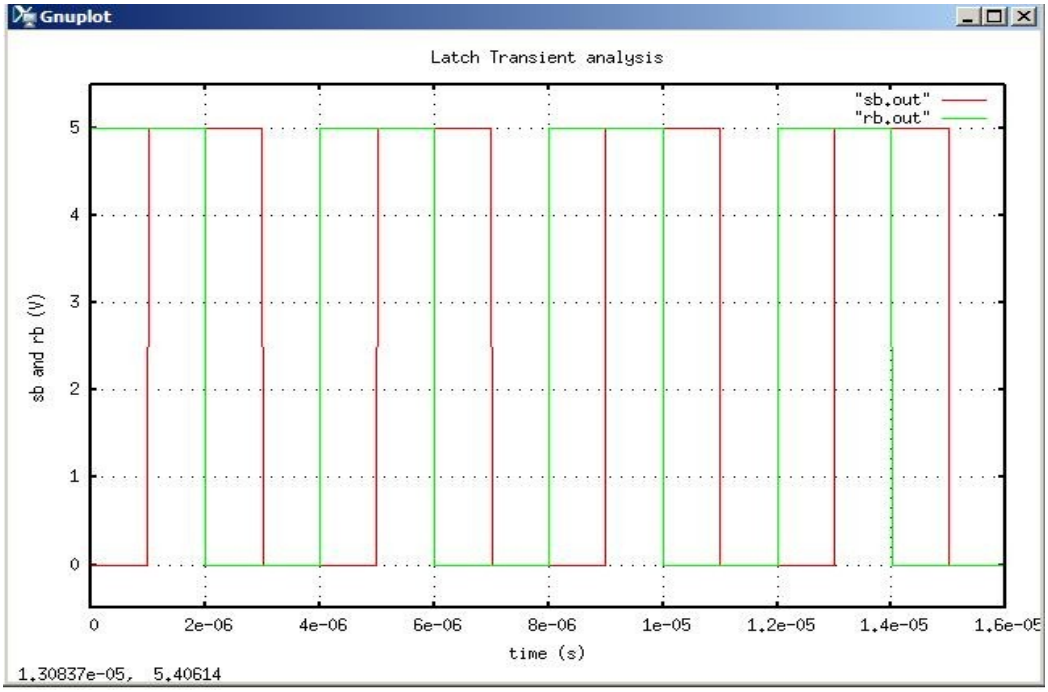
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	Operation
0	1	1	0	Set
1	0	0	1	Reset
1	1	H	H	Hold the previous values
0	0	1	1	Restricted combination

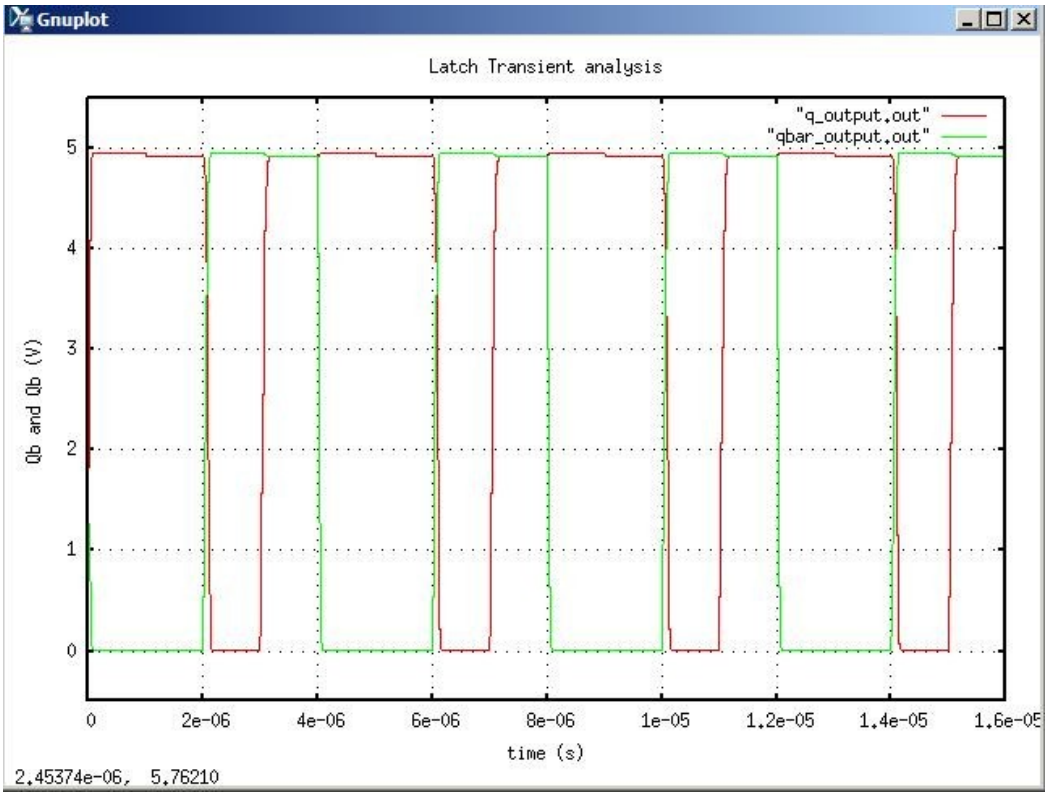
Schematic
Following is the schematic of latch:



Sample Netlist:
*** Nand based SR Latch
* **This netlist is for Transient Analysis of Nand based SR Latch***
.tran2 tstop=16e-6 tstep=10e-9
vpulse:Vin2 2 0 v1=0 v2=5 td=1e-6 per=4e-6 pw=2e-6 tr=0.005e-6 tf=0.005e-6
vpulse:Vin5 5 0 v1=0 v2=5 per=4e-6 pw=2e-6 tr=0.005e-6 tf=0.005e-6
****** Vdd Connection
vsource:Vdd 1 0 vdc=5
****** Instantiation
cmoslatchsrnand:latch 1 2 5 4 3 0
*** Load Resistance and Capacitance
r:R1 4 0 r=1000000
r:R2 3 0 r=1000000
.options gnuplot
.out plot term 2 vt in "sb.out"
.out plot term 5 vt in "rb.out"
.out plot term 4 vt in "Q_output.out"
.out plot term 3 vt in "Qbar_output.out"

Validation:
The output graph from the above netlist is shown below:





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