

Figure 1: Equivalent Circuit Model

Description:

This element implements a thin film transistor based on a-Si:H HP model

Non-Charge Conserving model:

Form: mosntft: <instance name> n1 n2 n3 <parameters>

<instance name>: instance of the model

n1 is the drain element node,

n2 is the gate element node,

n3 is the source element node

Charge conservation model:

Form: mosntft:<instance name> n1 n2 n3 n4 <parameters>

n1 is the drain element node,

n2 is the gate element node,

n3 is the source element node,

n4 is the bulk element node.

Equations:

The threshold voltage:

$$V_{TH} = V_{T0} + \eta . V_{DS}$$

The linear current equation: (Vgs > Vth)

$$I_{DS} = \frac{W}{L} * \mu_{eff} * C_{fm} \left[\left(V_{GS} - V_{T0} - \eta V_{DS} \right) V_{DS} - \frac{V_{DS}^2}{2.0} \right]$$

$$V_{\text{TH}}^{\text{eff}} = V_{\text{TH}} + \nu \cdot \left(V_{\text{GS}}^{\psi} - \frac{V_{\text{DS}}^{\psi}}{2.0}\right) \cdot \exp\left[-\frac{q \cdot V_{x}}{k \cdot T_{\text{DEV}}} \cdot \log(t_{vst})\right]$$

The saturation current: (Vds > Vgs - Vth)

$$I_{DS}^{sat} = I_{DS}. \frac{v_{sat}.L}{(1.0 + V_{DS})\mu_{eff}}$$

The sub-threshold current: (Vgs < Vth)

$$I_{DS}^{subth} = I_{DS}.exp \left(\frac{V_{GS} - V_{TH}^{eff}}{xn.vt} + 1.0 \right)$$

$$von = V_{TH}^{eff} + \eta.V_{DS} + xn.vt$$

$$xn = 1.0 + \frac{q.N_{FS}.L.W}{C_{fm}}$$

The off current is given by: (Vgs < 0)

$$I_{DS}^{off} = I_{DS}^{subth} + g_o.(V_{GS} + D_{eff}.V_{DS})$$

In case of the model which does not conserve charge, The capacitance values are given by the equations:

$$C_{\text{MISIW}} = \frac{C_{\text{fm}}.C_{\text{SC}}}{C_{\text{SC}} + C_{\text{fm}}}.L.W$$

$$C_{\text{GSI}} = C_{\text{MIS}}.\left[1.0 - \frac{V_{\text{DS}}^2}{12.0*(2.0.V_{\text{GS}} - 2.0.V_{\text{TH}}^{\text{eff}} - V_{\text{DS}})^2}\right]$$

$$C_{\text{GDI}} = C_{\text{MIS}}.\left[0.5 - \frac{2.0.V_{\text{DS}}(2.0.V_{\text{GS}} - 2.0.V_{\text{TH}}^{\text{eff}} - V_{\text{DS}}) + V_{\text{DS}}^2}{6.0*(2.0.V_{\text{GS}} - 2.0.V_{\text{TH}}^{\text{eff}} - V_{\text{DS}})^2}\right]$$

To ensure charge conservation, terminal charges are used as state variables along with terminal voltages. The terminal charges are given by:

$$\begin{aligned} Q_G &= C_K(V_{GS} - V_{3t}) \frac{1 - a^{(1 + \frac{2}{kt})}}{\left[1 + \frac{k_t}{2}\right] \left[1 - a^{\frac{2}{kt}}\right]} \\ Q_D &= -C_K(V_{GS} - V_{3t}) \left[\frac{1 - a^{(1 + \frac{2}{kt})}}{\left[1 + \frac{k_t}{2}\right] \left[1 - a^{\frac{2}{kt}}\right]^2} - \frac{1 - a^{(1 + \frac{4}{kt})}}{\left[2 + \frac{k_t}{2}\right] \left[1 - a^{\frac{2}{kt}}\right]^2} \right] \\ Q_S &= -C_K(V_{GS} - V_{3t}) \left[\frac{-a^{\frac{2}{kt}} \left[1 - a^{(1 + \frac{2}{kt})}\right]}{\left[1 + \frac{k_t}{2}\right] \left[1 - a^{\frac{2}{kt}}\right]^2} - \frac{1 - a^{(1 + \frac{4}{kt})}}{\left[2 + \frac{k_t}{2}\right] \left[1 - a^{\frac{2}{kt}}\right]^2} \right] \\ a &= \frac{V_{GS} - V_{3t}}{V_{DS} - V_{3t}} \\ C_K &= WLC_1 \frac{1}{1 + \frac{5V_1}{2}V_2} \end{aligned}$$

The net currents at the gate, drain and source:

$$I_{G}(t) = \frac{dQ_{G}(t)}{dt}$$

$$I_{D}(t) = I_{DS}(t) + \frac{dQ_{D}(t)}{dt}$$

$$I_{S}(t) = -I_{DS}(t) + \frac{dQ_{S}(t)}{dt}$$

Non-charge conservation model:

Parameters:

Parameter	Type	Default Value	Required
Description			
Length (L)	Double	11 μ m	No
Width (W)	Double	41 μ m	No
Mobility (μ ₀)	Double	$0.450 \text{ cm}^2/\text{Vs}$	No
Threshold voltage	Double	1.699 V	No
(V_{TO})			
Potential Barrier	Double	0.620 V	No
(ϕ)			
Density of States	Double	$1.925 \times 10^{21} \text{ cm}^{-2}$	No
(N_{FS})			
Saturation Velocity	Double	2783 m/s	No
(V _{sat)}			
Mobility Reduction	Double	17.8mV ⁻¹	No
(θ)			
Static feedback	Double	410.8	No
effect (η)			
Film Thickness (T1)	Double	300nm	No
Film Thickness (T2)	Double	0	No
Dielectric Constant	Double	3.9	No
<i>E</i> 1			
Dielectric Constant	Double	0	No
<i>E</i> 2			
Conductance (g0)	Double	9.728x10-15 Ω	No
Tref	Double	1.5	No
Overlap	Double	52.03fF	No
Capacitance (CGS0)	- 11	10.01.75	
Overlap	Double	42.21fF	No
Capacitance			
(CGD0)	D 11	150.05/	N
CSC	Double	158.8F/m	No
RD	Double	8030 K	No
RS	Double	8030 K	No
Frequency (f)	Double	100 KHz	No
DEFF	Double	1.968	No
Relaxation time (τ)	Double	10.7ns	No

fEFF	Double	0.302	No
Empirical factor v	Double	0.0008	No
Empirical factor ψ	Double	0.2	No
Vx	Double	0.033 V	No
Voltage Supply	Double	100ms	No
time (t _{vst})			
TNOM	Double	300.15 K	No

Example: mosntft m1 1 2 0 1=11u w=41u

Charge-conserving model

Parameters:

Parameter	Type	Default Value	Required
Description			_
Length (L)	Double	5.5 μ m	No
Width (W)	Double	80 μ m	No
Mobility (μ ₀)	Double	$0.124 \text{ cm}^2/\text{Vs}$	No
Threshold voltage (V_{TO})	Double	3.2 V	No
Threshold Voltage (V _{THM)}	Double	4.2V	No
Beta	Double	3.0V ⁻¹	No
Lambda (\(\lambda\)	Double	450V	No
c_{TR}	Double	0.06	No
$R_{\rm off}$	Double	4T	No
Overlap	Double	80fF	No
Capacitance (CGS0)			
Overlap	Double	80fF	No
Capacitance			
(CGD0)			
RD	Double	83 K	No
RS	Double	83 K	No
cl	Double	400e-6	No
Characteristic Temp (TTS)	Double	232 K	No

Example:

mosntft:m1 1 2 0 0 l=11u w=41u

Model Documentation

The model is based on a-Si:H HP model equations. The original model suggested by Hitoshi Aoki does not conserve charge. Khakzar and Leuder suggested a charge-conserving model. This model has improved dynamic and transient behavior. The static device operation is governed by a set of current equations in every region of operation. The transfer and forward bias characteristics of the thin-film transistor closely match the MOS3 model. Hence a lot of the curve-fitting equations were adopted from the MOS3 model. The a-Si TFT has significant sub-threshold and leakage current, which is not seen in ordinary CMOS transistors. The optical and electrical measurements of the thin-film transistor suggest that, the dominant transport mechanism is through gap assisted tunneling process. The energy-band diagram shows the existence of localized states in the band-gap. The localized states increase the threshold voltage.

The non-charge conserving model is an AdolcElement, while the charge-conserving model, is a NAdolcElement. The NAdolcElement class allows specifying charge as a state-variable and obtaining its derivative. The threshold voltage depends on the voltage stress, Vds, Vgs.

This model is generally the level 16 MOS model in SPICE.

References:

- [1] Dynamic Characterization of a-Si TFT-LCD Pixels Hitoshi Aoki
- [2] Level 40 HP a-Si TFT Model Star-Hspice Manual
- [3] Modeling of Amorphous-Silicon Thin-Film Transistor for Circuit Simulations with SPICE Karim Khakzar and Ernst H. Leuder
- [4] An investigation of the Charge Conservation Problem for MOSFET Circuit Simulations Ping Yang, Berton D. Epler and Pallab K. Chatterjee
- [5] Transient Analysis of MOS Transistors Soo-Young Oh, Donald E. Ward, Robert W. Dutton
- [6] Physics of amorphous silicon based alloy field-effect transistors M. Shur and M. Hack

Sample Netlist:

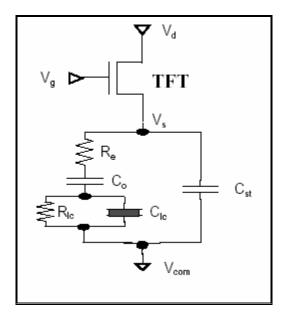


Figure 2: Test Circuit - LCD Driver Here Re=1.29Kohm, Co=317fF, Rlc=10GOhm, Cst=10.06pF

**** a-Si TFT-lcd driver circuit *****

vpulse: vdd 2 0 v1=1 v2=11 td=0 tr=10us tf=10us pw=200us per=400us vpulse: vgs 4 0 v1=0.5 v2=20 td=0 tr=10us tf=10us pw=20us per=170us

nmos16:m1 2 4 3 3

res:re 3 5 r=1.28e3 c:co 5 6 c=317e-15

res:rlc 6 0 r=10e9 LCCapacitor:clc 6 0 C:cst 3 0 c=10e-12

.tran2 tstep=10u tstop=800u gcomp=0

.out plot term 4 vt in "nmos-vg.out" .out plot term 2 vt in "nmos-vd.out" .out plot term 3 vt in "nmos-vs.out" .end

Validation:

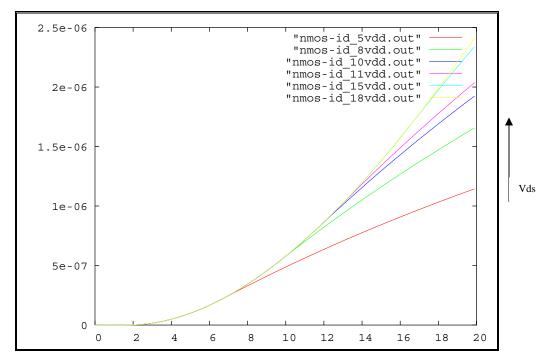


Figure 3: Id-Vgs Curve : fREEDA

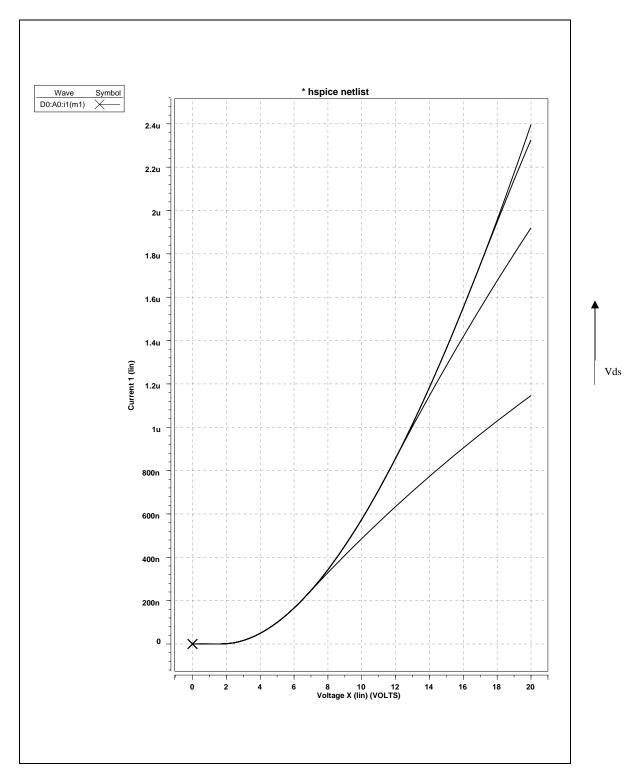


Figure 4: Vgs-Id - HSpice Output

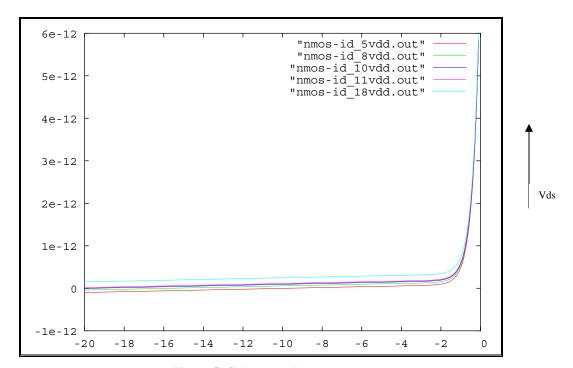


Figure 5: Subthreshold current

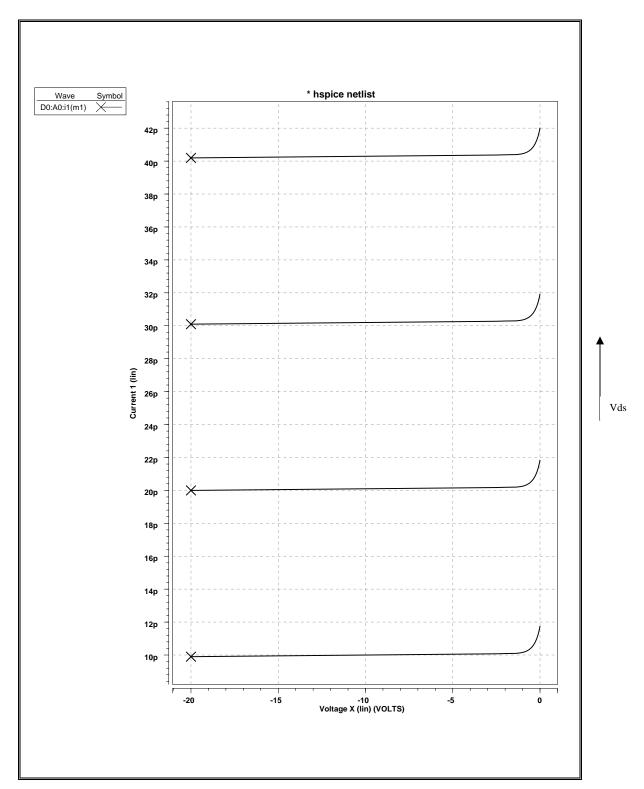


Figure 6: Subthreshold current - Hspice Output

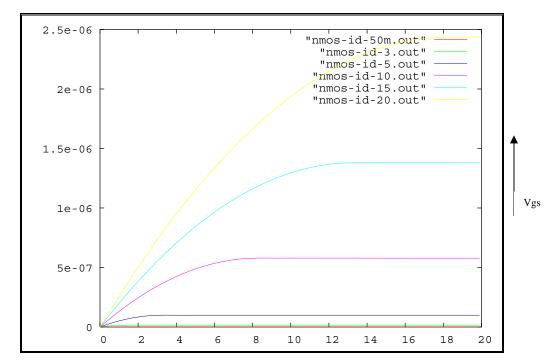


Figure 7: Transfer Curve – fREEDA

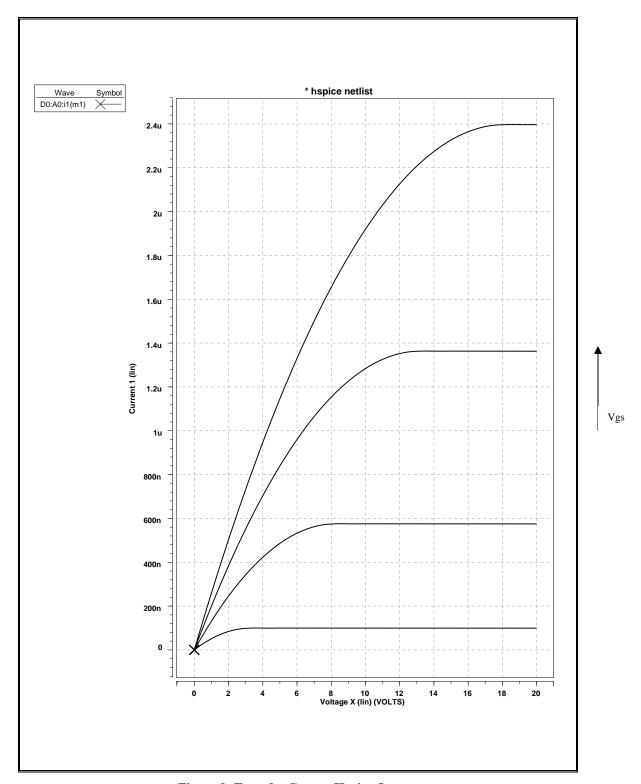


Figure 8: Transfer Curve - Hspice Output

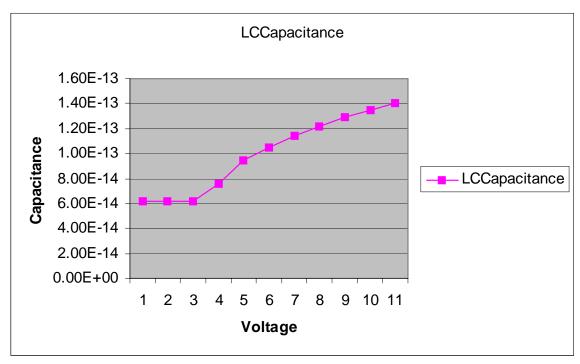


Figure 9: Capacitance of the LC capacitor with bias voltage.

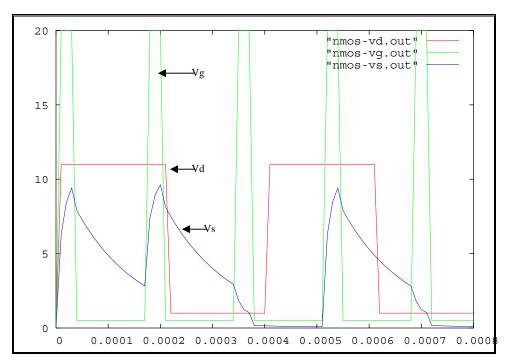


Figure 10: Output of LCD driver without charge convservation

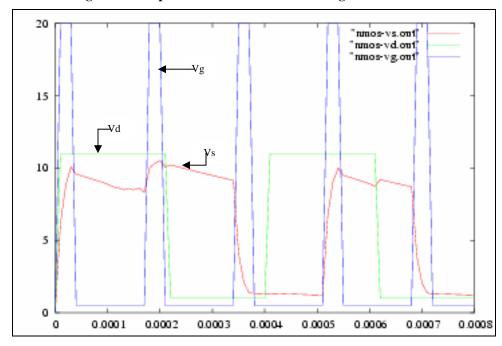


Figure 11: Output of LCD driver with charge conservation

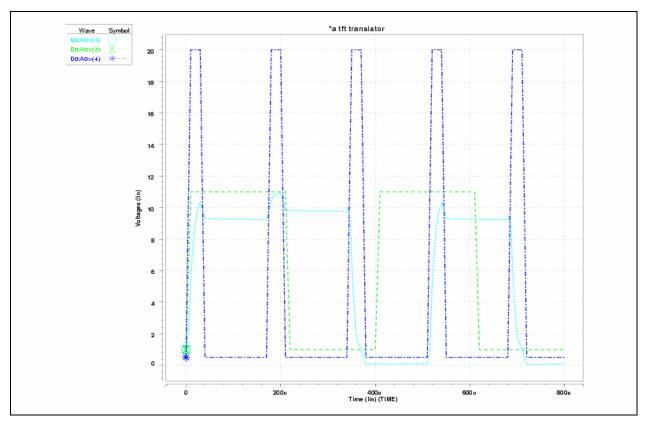


Figure 12: Hspice Output of LCD driver

Known Bugs:

- 1. The temperature dependence equations are not implemented.
- 2. The source and drain resistances must be explicitly given in the netlist for proper transient behavior.

Credits:			
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Notes:

A Thin Film Transistor model based on the HP a-Si:H device was implemented in the circuit simulator fREEDA. In [1] Hitoshi provided the Spice parameters extracted using IC-CAP. This paper also explains the device operation and the device equations.

Since this model does not conserve charge, a a-Si TFT model using the charge equations given by Khakzar and Leuder[3] was implemented too. This modified model significantly improved the dynamic and transient behavior of the device. The model is simulator independent and the same model can be used for DC and transient analysis. A a-Si NMOS thin film transistor was implemented. The model was used in a simple netlist to drive a single LCD pixel and its transient behavior was studied. To test the LCD driver circuit a liquid crystal capacitor (see lccapacitor) was implemented too.

Amorphous silicon based alloy (a-Si) field effect transistors have emerged as a viable and important technology for large area, low cost integrated circuits. These circuits are currently being used to drive large area liquid crystal displays and have good potential for basic integrated circuits (IC's) and addressable image sensing arrays.

These IC's require powerful tools for the design and optimization in order to reduce the costs and save time. Several authors have already reported on a-Si H-TFT models, which could be incorporated into circuit simulation programs. The static and dynamic analysis of Shur [6] proposed two exponential regions for the tail states and the deep states. But these models do not include the effects of surface states or analytic expressions for the temperature dependency of the current-voltage characteristics. In addition, the model for the dynamic transient analysis cannot guarantee charge conservation, which is especially required for circuits with high impedance nodes.

In [3] Khakzar and Leuder present a model, which incorporates a charge-conserved model, which is appropriate for calculating the static and dynamic behavior of the TFT.

A charge-conserving model for amorphous silicon thin-film transistors was implemented. The simulated current-voltage characteristics show good agreement with Spice results. The charge-conserved model was used to simulate a driver circuit for an LCD pixel. This simulation was compared with a circuit generated by using another model, which did not conserve charge. The graphs show the importance of charge conservation.