Discrete-Time Quasi Sliding Mode Control of Single-phase T-type Inverters for Residential PV Applications

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***Abstract*—This research focuses on improving the performance of single-phase grid-connected DC/AC converters, which is intensively used in PV systems. First, the single-phase T-type topology which offers more voltage level than the conventional H-bridge is used to lower the total harmonic distortion (THD) of the output current. Second, the quasi-sliding mode control in combination with a lump disturbance compensation is used for the current control loop. This approach guarantees that the output current quickly tracks its reference in a few sampling cycles despite the existence of the modeling error. Finally, a DC bus voltage controller with a discrete-time notch filter that exactly extracts the average DC bus voltage from the second harmonic ripple is designed. The proper design of the notch filter plays a key role not only in the improvement of the DC bus voltage control-loop but also in the reduction of the overall THD of the line current. The validity of the proposed solution is verified by numerical simulation using Matlab/Simulink.**

***Keywords*—T-type inverter, grid connected, PV, discrete-time control.**

I. Introduction

Along with the increasing of the world's power demand and the depletion of the fossil energies, the role of renewable energy such as solar is more and more important. With huge government supports, the worldwide cumulative installed capacity of the photovoltaic (PV) energy has grown substantially over the last two decade, not only in large scale, i.e, solar farm, but also in small scale, i.e, residential PV systems.

To effectively utilize solar energy, photovoltaic and two-stage converter are normally used. The first stage is usually a DC/DC converter that performs maximum power point tracking (MPPT) and converts the DC voltage of the PV to an appropriate level which is then utilized by the second stage. In most cases, the second stage is a DC/AC converter which regulates the DC link voltage as well as control the flow of both active and reactive power to the grid smoothly. Recently, the single-phase grid-connected inverters are an interest of the solar market since they suit well the residential PV applications where the power range is $1kW \div 10kW$. Instead of using a low-frequency galvanic isolation transformer at the DC/AC stage, the topology with a high-frequency transformer at DC/DC stage which exhibits several advantageous features such as lower cost, lighter weight, smaller volume, and higher efficiency are commonly used for the above-mentioned power range [2]. Currently, PV inverters manufactured by companies such as REFU, SMA, Conergy, Danfos Solar, and Sunways are available in the market. The maximum efficiency of these inverters are up to 98% which satisfies the European standard. The topologies employed for the grid connected converter are mainly based on H-bridge and neutral point clamped (NPC) family [1]. Among which, the H-bridge topology is commonly used because of its bi-directional power transfer feature which is vital in small capacity PV systems due to the existence of backup batteries [2]. However, the main issues of grid-connected converters do not come from the topology, but mostly from the control system perspective.

In order to connect to grid, certain requirements of the Grid code, which guarantees the stable and secure operation of the power system network, must be fulfilled such as: variation in voltage and frequency range, harmonic currents (order-h) limits, maximum current total harmonic distortion (THD), DC current injection [4]. To satisfy the above mentioned standard, many solutions have been developed for the grid-connected inverter and mainly focus on control techniques [3]. In general, the PV inverter control system consists of two cascaded loops. In which, the inner loop is a grid current controller that regulates the injected active and reactive power to the grid, while the outer loop stabilizes the DC link voltage of the inverter by balancing the power flow between the grid and the PV system. Among the two above mentioned control loops, the inner current loop controller plays a key role in improving dynamic performance and harmonic compensation in the case of weak and distorted grid. Hence, great effort has been made for the current controller design. In order to utilize the conventional proportional-integral (PI) controller which is familiar with most researchers, voltage oriented control, in which synchronous rotating dq reference frame that not only transforms all sinusoidal quantities into constants but also

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decouple active and reactive power, is employed. Although the control design is simple in this case, the transient response of the control system is poor due to the limited bandwidth of the PI controller as well as the coupling between the direct and quadrature current controllers. To remove the coupling effect mentioned above, the proportional-resonant (PR) is used where the control design is carried out in static $\alpha\beta$ reference frame [5]–[8]. By utilizing the high gain of the PR controller at its resonant frequency, the steady-state current error is eliminated despite the fact that the reference grid current is sinusoidal. Even though, the transient performance is not much improved due to the existence of a second-order generalized integrator (SOGI) [9] in the transformation. Advanced control techniques such as sliding mode control (SMC) [10], [11] is also employed to improve the inner current loop performance. As pointed out in [10], the conventional SMC can not achieve good tracking performance in the case of modeling error due to the drift of the sliding surface. Hence, additional modifications such as multiple resonant sliding surface [10] and double band hysteresis [11] are proposed. Even though, the design in continuous-time domain is not convenience to be implemented as well as evaluated in digital platform. Another factor which strongly affects the THD of the output current is the existence of the second harmonic ripple across the DC bus voltage. Improper DC bus voltage control design may result in polluted output current since the reference of the inner current loop is computed by the outer DC loop. Various solutions have been stated in [12] and its references, mainly based on the conventional PI controller in combination with a notch filter to reject the ripple frequency. In most case, the dynamic response is slow due to the reduced bandwidth of the controller while the tuning procedure of the PI controller is not really clarified.

In this research, a combine solution is proposed to cope with all above mentioned problems of the grid-connected inverter in residential PV application. First, the T-type topology, which offer more voltage levels in comparison with its conventional H-bridge counterpart, is employed for the inverter. Second, a simple but very effective discrete-time quasi-sliding mode control (DQSMC) in combination with a lump disturbance estimation (LDE) is used to achieve fast tracking the AC current. Finally, a very simple but effective design of the PI controller and the notch filer in discrete-time domain are carried out to guarantee the stability of the DC bus voltage. It should be noted that all the controllers are designed in discrete-time domain and does not require any coordinate transformation, which may affect the dynamic performance of the system.

To this end, the paper is organized as follows. The system description is shown in section II. The control design is carried out in section III. The simulations implemented by Matlab/Simulink is presented in section IV. The last section shows the conclusions.

II. System Description

The block diagram of our developed PV system is shown in Fig. 1 that consists of PV modules, DC/DC converters, a backup-battery and the T-type converter which regulates the DC bus voltage by balancing the power flow. Suppose that the pulse width modulation (PWM) technique is used, the behavior of the converter in grid-connected mode can be described by the following equations

$$L\frac{di_L(t)}{dt} = u_s(t) - R_L i_L(t) - mU_{dc} \tag{1}$$

$$C\frac{dV_{dc}(t)}{dt} = mi_L(t) - i_o(t) \tag{2}$$

where $u_s(t)$, $i_L(t)$ and $i_o(t)$ are line voltage, inductor current and load current of DC side, respectively. The passive components are inductor L, resistor R_L and DC bus capacitor C while $-1 \leq m \leq 1$ represents for the modulation index.

Since the control design are carried out in discrete-time domain, the following equations, which are derived from (1) and (2) by applying the Forward-Euler with sampling time T_s, are employed.

$$i_{L,k+1} = \left(1 - \frac{R_L}{L}T_s\right) i_{L,k} + \frac{T_s}{L}u_{s,k} - \frac{T_s}{L}V_{dc,k}m_k + p_k \tag{3}$$

$$V_{dc,k+1} = V_{dc,k} + \frac{mT_s}{C}i_{L,k} - \frac{T_s}{C}i_{o,k} \tag{4}$$

where the modeling error p_k is

$$p_k = \left(1 - \frac{\Delta R_L}{\Delta L}T_s\right) i_{L,k} + \frac{T_s}{\Delta L}u_{s,k} - \frac{T_s}{\Delta L}V_{dc,k}m_k \tag{5}$$

III. Control Design

A. Inductor Current Control

The goal of the inductor current controller is to track the AC reference one with best tracking performance under the presence of uncertainties. To achieve this goal, the QSMC with perturbation estimation is adopted as following.

Define the first order sliding variable S_k as

$$S_k = e_k - \lambda e_{k-1} \tag{6}$$

in which the current tracking error e_k is computed by:

$$e_k = i^*_{Lk} - i_{Lk} \tag{7}$$

To obtain the control signal which maintains S_k on the sliding manifold, the following equation is considered:

$$S_{k+1} = 0 \tag{8}$$

which means,

$$i^*_{L,k+1} - i_{L,k+1} - \lambda e_k = 0 \tag{9}$$

By substituting (3) into (9), a simple manipulation gives

$$m_{k,eq} = -\frac{LT_s}{V_{dc,k}}\left[i^*_{L,k+1} - \left(1 - \frac{R}{L}T_s\right) i_{L,k} - \frac{T_s}{L}u_{s,k}\right] - \frac{LT_s}{V_{dc,k}}\left[-p_k - \lambda e_k\right] \tag{10}$$

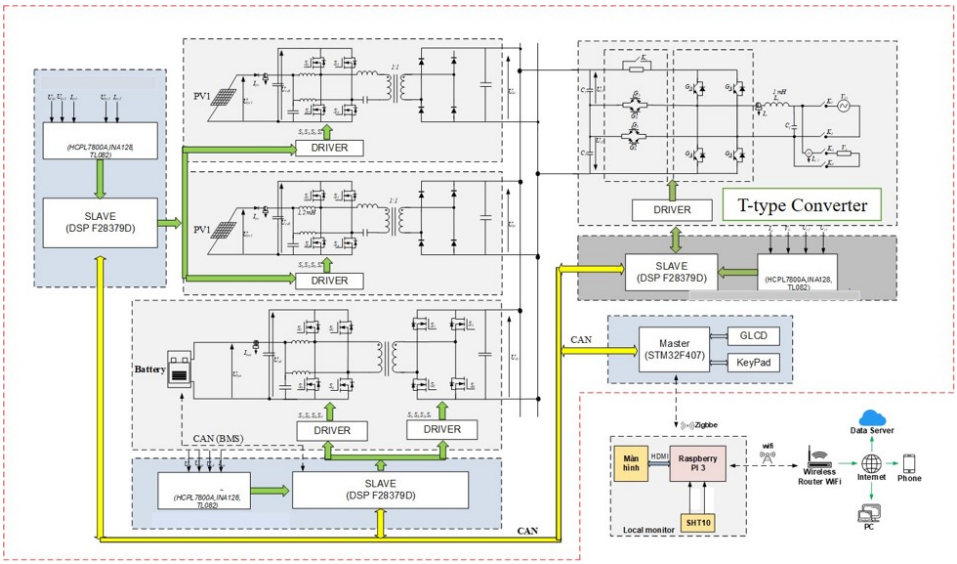

Fig. 1. The block diagram of our developed PV system with backup-battery

By observing (14), it can be realized that this control action is impractical due to the fact that the lump disturbance p_k is unknown. Conventionally, a QSMC needs a switching control action to cope with the unknown p_k following that the chattering is inevitable. In addition, the upper bound of p_k must be known in order to chose the amplitude of the switching control signal.

To cope with the aforementioned problem, a lump disturbance estimation is employed. In detail, it can be deduced from (3) that

$$\begin{aligned} p_k =& i_{L,k+1} - \left(1 - \frac{R_L}{L}T_s\right) i_{L,k} \\ & - \frac{T_s}{L}u_{s,k} + \frac{T_s}{L}V_{dc,k}m_k \end{aligned} \tag{11}$$

Once again, the future inductor current $i_{L,k+1}$ and the control action m_k are unknown at this time instance. Therefore, one-step delay technique is used in this situation based on an assumption that the sampling frequency of the current controller is sufficient high in comparison with the lump disturbance p_k. In fact, this assumption is reasonable since the sampling frequency of the current-loop is as high as the switching frequency of the power converter, i.e., $(3 \rightarrow 10)kHz$. Then, p_k can be approximated by:

$$p_k \approx \hat{p}_k = LPF(p)_{k-1} \tag{12}$$

in which, p_{k-1} is computed by

$$\begin{aligned} p_{k-1} =& i_{L,k} - \left(1 - \frac{R_L}{L}T_s\right) i_{L,k-1} \\ & - \frac{T_s}{L}u_{s,k-1} + \frac{T_s}{L}V_{dc,k-1}m_{k-1} \end{aligned} \tag{13}$$

and LPF is a low pass filter with unity gain. The bandwidth of the LPF has strong influence on the transient response of the control system and need to be well tuned [13].

Based on (12) and (13), the final control action sent to the converter is

$$\begin{aligned} m_k =& -\frac{LT_s}{V_{dc,k}}\left[i^*_{L,k+1} - \left(1 - \frac{R}{L}T_s\right) i_{L,k} - \frac{T_s}{L}u_{s,k}\right] \\ & - \frac{LT_s}{V_{dc,k}}\left[-\hat{p}_k - \lambda e_k\right] \end{aligned} \tag{14}$$

Substitute (14) into (7), it results in

$$e_k = p_k - \hat{p}_k = O(T_s) \tag{15}$$

Equation (15) means that the tracking error is same order with the sampling time T_s, i.e, $e_k = 0$ as $T_s = 0$.

B. Discrete-time Notch Filter Design

By observing (14), it can be realized that the performance of the current controller can be affected by the 2nd-order ripple across the DC bus because the actual value of the DC bus voltage is needed. Hence, an infinite impulse response (IIR) notch filter is chosen to reject the ripple frequency in this research. Define f_{Ns} as the sampling frequency of the discrete-time notch filter, and f_c is the frequency needed to be rejected. Then, a zero transmission at f_c can be achieve by a pair of zeros on unit circle at

$$\Omega = 2\pi\frac{f_c}{f_{Ns}} \tag{16}$$

To control the bandwidth of the filter, a pair of poles on the same frequency as the notch frequency is placed. As a result, the transfer function of the IIR notch filter is

$$H(z) = \frac{(z - e^{j\Omega})(z + e^{j\Omega})}{(z - re^{j\Omega})(z + re^{j\Omega})} \tag{17}$$

in which, $r < 1$ is a parameter which change the bandwidth of the filter.

In this particular application, the grid frequency is $50Hz$ following that $f_c = 100Hz$. To reduce the computational time, the sampling frequency is normally chosen such that $f_{Ns} = 4f_c$ which yields $\Omega = \frac{\pi}{2}$. Consequently, (17) can be rewritten as

$$\begin{aligned} H(z) =& \frac{(z-j)(z+j)}{(z-rj)(z+rj)} \\ =& \frac{1+z^{-2}}{1+r^2z^{-2}} \end{aligned} \tag{18}$$

The response of the notch filter with $r = 0.99$ is illustrated in Fig. 2.

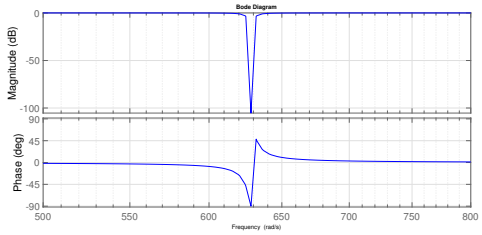

Fig. 2. Bode diagram of the notch filter

C. DC Bus Voltage Control

Define R_{eq} as the equivalent load of the DC bus, then (2) can be rewritten as

$$C\frac{dV_{dc}(t)}{dt} = mi_L(t) - \frac{V_{dc}(t)}{R_{eq}} \tag{19}$$

By applying Forward-Euler to (19), it yields

$$V_{dc,k+1} = \left(1 - \frac{T_s}{R_{eq}C}\right)V_{dc,k} + \frac{T_s}{C}m_k i_{L,k} \tag{20}$$

Suppose that the current controller is perfectly designed and unity power factor is required, then (20) can be represented in grid voltage oriented reference frame as

$$V_{k+1} = \left(1 - \frac{T_s}{R_{eq}C}\right)V_k + \frac{T_s}{C}m_{d,k} i_{Ld,k} \tag{21}$$

By treating the direct axis component $I^*_{Ld,k+1} = m_{d,k}i_{Ld,k}$ as the reference for the inner loop current controller, the transfer function of the voltage loop is

$$\frac{V_{dc,k}}{I^*_{Ld,k+1}} = \frac{\frac{T_s}{C}z^{-1}}{1 - \left(1 - \frac{T_s}{R_{eq}C}\right)z^{-1}} \tag{22}$$

Based on (22), a simple proportional-integral (PI) controller can be designed to stabilize the DC bus in a wide range of the equivalent load $R_{eq,min} < R_{eq} < R_{eq,max}$. The transfer function of the PI controller in discrete-time domain with sampling time T_s, proportional coefficient K_P and integral time constant T_I is

$$W_{PI} = K_P\frac{1 - Dz^{-1}}{1 - z^{-1}} \tag{23}$$

with,

$$D = 1 - \frac{T_s}{T_I} \tag{24}$$

The closed-loop transfer function of the DC bus voltage loop with PI controller is

$$W_{CL} = \frac{b_1K_Pz^{-1} - b_1K_PDz^{-2}}{1 + (b_1K_P - a_1 - 1))\,z^{-1} + (a_1 - b_1K_PD)\,z^{-2}} \tag{25}$$

where $b_1 = \frac{T_s}{C}$ and $a_1 = -\left(1 - \frac{T_s}{R_{eq}C}\right)$ are parameters of (22).

In startup mode, the grid-connected converter always operates in light load condition corresponding to $R_{eq} = R_{eq,Max}$ to charge the DC bus capacitor. The most important criteria in the startup is the overshoot restriction. Otherwise, over voltage may damage the DC link capacitor. In normal operation mode, quick transient response against the sudden change of load is more important. A contradiction between the two mentioned criteria is guaranteed by pole-placement technique where the poles of (25) are placed inside a "nice region" for second order systems as illustrated in Fig. 3. The relation between the desired poles p_1, p_2 and the PI parameters can easily be obtained by

$$\begin{aligned} K_P =& \frac{p_1 + p_2 + a_1 + 1}{b_1} \\ D =& \frac{a_1 - p_1p_2}{b_1K_P} \end{aligned} \tag{26}$$

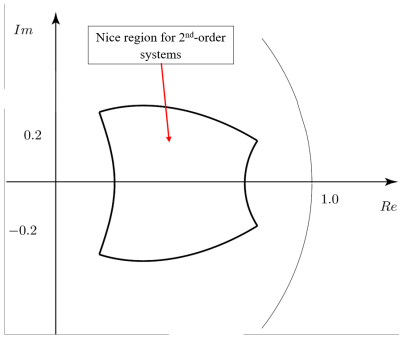

Fig. 3. Nice pole region for 2nd-order systems

In unity power factor condition, the relation between the inductor current $i_{L,k}$ and the direct axis current $i_{Ld,k}$ is

$$i^*_{L,k+1} = i^*_{Ld,k+1}cos\varphi \tag{27}$$

where φ is the phase angle of the grid voltage which is provided by the phase lock loop (PLL). Finally, the block diagram of the proposed grid-connected control system is depicted in Fig. 4.

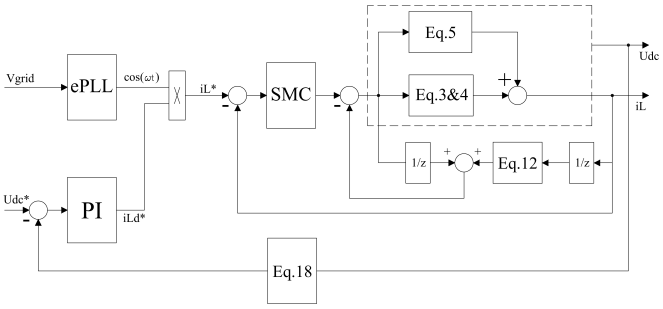

Fig. 4. The block-diagram of the grid-connected control system

IV. Numerical Simulation

To show the effectiveness of the proposed solution, simulations in various complicated scenarios of a 5kW T-type grid-connected converter using Matlab/Simulink are conducted. The parameters of the power converter are provided in Table I. All controllers are implemented by S-Function block using C language which can easily be installed on any digital platforms.

TABLE I. Systems Parameters

L_f	0.84 mH
R_f	0.05 Ω
R_c	0.05 Ω
C_1, C_2	940μF
T_s	100 μs
f_{sw}	10 kHz
λ	0
K_P	0.2695
T_I	0.0149 s

First, the simulation with perfect model is carried out. The starting sequence of the converter is the same as commercial devices. In details, the DC link capacitor is charged via a power resistor in the first $0.04s$ to limit the inrush current. Then, the charging resistor is removed and the T-type converter is activated to regulate the DC bus voltage at $400Vdc$. At time instances $0.14s$ and $0.315s$, commands corresponding to 50% and 100% rated power are sent to the control system. The systems responses are shown in Fig. 5, Fig. 6 and Fig. 7. By observing Fig. 5, it can be realized that the injected current is phase inverse with the line voltage, which means only active power is delivered to the grid. Besides, the performance of the DC bus voltage controller is excellent since it takes only $40ms$ corresponding to two line-cycle to stabilize the voltage when the power is step up from $3.5kW$ to $7kW$. This transient response is much faster than the results achieved in [12]. Besides, the proper design of the discrete-time notch filter perfectly removes the influence of the second order harmonic as seen in Fig. 6.

The key factor to achieve quick response for the DC bus voltage loop is the superior of the current controller where the DQSMC is employed. Since it takes only a few sampling cycles to track the reference current as seen in Fig. 7, the

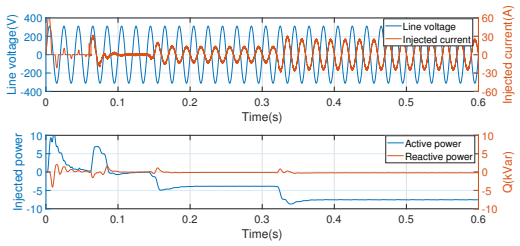

Fig. 5. Injected current and power

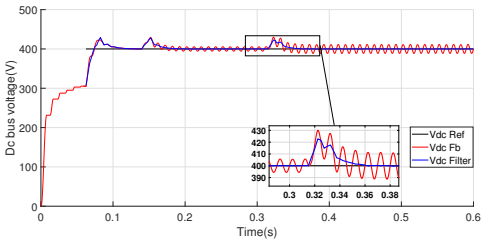

Fig. 6. DC bus voltage controller performance in the case of perfect model

power is instantly delivered to the grid following that the voltage of the DC bus is quickly stabilized.

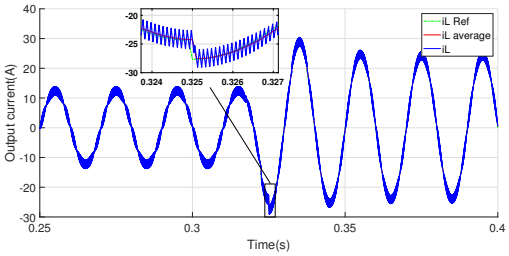

Fig. 7. Inner current controller performance in the case of perfect model

With more voltage level of the T-type topology and an appropriate control strategy, the THD of the output current is 4.25% which satisfies the requirement of the grid code as shown in Fig. 8. It should be noted that same simulation with H-bridge topology results in much higher THD, i.e, 8.02%.

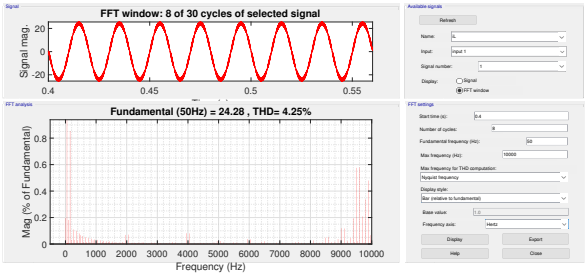

Fig. 8. THD of the injected current with T-type topology

To show the robustness, which is extremely important in practical applications, of the proposed control solution, sim-

ulation with imperfect model where the DC-link capacitors and the output inductor are 10% deviated from their nominal values. Besides, the line voltage is also polluted by several high-order harmonic at time instance $0.415s$. It can be seen from Fig. 9 that the response of the control system is almost not affected by the modeling error. In addition, the THD of the output current is only slightly increased due to the distorted line voltage and the change of the output inductor as illustrated in Fig. 10.

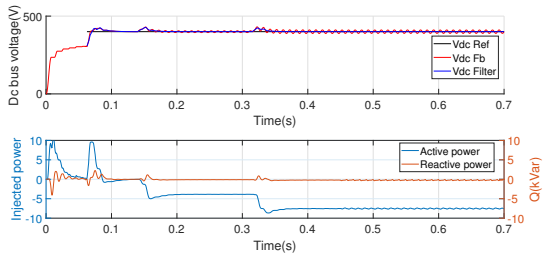

Fig. 9. The transient response of the control system with imperfect model

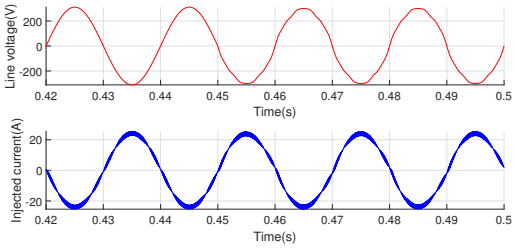

Fig. 10. Distorted line voltage and output current

V. Conclusions

In this research, various solutions are offered to improve the performance of the grid-connected converter used in PV residential applications. Aiming to reduce the THD of the output current, the T-type topology which provides more voltage level than its conventional H-bridge counterpart is employed. Then, various control techniques such as quasi-sliding mode control with lump disturbance estimation, PI control with notch filter are adopted to enhance the tracking performance as well as the robustness of the control system. Numerical simulations using Matlab/Simulink shows that the proposed solution performs well even with $\pm 10\%$ tolerant of the system parameters whilst the THD is 50% reduced in comparison with the conventional H-bridge topology. In addition, the dynamic of the control system is significantly improved. Further experiments are going to be carried out in our future works.

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References

[1] S. B. Kjaer, J. K. Pedersen and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," in IEEE Transactions on Industry Applications, vol. 41, no. 5, pp. 1292-1306, Sept.-Oct. 2005, doi: 10.1109/TIA.2005.853371.

[2] I. Sulaeman, V. Vega-Garita, G. R. C. Mouli, N. Narayan, L. Ramirez-Elizondo and P. Bauer, "Comparison of PV-battery architectures for residential applications," 2016 IEEE International Energy Conference (ENERGYCON), Leuven, 2016, pp. 1-7, doi: 10.1109/ENERGYCON.2016.7514014.

[3] Zeb, K.; Khan, I.; Uddin, W.; Khan, M.A.; Sathishkumar, P.; Busarello, T.D.C.; Ahmad, I.; Kim, H.J. "A Review on Recent Advances and Future Trends of Transformerless Inverter Structures for Single-Phase Grid-Connected Photovoltaic Systems". Energies 2018, 11, 1968.

[4] M. Tsili and S. Papathanassiou, "A review of grid code technical requirements for wind farms," in IET Renewable Power Generation, vol. 3, no. 3, pp. 308-332, Sept. 2009, doi: 10.1049/iet-rpg.2008.0070.

[5] H. Wang, Q. Cheng, M. Li, G. Chen and L. Deng, "The study of single-phase PWM rectifier based on PR control strategy," The 26th Chinese Control and Decision Conference (2014 CCDC), Changsha, 2014, pp. 3818-3823, doi: 10.1109/CCDC.2014.6852845.

[6] M. Elkayam and A. Kuperman, "Optimized Design of Multiresonant AC Current Regulators for Single-Phase Grid-Connected Photovoltaic Inverters," in IEEE Journal of Photovoltaics, vol. 9, no. 6, pp. 1815-1818, Nov. 2019, doi: 10.1109/JPHOTOV.2019.2937386.

[7] S. Silwal, S. Taghizadeh, M. Karimi-Ghartemani, M. J. Hossain and M. Davari, "An Enhanced Control System for Single-Phase Inverters Interfaced With Weak and Distorted Grids," in IEEE Transactions on Power Electronics, vol. 34, no. 12, pp. 12538-12551, Dec. 2019, doi: 10.1109/TPEL.2019.2909532.

[8] X. Guo and J. M. Guerrero, "General Unified Integral Controller With Zero Steady-State Error for Single-Phase Grid-Connected Inverters," in IEEE Transactions on Smart Grid, vol. 7, no. 1, pp. 74-83, Jan. 2016, doi: 10.1109/TSG.2015.2419236.

[9] W. Song, Z. Deng, S. Wang and X. Feng, "A Simple Model Predictive Power Control Strategy for Single-Phase PWM Converters With Modulation Function Optimization," in IEEE Transactions on Power Electronics, vol. 31, no. 7, pp. 5279-5289, July 2016, doi: 10.1109/TPEL.2015.2481323.

[10] X. Hao, X. Yang, T. Liu, L. Huang and W. Chen, "A Sliding-Mode Controller With Multi resonant Sliding Surface for Single-Phase Grid-Connected VSI With an LCL Filter," in IEEE Transactions on Power Electronics, vol. 28, no. 5, pp. 2259-2268, May 2013, doi: 10.1109/TPEL.2012.2218133.

[11] H. Komurcugil, S. Ozdemir, I. Sefa, N. Altin and O. Kukrer, "Sliding-Mode Control for Single-Phase Grid-Connected LCL-Filtered VSI With Double-Band Hysteresis Scheme," in IEEE Transactions on Industrial Electronics, vol. 63, no. 2, pp. 864-873, Feb. 2016, doi: 10.1109/TIE.2015.2477486.

[12] Li, B.; Huang, S.; Chen, X. ,"Performance Improvement for Two-Stage Single-Phase Grid-Connected Converters Using a Fast DC Bus Control Scheme and a Novel Synchronous Frame Current Controller", Energies 2017, 10, 389.

[13] SangJoo Kwon and Wan Kyun Chung, "A discrete-time design and analysis of perturbation observer for motion control applications," in IEEE Transactions on Control Systems Technology, vol. 11, no. 3, pp. 399-407, May 2003, doi: 10.1109/TCST.2003.810398.