Implementation of Short Reach (SR) and Very Short Reach (VSR) data links using POET DOES (Digital Opto-electronic Switch)

Summary

POET's implementation of monolithic opto-electronic devices enables the creation of a "transceiver module on a chip". Through the combination of all of the critical components of a transceiver — Laser, Detector, Laser Driver/Modulator, Amplifiers and some control electronics — on to a single chip, the POET solution can create a discontinuity in traditional cost and power curves associated with optical transceivers, through a dramatic reduction in the BOM and packaging costs associated with these applications.

1. Introduction

Semiconductors that emit, detect, and manage light have evolved to become a mature photonics technology for advanced products today that range from laser based systems such as DVD and Blu-ray consumer products to high performance solar cell systems that power satellites and remote solar farms, and to the communications engines inside huge data centers that power the internet.

However as internet traffic grows, there is a growing need to proliferate optical communications across all communication links including Very Short Reach segments where copper transceivers dominate today. This is critical in order to lower the power consumption associated with typical copper based interconnects. Energy consumption is quite literally a hot topic for data center designers these days!

According to one presentation at the 2013 OFC conference, the average power consumption from a 10 gigabit per second copper PHY is around 3W; this can perhaps be reduced to 1.5W using an active copper link with power control. Compare this with a fiber optic transceiver (using a short wavelength VCSEL source over multimode fiber) which comes in at only 15mW (at 1.5pJ/bit). However, in order for optical communications to replace copper, the cost (in addition to the power) must come down by up to a factor of 10.

How can photonics manufacturers lower the cost and power in a disruptive manner? It's clear that just extrapolating current technology is not going to work.

Incremental changes in components or technology will not provide the desired solution.

2. Monolithically integrated opto-electronic circuits

The silicon integrated circuit is comprised of a bunch of CMOS transistors on silicon. And the process of integration over the years has simplified system design and resulted in substantial improvements in cost, performance, power and functionality.



Fig. 1 Example of Functionality Integration realized in Silicon Integrated Circuits

Photonics IC's by corollary are comprised of a series of monolithically integrated photonic components — lasers, detectors, modulators, amplifiers and electronic circuitry. Photonic IC platforms will be symbiotic with silicon ICs, and provide a mechanism for optical communications to occur in a cost effective manner.

It's been recognized at OFC/NFOEC that a limiting factor in the design of future exascale supercomputers is the energy consumption per calculation. Research also shows that the energy involved in data transport is significantly larger than the energy involved in computations. As an example, the energy consumed in a single computation is around 0.1 pJ per bit. The energy involved in transporting that data across printed circuit board distances (3-10 inches) is about 200 times higher, and the energy used in transporting data across distances typically found in a data center is about 2000 times higher. Optical communications hold the key to lowering the energy consumption of the interconnect fabric, from the chip, across the board and from board to board. More specifically, photonic integration will revolutionize the field of optics in the same way that integrated circuits revolutionized the world of electronics.

There are various approaches to how one can create integrated photonics IC's: silicon photonics, indium phosphide, gallium arsenide, optical polymers etc. The POET platform provides one such means of co-integrating high speed photonics

and high speed analog and digital electronics, using a Gallium Arsenide integration platform, which is particularly cost and power efficient.

3. Monolithic Photonic Integration applied to Optical Transceivers

A critical current need in data communication technology is for high performance transceivers to provide data links between chips, boards and racks. Current speeds are dominantly 10Gbps with the availability of four 25Gbps channels to achieve 100Gbps and plans to eventually achieve 400Gbps. Two key applications are SR (<500m) and VSR (< 50m). There are two competing technologies today which are VCSEL's and pin detectors operating at 850nm or SiP (silicon photonics) based on external DFB lasers and integrated Ge waveguide detectors operating at either 1310nm or 1550nm.

3.1 VCSELS

The VCSEL solution is a hybrid assembly of 4 IC's including a discrete 850nm VCSEL, a Si CMOS or SiGe BiCMOS laser driver IC, a discrete GaAs pin detector and a Si receiver IC consisting of a TIA, limiting amplifiers and an output amplifier. Cost and power are significant limitations. The assembly of multiple chips in a single package is labor intensive, is very sensitive to parasitics and degrades yield. The power consumption of this approach is a limitation due to the low conversion efficiency of the driver circuit, the need for equalization at both receive and transmit nodes and the multiple amplifiers required in the receive chain.

The VCSELs currently have reached 25GHz ft's in a lab setting which is sufficient to achieve a 50Gbps data channel although the commercially available VCSEL links are operating at 10Gbps to 25Gbps line rates. All of these 850nm VCSEL links are implemented with a MMF optical connection because the VCSEL itself is multimode over its operating range and the MMF alignment is the lower cost solution. The MMF has now been optimized for VCSEL power profiles and 300m is possible at 10Gbps. It is currently the mainstay of the data link market and is the desired solution whenever possible. However it fails currently for 500m links, especially at 25Gpbs link rates, where the maximum reach achievable is limited to about 100m. Therefore for aggregate 100Gbps links, VCSELs are being challenged by SiP (Silicon Photonics) circuits using SMF for optical propagation. The consensus is that all future fiber plants will have to be SM for link distances beyond 100m and thus this represents a growth market for SiP.

3.2 Silicon Photonics

SiP implements some optical functions on a Si wafer with waveguide technology to achieve integration. The elements integrated are a MZ modulator based on the relatively weak index variation obtained by free carrier injection in a Si pn junction, a waveguide MSM detector based on Ge deposition and passive waveguides for I/O coupling. This coupling is achieved by angled fiber placement to a waveguide grating element. Much research has been devoted to the inclusion of CMOS driver circuits in the integration. However currently, in most implementations of SiP, the equalization circuits (FFE and DFE), the modulator driver circuits, the TIA and the receive amplifiers are all placed on a separate IC and bonded intimately to the optical chip. The laser source is an external component. An example of such an implementation, from IMEC is shown below.

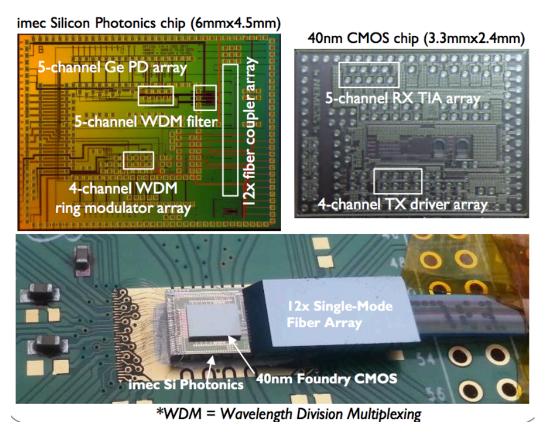


Fig 2. Example of a typical SiP solution – standard configurations involve three chips including an electronic IC, a photonic IC and the Laser

Compared to VCSELs, the problems of power and cost are also considered as limitations for SiP, i.e. the packaging is expensive and the drive and receive circuits are power hungry. However SiP has a key advantage over the VCSEL. It is a SM solution at 1310nm or 1550nm so reach is not a limitation. The other advantage of Silicon Photonics is its ability to incorporate higher modulation schemes (PAM4) or Coarse Wavelength Division Multiplexing (CWDM), which is currently not possible with VCSEL based technology. Current state of the art for Si Photonics is to provide line rates at 25Gbps for aggregate line rates of 100Gbaud or 200Gbaud using either Duplex CWDM or Parallel Single Mode (PSM) links.

3.3 The POET Solution

POET combines the cost benefits offered by traditional VCSEL links and the performance benefits offered by Si Photonics solutions. POET's solution to the data link problem involves new device and process innovations that provide the platform with unique advantages and combine the benefits of both the VCSEL and SiP solutions.

The POET solution offers two options. In the short term, lasing is architected to be out-of-plane and the laser solution is a VCSEL. However, in the medium term and as part of the POET roadmap, lasing can co-exist both in-plane and out-of-plane simultaneously.

3.3.1 Out-of-plane Lasing (VCSELs)

The POET VCSEL epitaxy and process sequence are designed to be able to cointegrate VCSELs and electronic devices like Field Effect Transistors (FETs) and Heterojunction Bipolar Junction Transistors (HBTs). The primary differentiating features of the POET platform are as follows.

- (i) The POET epitaxy for the integrated VCSEL/electronic stack is simpler than traditional VCSELs, providing an inherent cost advantage starting from the epi growth.
- (ii) The laser driver/modulator transistors and the laser are integrated. This integration greatly simplifies the laser circuit itself since one can use high speed GaAs based HFETs to directly modulate the laser without having to worry about signal integrity issues going through discrete packages and printed circuit boards. The overall power requirement is consequently reduced.

- (iii) POET implements a new paradigm for lasing utilizing a new laser structure in the form of a digital opto-electronic switch (DOES). The switch has binary optical states, i.e. it has high impedance (laser off) and low impedance (laser on) digital electrical states which ensures an essentially infinite extinction ratio. The DOES is a digital device and has internal gain and thus it is triggered to the on state with a single transistor delivering a much smaller drive current than a conventional laser driver circuit. It is worth noting here that all conventional lasers (including VCSELs) are fundamentally analog devices (PN diodes) and they require modulation around a bias current set point.
- (iv) POET further implements a new paradigm for the detector a resonant cavity detector again using the DOES concept. For the receiver the DOES is used as a digital detector in which the incident light causes switching from the high impedance off state to the low impedance on state. Here also the DOES's internal gain increases the sensitivity of the detection and provides digital waveform shaping so that the TIA and associated amplifiers are not required. The OE conversion and signal restoration are achieved in a single stage.
- (v) For both transmit and receive, the waveform shape is dictated by the DOES switching so that FFE and DFE circuits are not necessary. The benefits of this approach are clearly to reduce component count and power consumption.
- (vi) The unique structure and construction of the POET VCSEL results in single mode operation, which is typically not possible with the standard VCSEL.

Compared to traditional VCSEL based links, integration to realize a single chip to replace the current 4-chip solution substantially simplifies and reduces both the IC costs and the packaging cost. More importantly, the complete monolithic integration can provide up to an order of magnitude improvement in total power consumption. The speed parameters also favor higher speed performance compared to traditional VCSEL-based data link capabilities for MMF based short reach applications.

Since the POET VCSEL is single mode, it is further expected that using the POET VCSEL with SMF will allow a data rate of 25Gbps per channel up to 500m. This

solution would provide a very attractive single chip alternative to existing SiP approaches.

3.3.2 In-Plane Lasing

As previously mentioned, The POET architecture can lase in plane and out of plane simultaneously. When lasing in-plane, the POET solution provides access to a larger array of opto-electronic devices, which can be combined to create numerous and new applications such as RF Photonics, Optical ADC's, Optical clocking, CWDM etc. This platform provides all of the capabilities currently available in other in-plane waveguide based technologies such as Indium Phosphide or SiP with the added benefit of electronic and laser integration within the same chip.

Below is the table comparing the device suite between in-plane and out-of-plane lasing.

Components	In Plane	Out of Plane
Laser - light source	Ring Resonator	VCSEL
Modulator	•Direct w/ Thyristor •HFET coupling •EAM	Direct w/ Thyristor
Modulator Driver	On chip signaling	On chip signaling
Detector	•Thyristor Detector •HFET Detector	Thyristor Detector
Multiplexer	•Ring Resonators •Gratings	Fiber
Coupler	Evanescent	N.A.
Waveguides	Monolithic (low loss)	N.A.
Optical Amplifiers	Active waveguide	N.A.
WDM	DFB on chip lasers	N.A.
SST	Yes for Butt Coupling	N.A.

Specifically compared to SiP, in-plane lasing with POET technology provides access to critical active components – primarily the laser and the semiconductor Optical

Amplifier. Additional advantages of the POET solution to more conventional inplane lasing solutions are :

- tight confinement of light in the waveguides enabling 90 degree bends and smaller features
- strong index change through carrier modulation in the quantum wells
- no epitaxial growth interface to the waveguide resulting in low loss light coupling
- automatic locking of wavelength due to resonant cavities eliminating the need for wavelength tuning and heater elements

4. Conclusion

A new monolithic opto-electronic platform has been developed, with novel device and process innovations. The platform provides a unique way to monolithically integrate the optical and electronic devices needed for optical transceivers representing a disruption in both the Short Reach and Very Short Reach segments of the data communications market. Further build out of the POET platform to include in-plane lasing adds additional disruptive features and capabilities enabling a new class of optical communications and computing chips.