Circuit Schematic

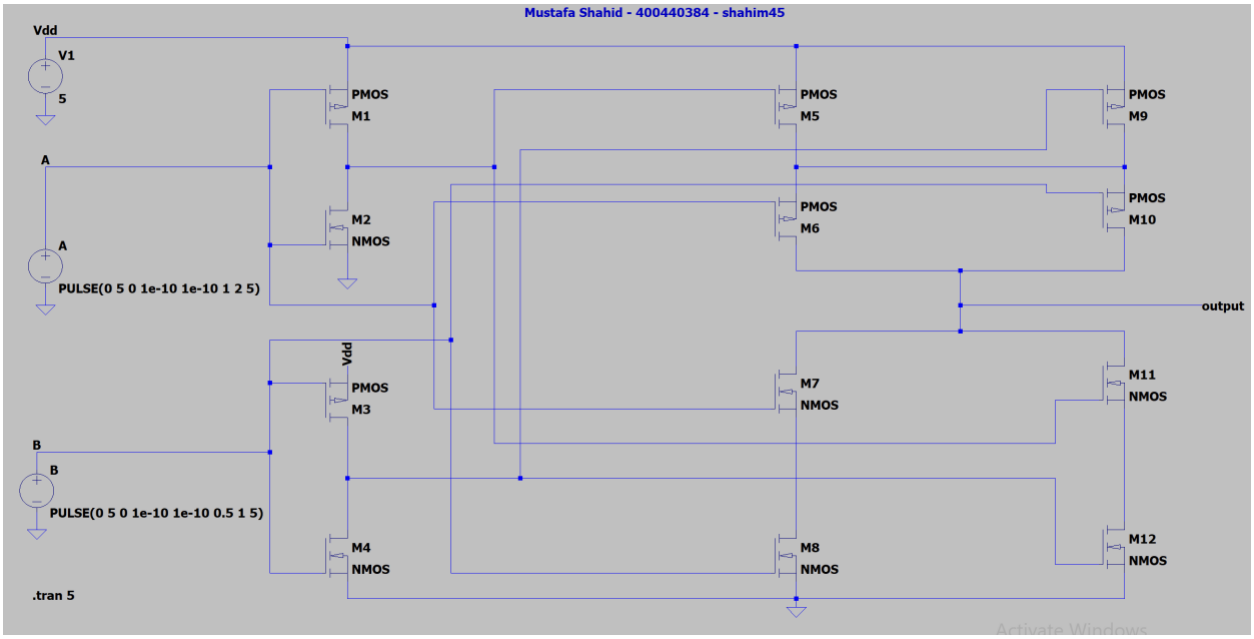


Figure 1: Circuit Schematic

Ideal Sizing

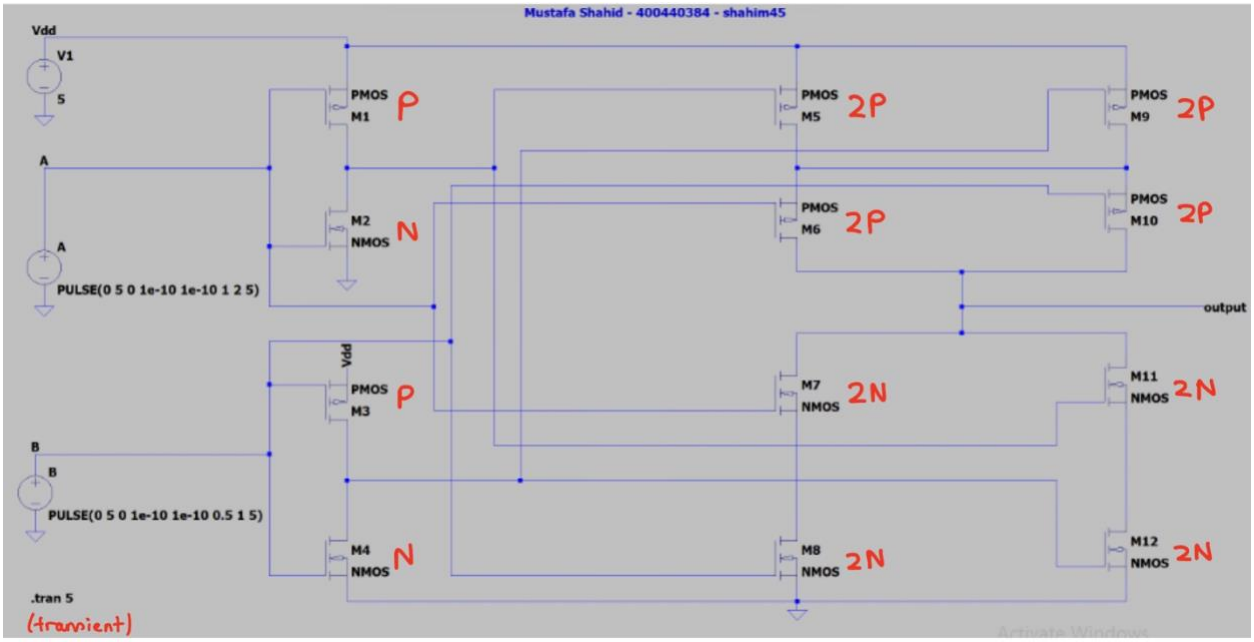


Figure 2: Circuit Schematic with size annotations

The goal when crafting transistors for this kind of application is to attain equal resistances. A transistor's resistance, denoted as RON, is inversely related to the W over L ratio. Given the variance in charge mobilities between NMOS and PMOS transistors, simply assigning W and L values isn't straightforward. For the resistances of both device types to align, differing W over L ratios are required. Electrons generally have a higher charge mobility compared to holes, necessitating a larger W over L ratio for PMOS transistors to achieve parity. In practice, we set the ratio for PMOS to $(w/l)p = 2.5 \times (w/l)n$, where $(w/l)n$ is the ratio for NMOS transistors. Our standard size ratio is thus 5:2. These ratios are pivotal in regulating the τPHL and τnLH parameters of our circuit, which are crucial for ensuring optimal circuit performance. Ideal sizing ensures that the rise and fall time constants, τREF, are matched. In the implementation phase, each MOSFET is allocated a p-factor, denoted as p and equating to $(w/l)p$, and an n-factor, denoted as n and equating to $(w/l)n$. This ensures that no current path's resistance exceeds that of the foundational inverter, details of which are visible next to each MOSFET in Figure 2 above.

IMPLEMENTATION OF IDEAL SIZING

We lack the ability to dictate the specific dimensions of our transistors, making it impractical to achieve the perfect transistor sizing. The physical dimensions of the transistors are pre-set by the creators of the MC14007UB IC. Despite our inability to alter the transistors' sizes, the MOSFETs approximately fulfill the necessary sizing ratios we aim for: a PMOS to NMOS ratio of 2.5 to 1. Matching the resistances precisely could lead to more consistent signal delay times for both the incoming and outgoing signals. This would enhance both the noise margins and the τ PLHv alue, which would, in turn, make the circuit more adaptable for integration into larger systems. Although perfect optimization isn't achievable, the outcome can still approach the ideal noise margins and τPLH values, albeit not exactly.

Functional Testing

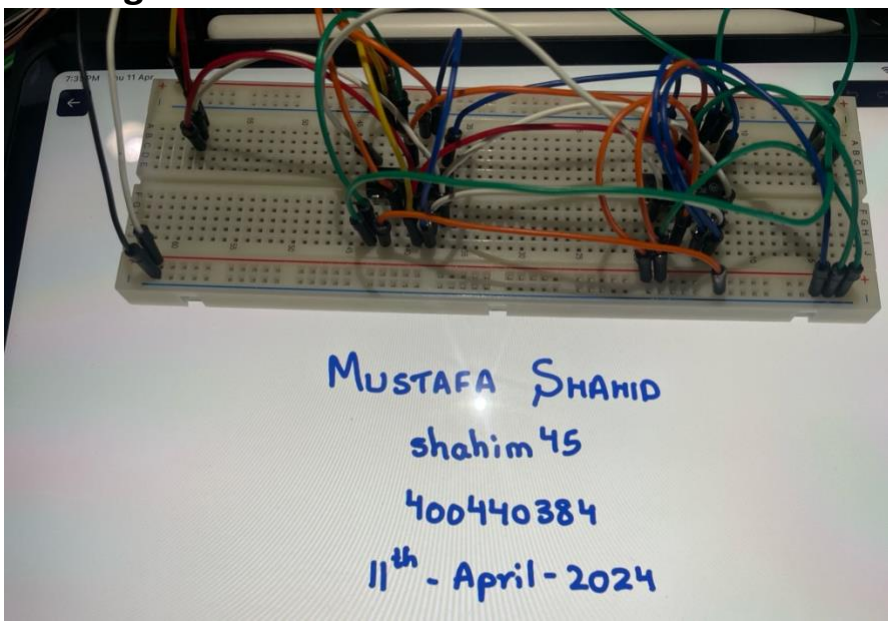


Figure 3: Top view of circuit

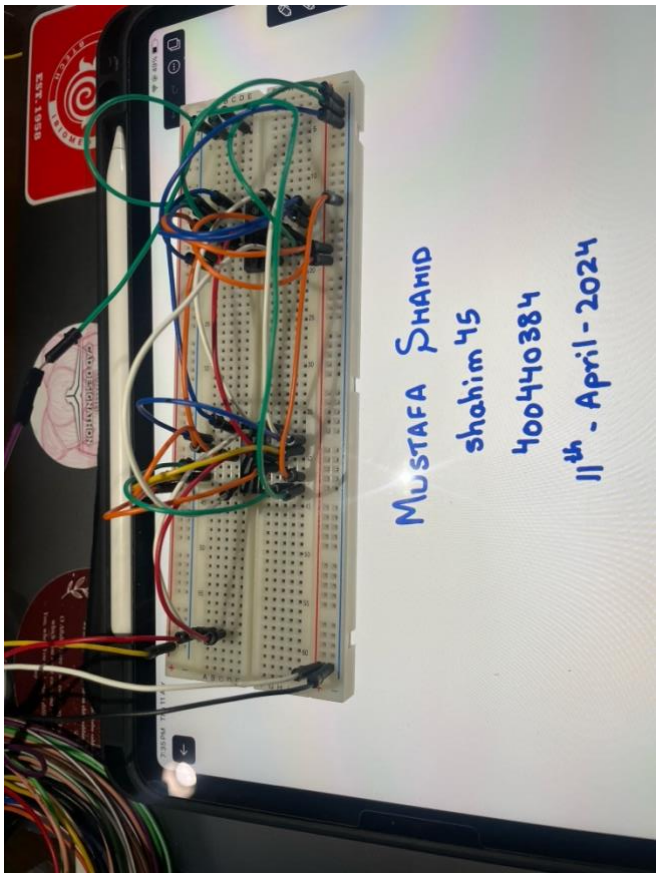


Figure 4 : Front view of circuit

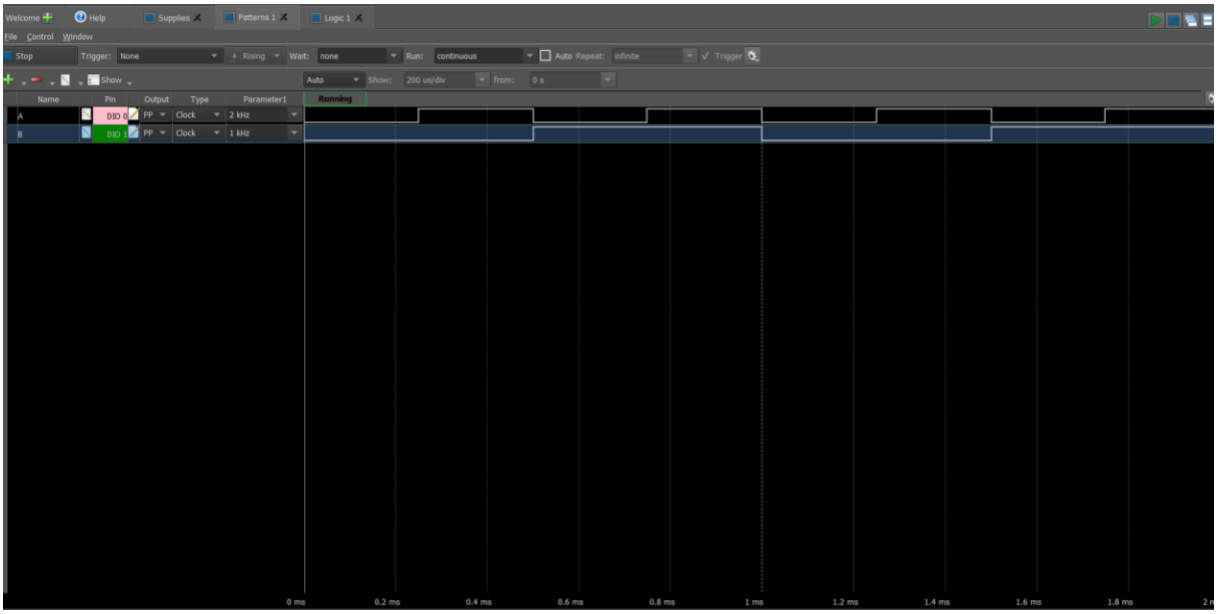


Figure 5 : Pattern Generator

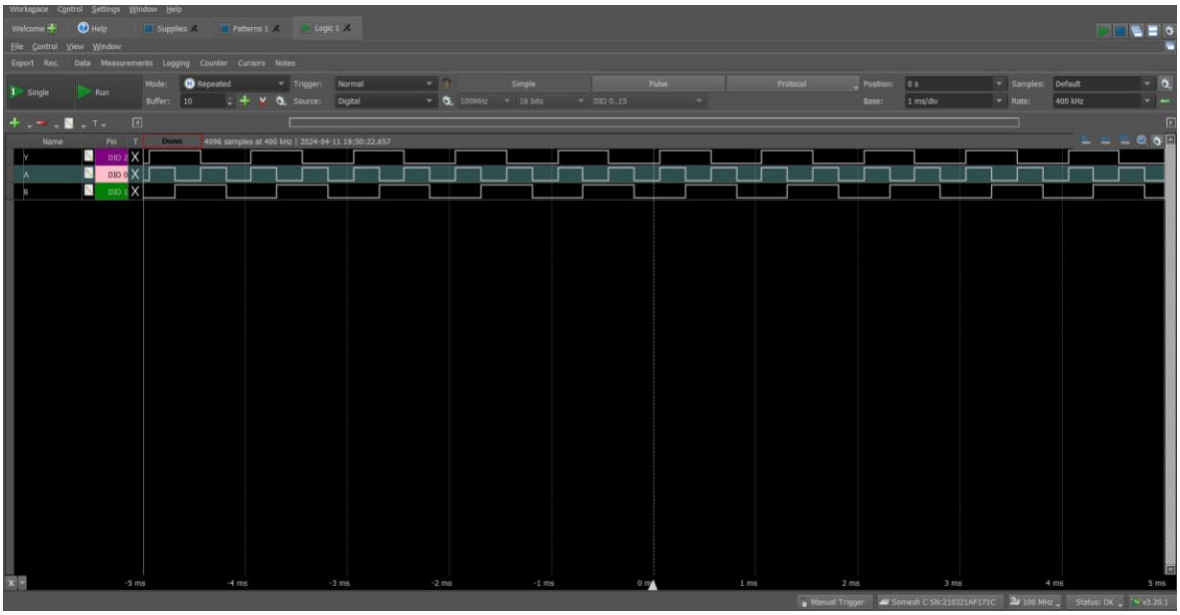


Figure 6 : Logic Analyzer Output

XOR Truth Table

Input 1	Input 2	Output
0	1	1
0	0	0
1	1	0
1	0	1

The outputs seen in the logic analyzer in Figures 5 and 6 match the expected outputs seen in the truth table for an XOR gate.

Static Level Testing

The oscilloscope result that follows was obtained when input 'A' was set to a 5V DC and input 'B' was set to a 50Hz square wave that goes from 0V to 5V. The blue wave (C2) is the XOR output, and the yellow wave (C1) is input "B." The output is equivalent to an XOR gate's performance.

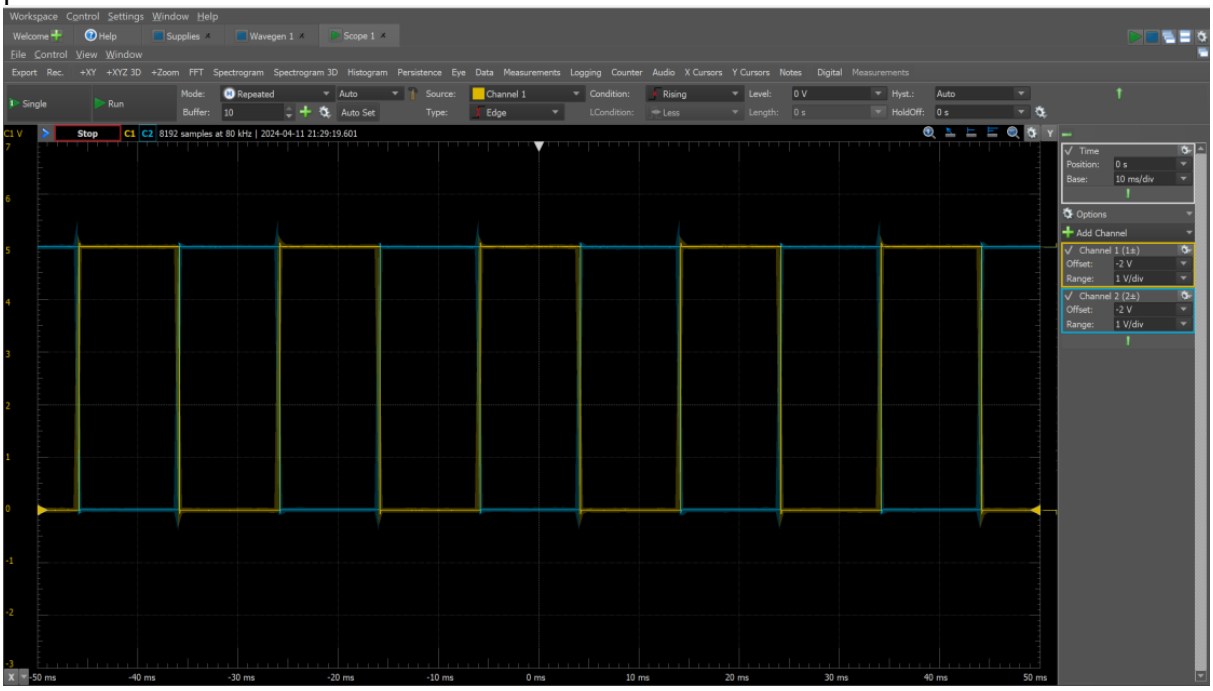
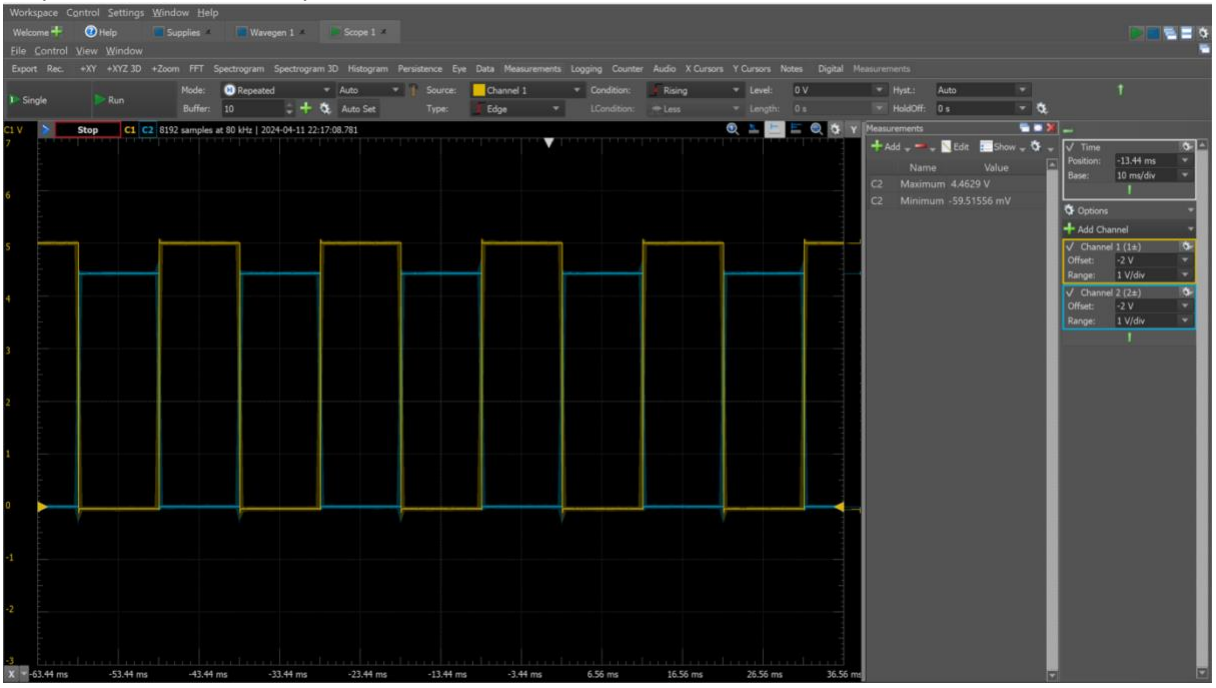


Figure 7 : Oscilloscope results when $A = 5V$ and $B = 50Hz$ square wave. Yellow is output, Y, and blue is B input.



The oscilloscope result that follows is obtained when the inputs are reversed, that is, when input 'A' is the square wave and input 'B' is a 5V DC.

VH and VL Values

The square wave input's amplitude was decreased by 0.1V starting at the original 2.5V and continuing until the output no longer produced the desired performance in order to calculate VH and VL. Since the output LOW was marginally greater than 0V at this amplitude, the amplitude was calculated to be 0.75V. The formulas used are V_H = Offset + Amplitude and V_L = Offset – Amplitude.

$$V_H = 3.25V \text{ and } V_L = 1.75V$$

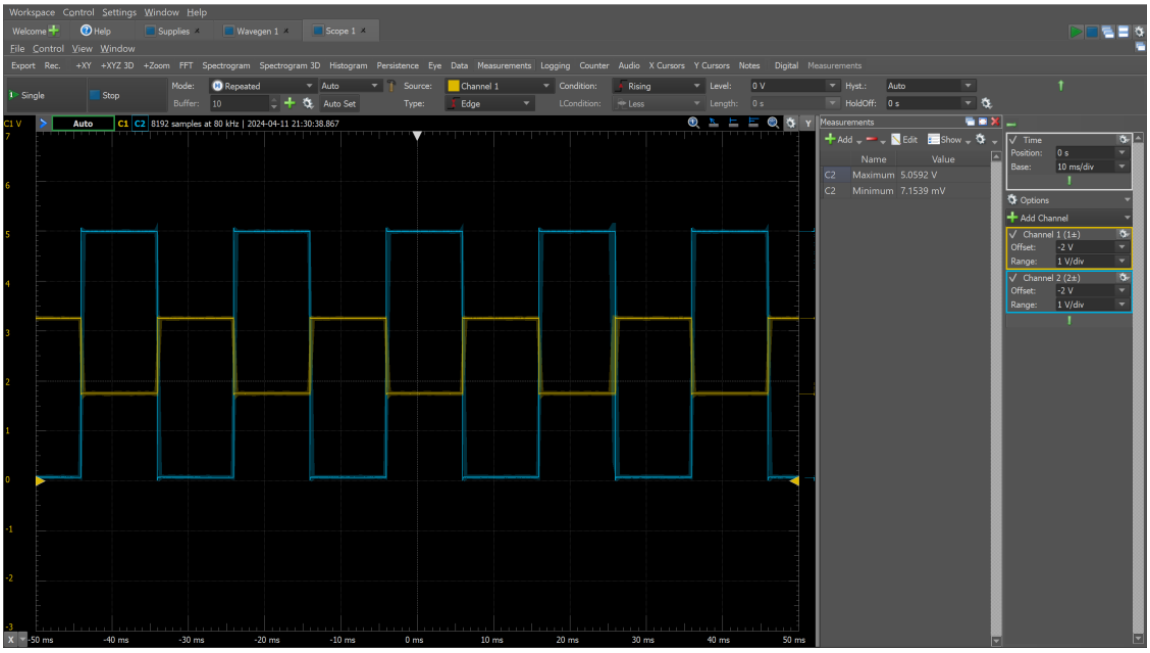


Figure 8 : Oscilloscope output showing the output, Y, in yellow and the input B in blue. A = 5 V. Amplitude = 0.7 V. Offset = 2.5 V.

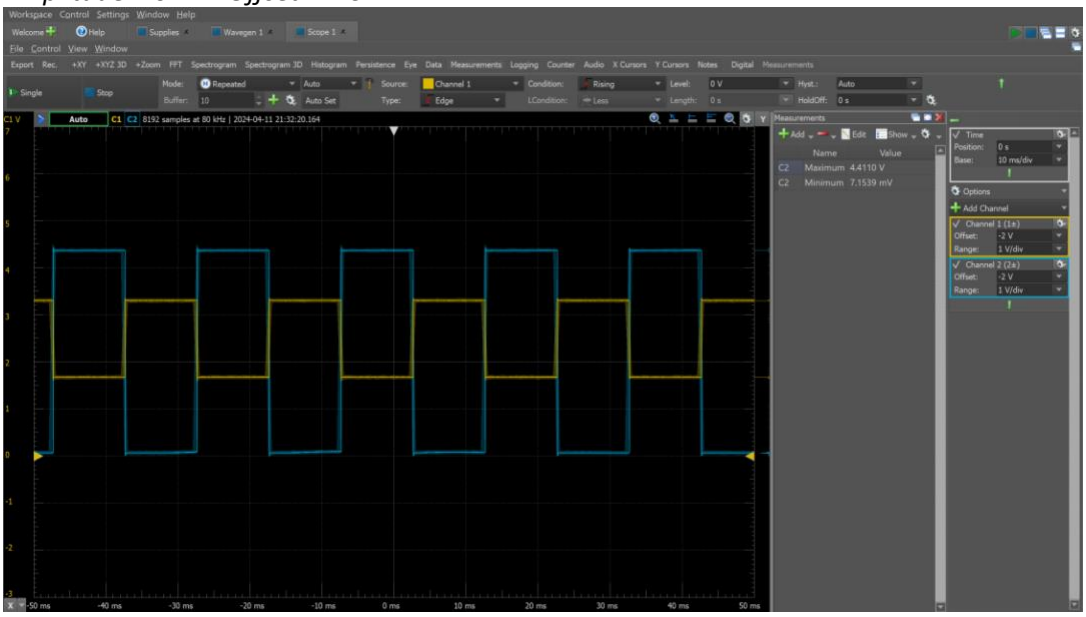


Figure 9 : Oscilloscope output showing the output Reversed, Y, in yellow and the input B in blue. A = 5 V. Amplitude = 0.7 V. Offset = 2.5 V.

Timing Performance

To serve as a load, a 100nF capacitor was added to the output node's end. The new load was used to operate the oscilloscope. Cursors were used to calculate Rise Time and Fall Time after zooming in on a single rising and falling edge.

Rise Time

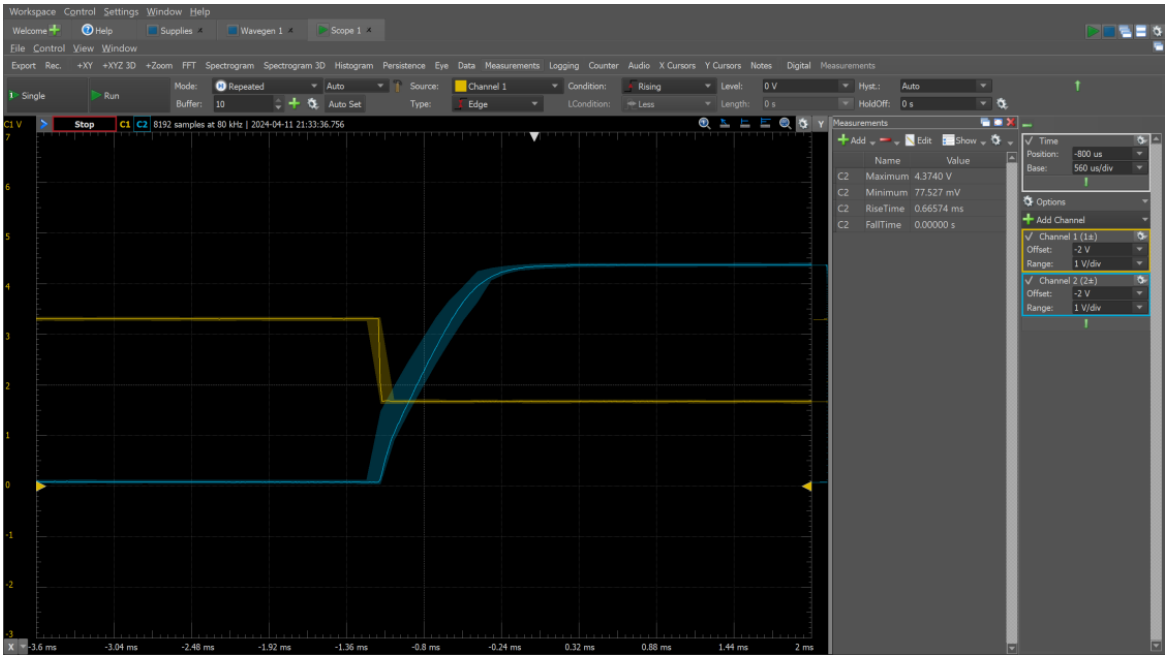


Figure 10 : Oscilloscope output for the rise time.

Fall Time

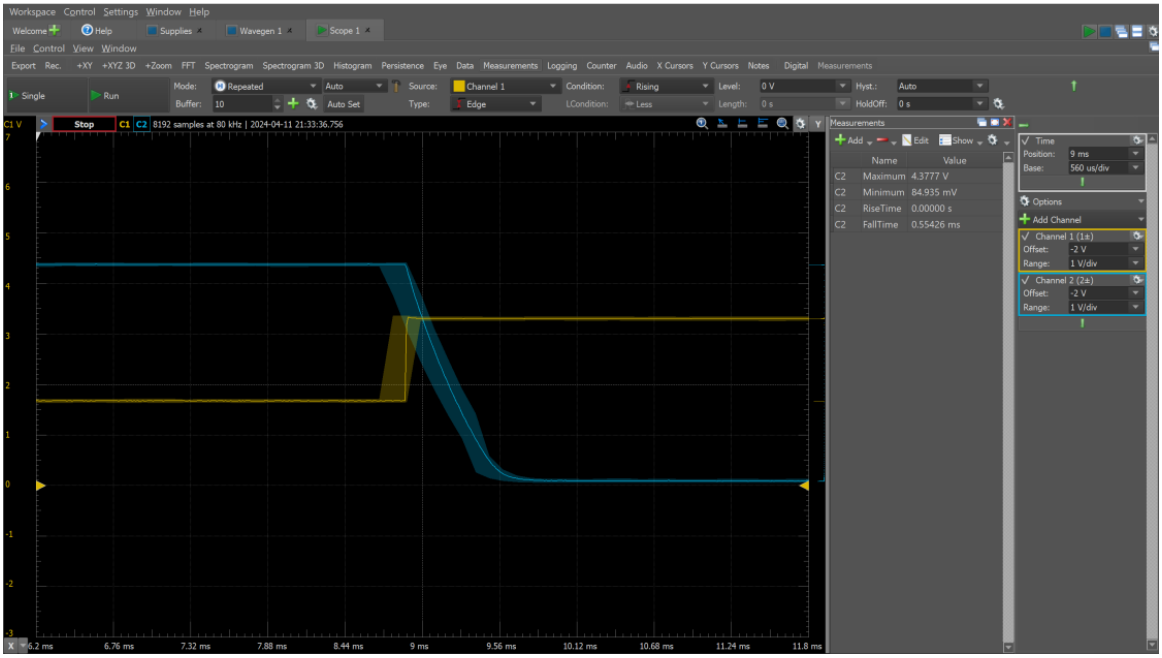


Figure 11 : Oscilloscope output for the fall time.

The fall time is 0.55426 ms and the rise time is 0.66574 ms.

Determining τ_{PLH}, τ_{PHL}, and τ_P

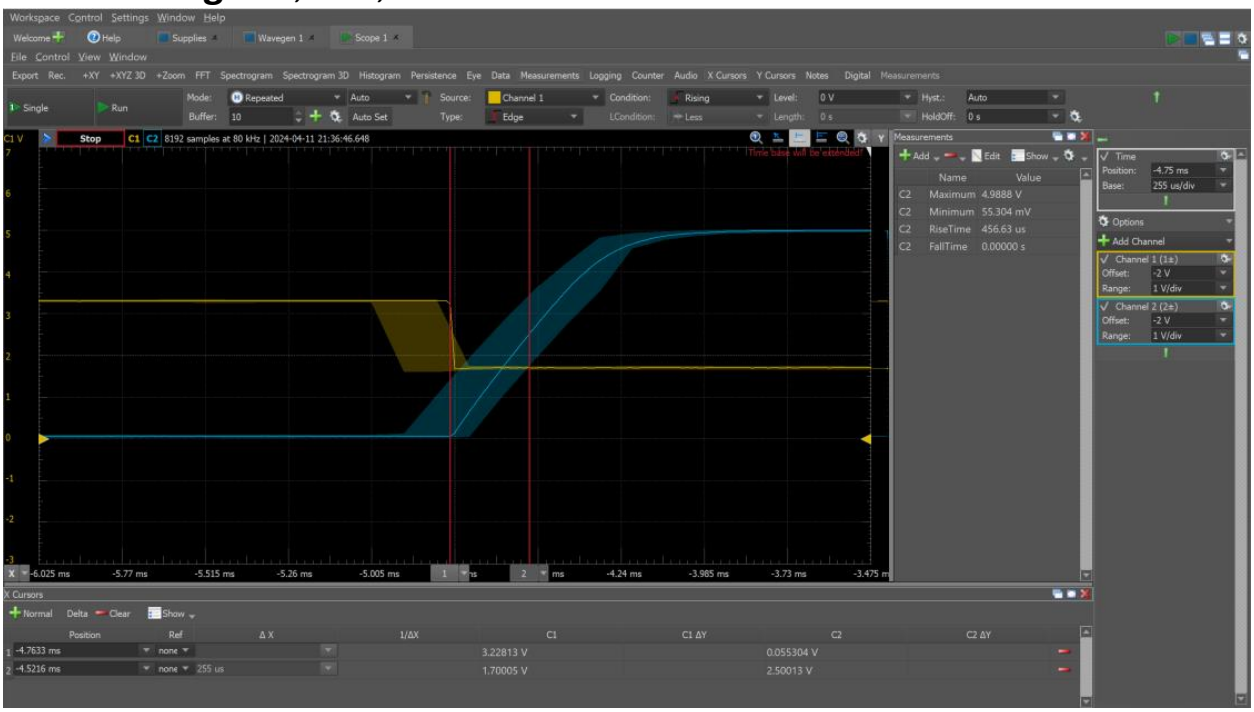


Figure 12 : Annotated oscilloscope output to measure where blue τ is input and yellow $_{PLH}$ is output.

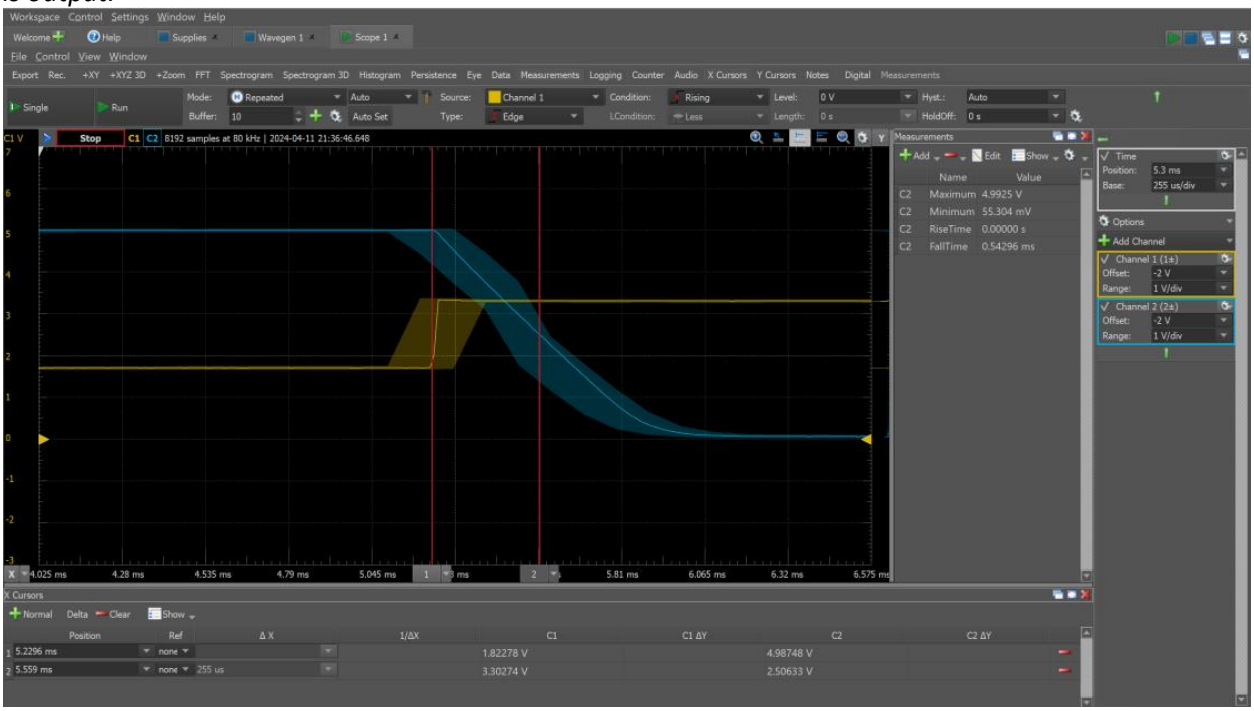


Figure 13 : Annotated oscilloscope output to measure τ where blue is input and yellow $_{PHL}$ is output.

τpHL: 255us

τ_{LH} : 255us.

τ_p : $\tau_p = (\tau_{LH} + \tau_{pHL}) / 2 = 255$ us