Design Rules Verification Report

Filename : C:\Users\Jerome\OneDrive - UCB-O365\ECEN5613_ESD\Project.git\Schematics\F

Warnings 0
Rule Violations 8

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=8mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	4
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=8mil) (Max=30mil) (Preferred=12mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=20mil) (Air Gap=12mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	4
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=4mil) (All),(All)	0
Silk To Solder Mask (Clearance=4mil) (IsPad),(All)	0
Silk to Silk (Clearance=4mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	8

Un-Routed Net Constraint ((All))
Un-Routed Net Constraint: Net NetP1_1 Between Pad Q2-2(1356.102mil,1711.024mil) on Top Layer And Pad Q2-2(1608.071mil,1711.024mil) on Top
Un-Routed Net Constraint: Net NetL1_2 Between Pad Q3-2(1358.268mil,588.583mil) on Top Layer And Pad Q3-2(1610.236mil,588.583mil) on Top Layer
Un-Routed Net Constraint: Net NetP1_1 Between Pad Q4-2(1356.102mil,1336.024mil) on Top Layer And Pad Q4-2(1608.071mil,1336.024mil) on Top
Un-Routed Net Constraint: Net NetL1_2 Between Pad Q5-2(1356.102mil,965.551mil) on Top Layer And Pad Q5-2(1608.071mil,965.551mil) on Top Layer

Hole Size Constraint (Min=1mil) (Max=100mil) (All)
Hole Size Constraint: (104.331mil > 100mil) Pad L1-1(2721.496mil,1251.968mil) on Multi-Layer Actual Slot Hole Width = 104.331mi
Hole Size Constraint: (104.331mil > 100mil) Pad L1-1(2892.126mil,1026.575mil) on Multi-Layer Actual Slot Hole Width = 104.331mi
Hole Size Constraint: (104.331mil > 100mil) Pad L1-2(1770.079mil,1026.575mil) on Multi-Layer Actual Slot Hole Width = 104.331mi
Hole Size Constraint: (104.331mil > 100mil) Pad L1-2(1940.709mil,800.197mil) on Multi-Layer Actual Slot Hole Width = 104.331mi