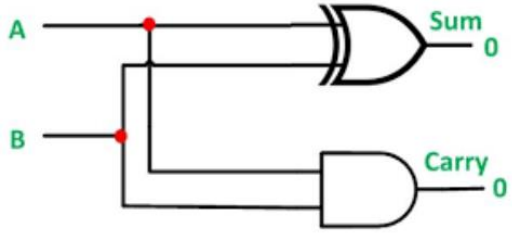
BITS-Pilani Dubai Campus
I Sem 2021-22
Digital Design Laboratory / ECE/INSTR/CS F215
Submission Report
Experiment No.- 4 (Adders and Subtractors)

Name: V N Suchir Vangaveeti **ID Number: 2020A7PS0018U**

Hardware runs

Run 1: Half adder

Diagram

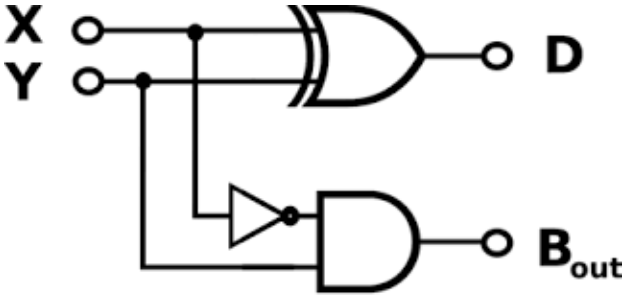


Truth Table

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Run 2: Half subtractor

Diagram



Truth Table

A	B	DIFFERENCE	BORROW
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

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Software runs

Run 3: Full adder and 4-bit adder

Q: Write the Verilog code and testbench of Full adder using data flow modeling.

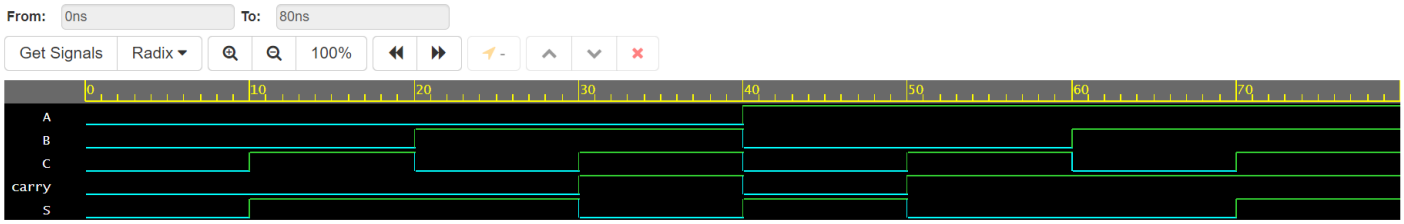
A: Verilog Code-

```
module fulladder (A,B,C,S,carry);
  input A,B,C;
  output S,carry;
  assign S = A^B^C;
  assign carry = C & (A^B) | (A&B);
endmodule

//testbench
module fulladder_tb;
  reg A,B,C;
  wire S,carry;
  initial
    begin
      $dumpfile("dump.vcd");
      $dumpvars(1,fulladder_tb);
      #00 A=0; B=0; C=0;
      #10 A=0; B=0; C=1;
      #10 A=0; B=1; C=0;
      #10 A=0; B=1; C=1;
      #10 A=1; B=0; C=0;
      #10 A=1; B=0; C=1;
      #10 A=1; B=1; C=0;
      #10 A=1; B=1; C=1;
      #10 $stop;
    end
  fulladder x1(A,B,C,S,carry);
endmodule
```

Q: Paste the Image of your **Simvision** window where you get the waveforms for the above code.

A:



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Q: Write the Verilog code and testbench for 4- bit parallel adder using structural modeling, use full adder as a building block.

A: Verilog Code-

```
module pfulladder (A,B,S,C,carry);
  input [3:0] A,B;
  input C;
  wire C1, C2, C3;
  output [3:0]S;
  output carry;
  fulladder fa0(C1, S[0], A[0], B[0], C);
  fulladder fa1(C2, S[1], A[1], B[1], C1);
  fulladder fa2(C3, S[2], A[2], B[2], C2);
  fulladder fa3(carry, S[3], A[3], B[3], C3);
endmodule

module fulladder (A,B,C,S,carry);
  input A,B,C;
  output S,carry;
  assign S=A^B^C;
  assign carry=C&(A^B)|(A&B);
endmodule

//testbench
module pfulladder_tb;
  reg[3:0]A,B;
  wire carry;
  wire [3:0]S;
  initial
    begin
      $dumpfile("dump.vcd");
      $dumpvars(1,pfulladder_tb);
      #00 A=4'b0001; B=4'b0010;
      #10 A=4'b1101; B=4'b1010;
      #10 A=4'b0110; B=4'b1010;
      #10 A=4'b0101; B=4'b1110;
      #10 A=4'b1101; B=4'b1010;
      #10 A=4'b0110; B=4'b0010;
      #10 $stop;
    end
  pfulladder FA1(A,B,S,C,carry);
endmodule
```

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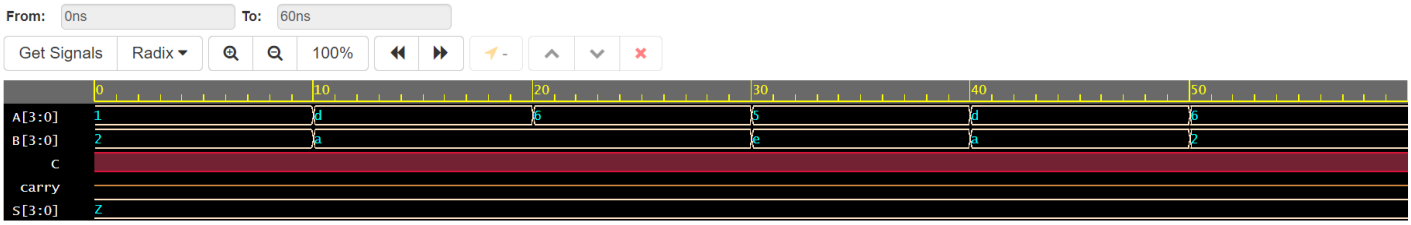
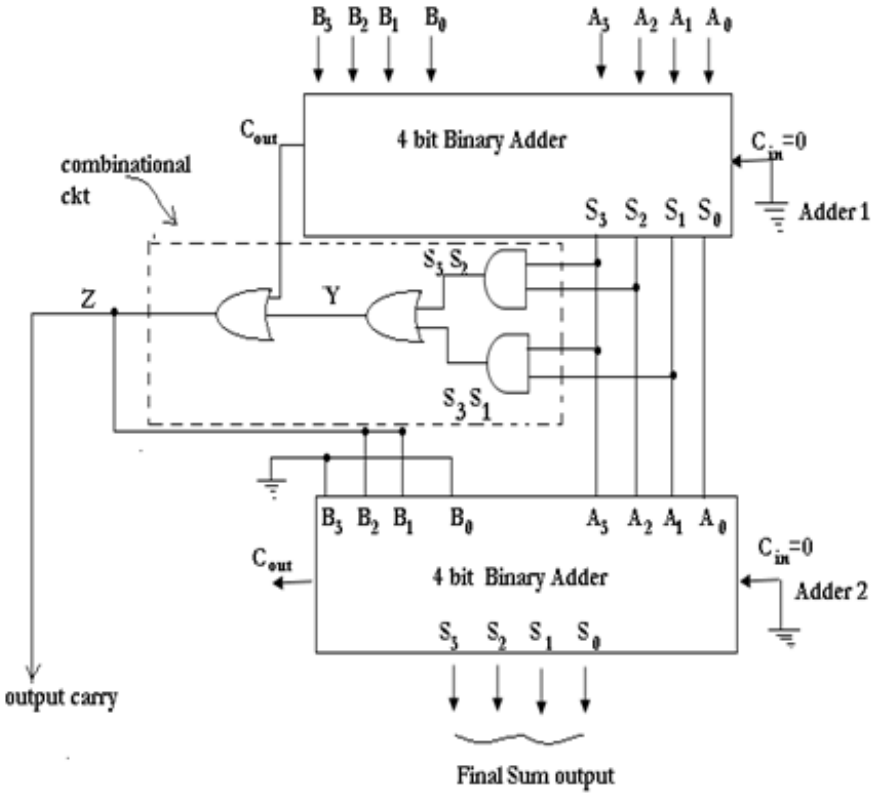
Q: Paste the Image of your **Simvision** window where you get the waveforms for the above code.
A:



Run 4: BCD adder

Q: Write the verilog code and testbench for BCD adder using structural modeling, use 4-bit parallel adder and other gates as building blocks. (Hint refer the image below)



A: Verilog Code-

```
module bcd_adder(carry,secondB, sum, a, b);
input[3:0] a,b;
output[3:0] sum;
output carry;
reg ip=0;
wire[3:0] s;
wire[1:0] op;
```

```
output reg[3:0] secondB;
paralleladder g1 (op[0], s, a, b, ip);
assign carry = s[1]&s[3] | s[2]&s[3] | op;
assign secondB[0] = 0;
assign secondB[1] = carry;
assign secondB[2] = carry;
assign secondB[3] = 0;
paralleladder g2 (op[1], sum, s, secondB, ip);
endmodule

module paralleladder(op, sum, a, b, iip);
input[3:0] a,b;
input iip;
output[3:0] sum;
output op;
wire[2:0] ip;
fulladder G1 (ip[0], sum[0], a[0], b[0], iip);
fulladder G2 (ip[1], sum[1], a[1], b[1], ip[0]);
fulladder G3 (ip[2], sum[2], a[2], b[2], ip[1]);
fulladder G4 (op, sum[3], a[3], b[3], ip[2]);
endmodule

module fulladder (op, sum, a, b, ip );
input a,b,ip;
output op, sum;
assign sum = a^b^ip;
assign cout = ip&(a^b) | a&b;
endmodule


//testbench
module testbench();
reg[3:0] a,b;
wire[3:0] sum,secondB;
wire carry;
initial begin
$dumpfile ("dump.vcd");
$dumpvars (1, testbench);
#000 a = 4'b0000; b = 4'b0000;
#100 a = 4'b1001; b = 4'b0011;
#100 a = 4'b1000; b = 4'b1000;
#100 a = 4'b1000; b = 4'b0111;
#100 a = 4'b0101; b = 4'b0111;
#100 a = 4'b0000; b = 4'b0000;
#100;
```

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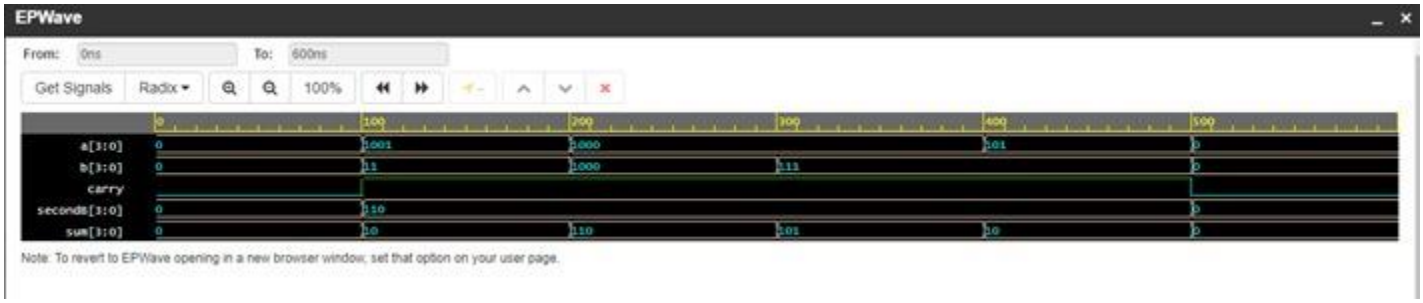
```
$stop;
end
bcd_adder g1 (carry,secondB, sum, a, b);
endmodule
```

Q: Paste the Image of your **Simvision** window where you get the waveforms for the above code.
A:



Assignment All assignments are to be submitted strictly before start of next lab session through online only. Late assignments will not be entertained and will be awarded '0' marks.
Copy-paste or type the unique URL of your assignment solution from website www.edaplayground.com for assignment questions. Please note that do not copy someone else's link as any kind of unfair means will result in academic misconduct and will be treated accordingly. All links for each user and each code are unique.

Q1: Verilog code and testbench for converting 8-bit binary number to gray code using data flow modeling.
Ans: Link1: https://edaplayground.com/x/EcGD

Q2: Verilog code and testbench for full subtractor using data flow modeling.
Ans: Link2: https://edaplayground.com/x/Wpcn

Q3: Verilog code and testbench for full subtractor using behavioral modeling.
Ans: Link3: https://edaplayground.com/x/hcCW