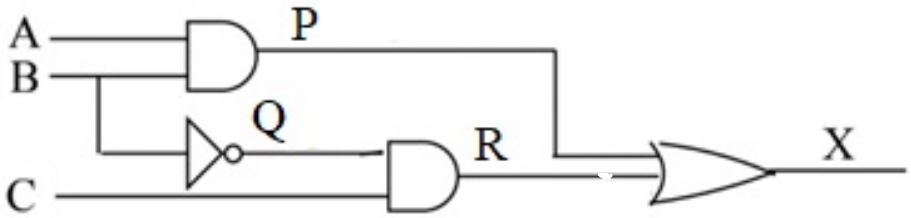
BITS-Pilani Dubai Campus
I Sem 2021-22
Digital Design Laboratory / ECE/INSTR/CS F215
Submission Report
Experiment No.- 3 (Implementation of Boolean Function)

Name: V N Suchir Vangaveeti **ID Number: 2020A7PS0018U**

Hardware runs
Run 1: AND-OR implementation
Diagram



Truth Table

A	B	C	P	Q	R	X
0	0	0	0	1	0	0
0	0	1	0	1	1	1
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	0	1	0	0
1	0	1	0	1	1	1
1	1	0	1	0	0	1
1	1	1	1	0	0	1

Q: For the above circuit diagram fill in the following details

A: **No. of AND gates used: 2** **No. of AND gate IC used: 1**
No. of NOT gates used: 1 **No. of NOT gate IC used: 1**
No. of OR gates used: 1 **No. of OR gate IC used: 1**
Total No. of ICs used: 3

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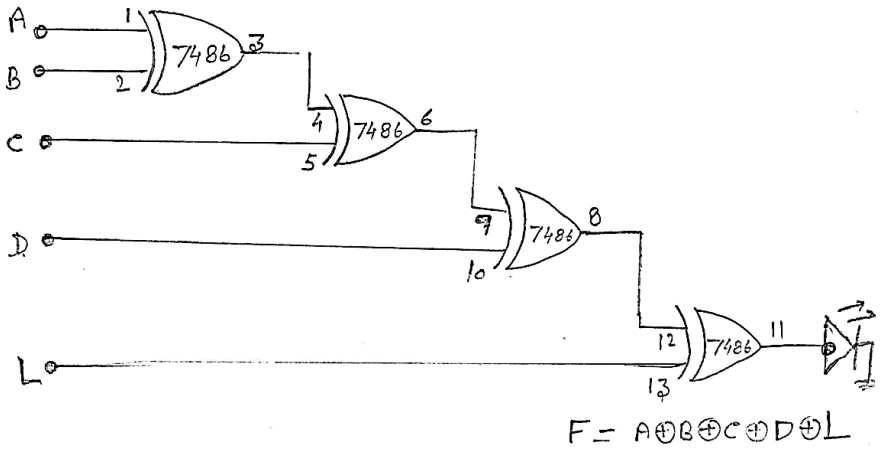
Run 2: Parity generator
Diagram



Q: How many XOR gates are used?
A: 4

Q: How many 7486 IC are used? Can the circuit be implemented using only **one** 7486 IC?
A: 1 and this circuit is possible even with a single 7486 IC because it has 4 XOR gates in it.

Q: Take any six-input combinations of your choice and complete the below table.
Truth Table

A	B	C	D	L	P
0	1	1	0	0	0
0	1	1	0	1	1
1	1	1	1	0	0
1	1	1	1	1	1
1	0	1	0	1	1
0	1	0	1	1	1

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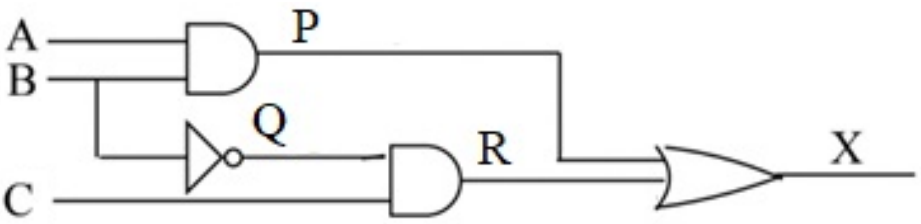
Software runs

Run 3: Circuit implementation

(a) Implement the below circuit using Gate level modeling, write the code as well as its testbench.

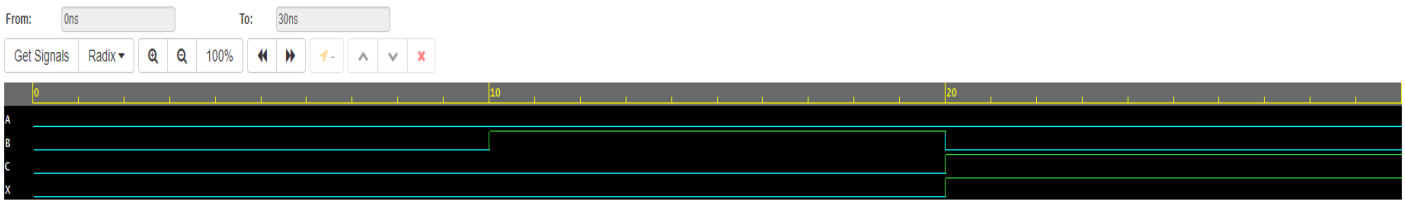



```
//design
module circuit(X, A,B,C);
input A,B,C;
output X;
wire P, Q, R;
and a1(P,A,B);
not (Q,B);
and (R,Q,C);
or (X,R,P);
endmodule

//testbench
module stimulus;
reg A,B,C;
wire X;
initial
begin
$dumpfile("dump.vcd");
$dumpvars(1, hamming_tb);
A=0; B=0; C=0;
#10 A=0; B=1; C=0;
#10 A=0; B=0; C=1;
#10 $stop;
end
circuit mycircuit(X,A,B,C);
endmodule
```

Q: Paste the Image of your **Simvision** window where you get the waveforms for the above code.

A:



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Run 4: Error detection and error correction codes

Q: Write Verilog code and testbench for generating even parity Hamming code for 4-bit data. (Hint: P0 = D2^D1^D0, P1 = D3^D1^D0, P2 = D3^D2^D0)

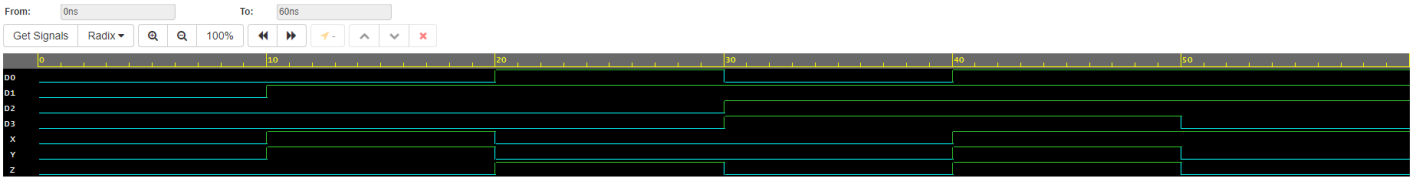
A: Verilog Code-

```
//design
module hamming (P0,P1,P2,D0,D1,D2,D3);
input D0,D1,D2,D3;
output P0,P1,P2;
xor (P0,D2,D1,D0);
xor (P1,D3,D1,D0);
xor (P2,D3,D2,D0);
endmodule

//testbench
module hamming_tb;
reg D0,D1,D2,D3;
wire X,Y,Z;
initial
begin
$dumpfile("dump.vcd");
$dumpvars(1, hamming_tb);
D0=0; D1=0; D2=0; D3=0;
#10 D0=0; D1=1; D2=0; D3=0;
#10 D0=1; D1=1; D2=0; D3=0;
#10 D0=0; D1=1; D2=1; D3=1;
#10 D0=1; D1=1; D2=1; D3=1;
#10 D0=1; D1=1; D2=1; D3=0;
#10 $stop;
end
hamming mycircuit(X,Y,Z,D0,D1,D2,D3);
endmodule
```

Q: Paste the Image of your **Simvision** window where you get the waveforms for the above code.

A:



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Assignment All assignments are to be submitted strictly before start of next lab session through online only. Late assignments will not be entertained and will be awarded '0' marks.
Copy-paste or type the unique URL of your assignment solution from website www.edaplayground.com for assignment questions. Please note that do not copy someone else's link as any kind of unfair means will result in academic misconduct and will be treated accordingly. All links for each user and each code are unique.

Q1: Implement a NOT gate using one 2-input NAND gate only. Write its verilog code also.
Ans: Link1: https://www.edaplayground.com/x/CMrj

Q2: Write Verilog code and testbench using data flow modeling for Y = ABC + AB +AC.
Ans: Link2: https://www.edaplayground.com/x/fMn3

Q3: Write Verilog code and testbench for detecting even parity error in 4 bit (3+1) binary number.
Ans: Link3: https://www.edaplayground.com/x/Cud8

Q4: Write Verilog code and testbench for generating even parity bit for 4-bit binary number. (Hint: you can use the structure of run-2 of this experiment also or y = A^B^C^D).

Ans: Link4: https://www.edaplayground.com/x/BAtA