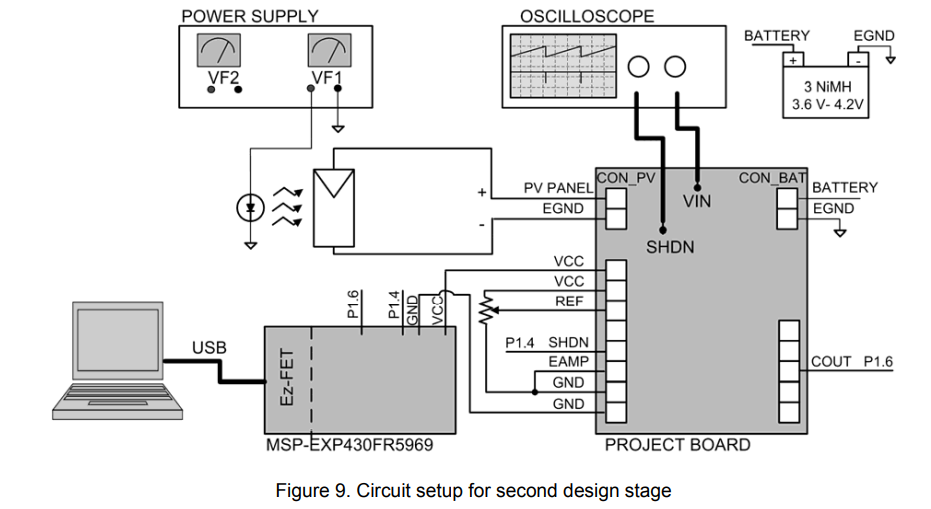
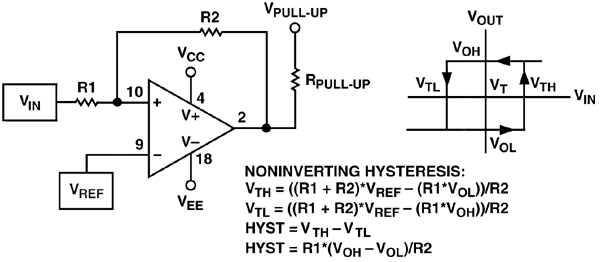
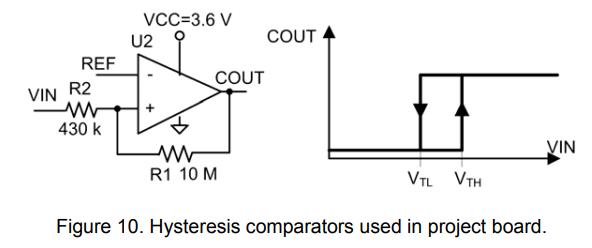
4. PULSE FREQUENCY MODULATION FOR A FIXED BIAS VOLTAGE The second design stage consists on controlling SHDN terminal to hold the bias voltage of input capacitor (VIN) into a hysteresis band gap. 4.1 Use the project board, MSP-EXPFR5969 and PV panels to build the circuit of Fig.9.



4.2 A potentiometer is used in this stage to set the value of REF. Analyse the circuit of Fig.10 and calculate the threshold values (VTL and VTH) with regards to REF.



https://www.analog.com/en/analog-dialogue/articles/curing-comparator-instability-with-hysteresis.html

V\_TL(V\_REF) = ((10M + 430k) \* V\_REF – (10M \* 0V)) / 430k

V\_TL(V\_REF) = ((10M + 430k) \* V\_REF – (10M \* 3.6V)) / 430k