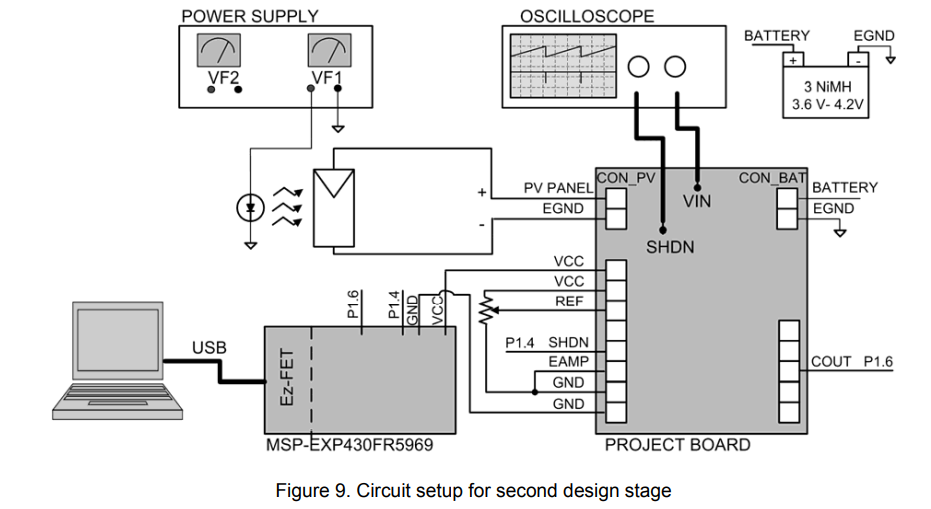
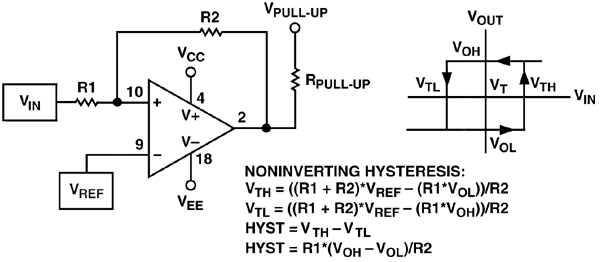
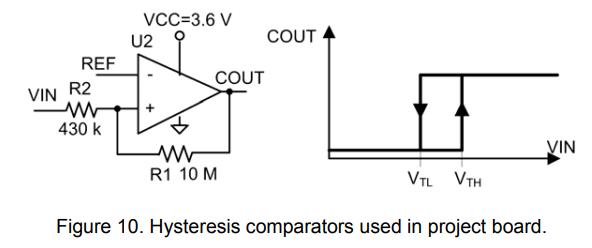
4. PULSE FREQUENCY MODULATION FOR A FIXED BIAS VOLTAGE The second design stage consists on controlling SHDN terminal to hold the bias voltage of input capacitor (VIN) into a hysteresis band gap. 4.1 Use the project board, MSP-EXPFR5969 and PV panels to build the circuit of Fig.9.



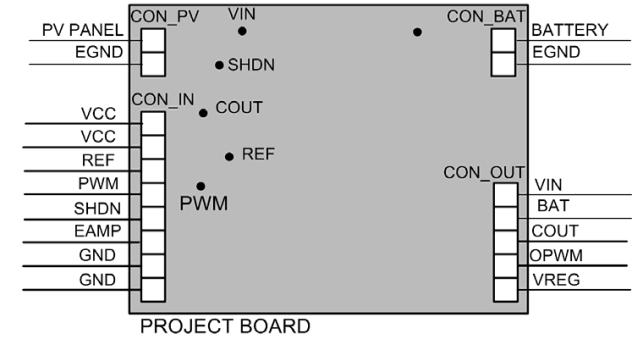
4.2 A potentiometer is used in this stage to set the value of REF. Analyse the circuit of Fig.10 and calculate the threshold values (VTL and VTH) with regards to REF.



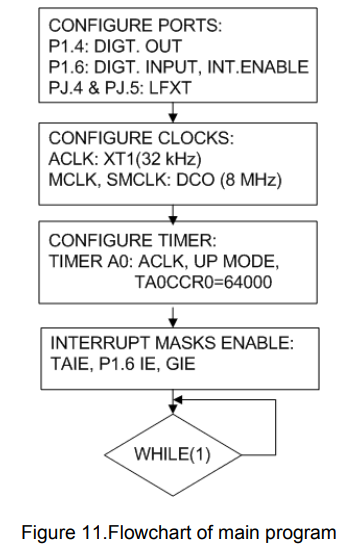
https://www.analog.com/en/analog-dialogue/articles/curing-comparator-instability-with-hysteresis.html

V\_TL(V\_REF) = ((10M + 430k) \* V\_REF – (10M \* 0V)) / 430k

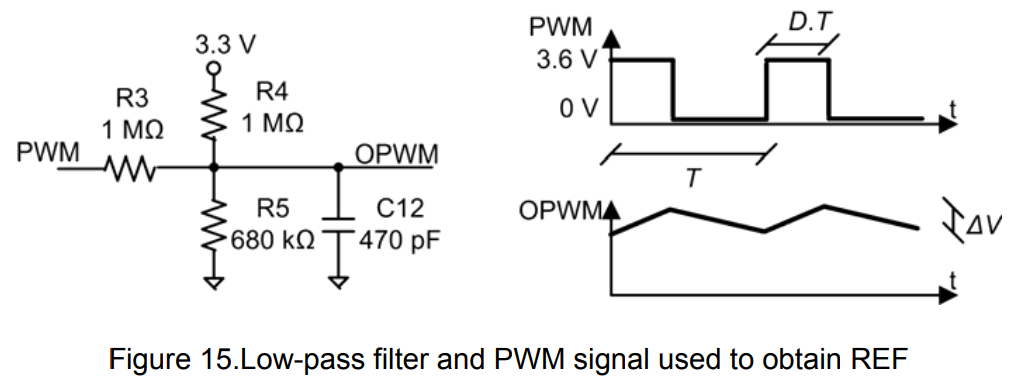
V\_TL(V\_REF) = ((10M + 430k) \* V\_REF – (10M \* 3.6V)) / 430k



4.3 Program the subroutines to control SHDN signal from the comparator output COUT and observe VIN and SHDN in the oscilloscope. The program comprises a main program and two interrupt services (Timer A and P1.6). The main program configures general digital ports, clocks, timer A and interrupts masks as is shown in Fig.11. Do not configure non used ports.



5. REFERENCE VOLTAGE GENERATION The objective of this design stage is software control of photovoltaic panel’s bias voltage (REF). This analogue signal is obtained from the average value of a PWM signal (OPWM). The low-pass filter used in the project board is shown in Fig.15. Figure 15.Low-pass filter and PWM signal used to obtain REF



5.1 Use the circuit of Fig.15 to calculate the value of OPWM versus the value of PWM’s duty cycle (D).

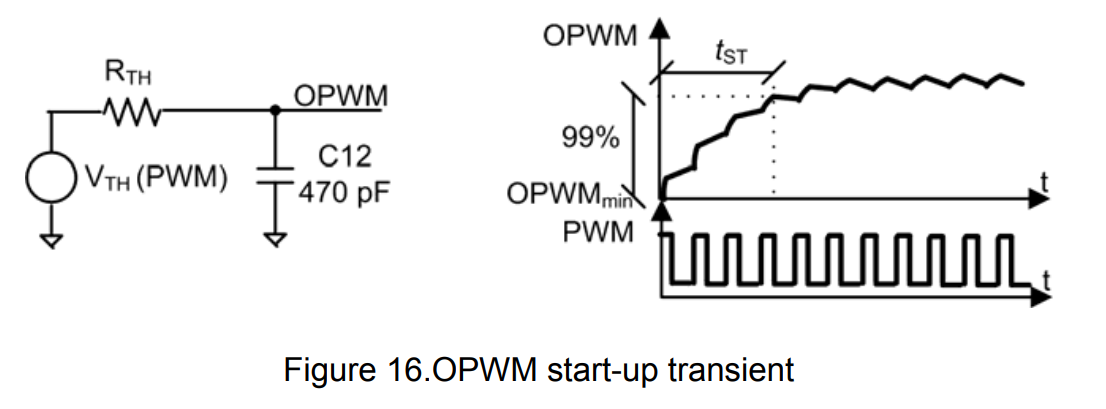
5.2 Considering that T=TBCCR0/fDCO (fDCO=8 MHz and TBCCR0=25), calculate the maximum voltage ripple of OPWM in full range of D. The voltage ripple is so small that the slopes of OPWM can be considered constants during charge and discharge states (linear OPWM shapes).

T = 25/8e6 = 0,000003125s = 3,125 µs

is equal to 320kHz

U\_C = U\_0 \* e^(-(t/R\*C)) = 3,6

5.3 The analogue signal generator must be fast enough disabled or enabled to save energy (dynamic power management). Calculate the value of RTH and VTH of the Thevening equivalent circuit shown in Fig.16 and deduce the time length (tST) needed to reach the 99% of final value.



U\_C = U\_0 \* 1 - e^(-(t/R\*C)) = t (99%) = 1,6ms

5.4 Connect the boards and instruments as shown in Fig.17. The potentiometer is substituted by the analogue signal OPWM. The PWM signal is obtained from P1.5 and OPWM is connected to REF. If it is possible, use a 10:1 oscilloscope’s probe to measure OPWM (=REF). Otherwise, the use of a 1:1 probe would modify the waveform of OPWM because the probe’s impedance (1 MΩ) has the same order of magnitude than RTH.

