野火_ZYNQ7010/20 BTB 核心板_原理图_V1.1

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东莞野火电子技术有限公司
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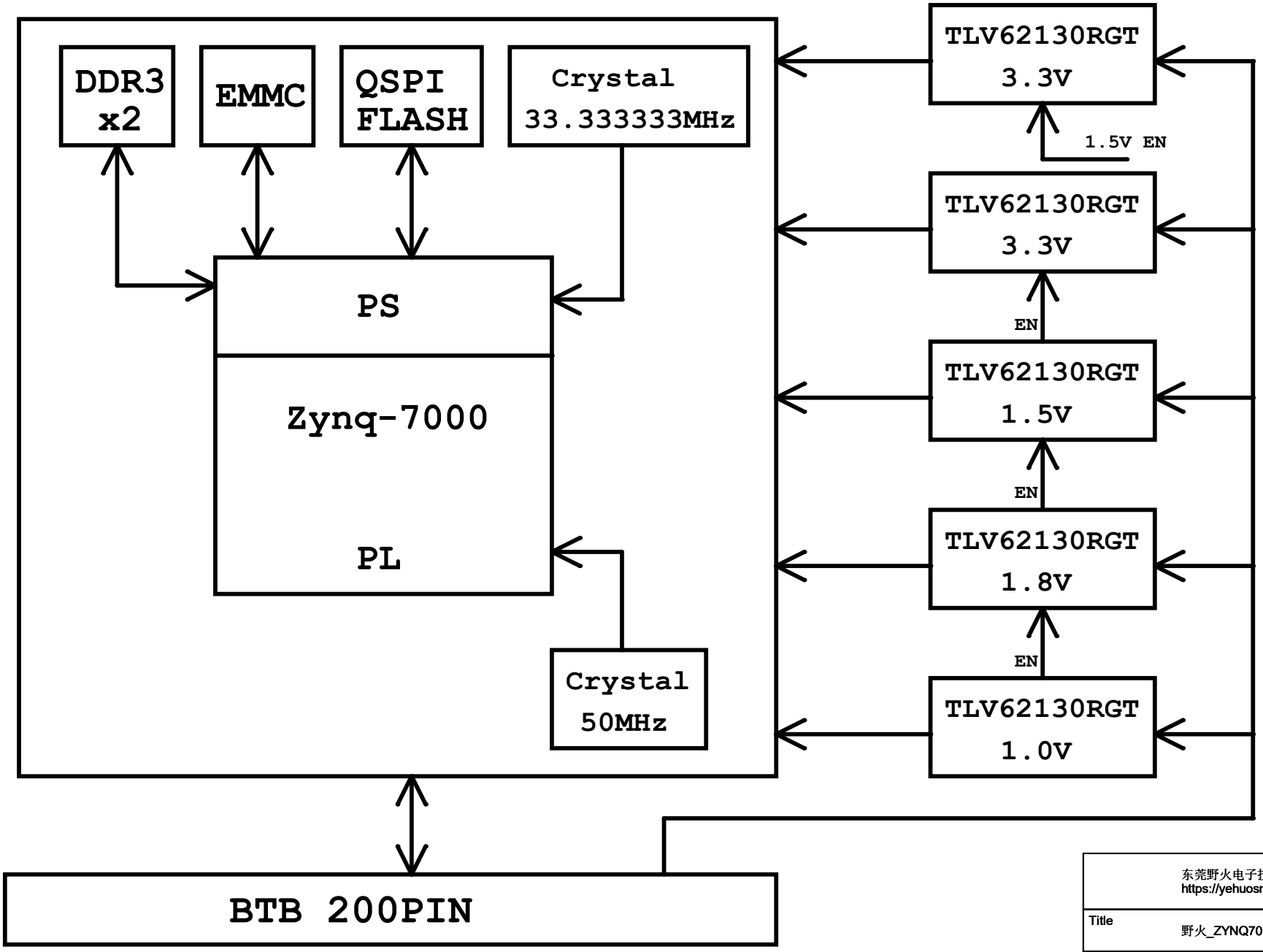
历史版本

版本号	日期	设计	描述
V1.0	2020-10-26	xgh	初始版本
V1.1	2023-06-26	GHS	BTB初始版本



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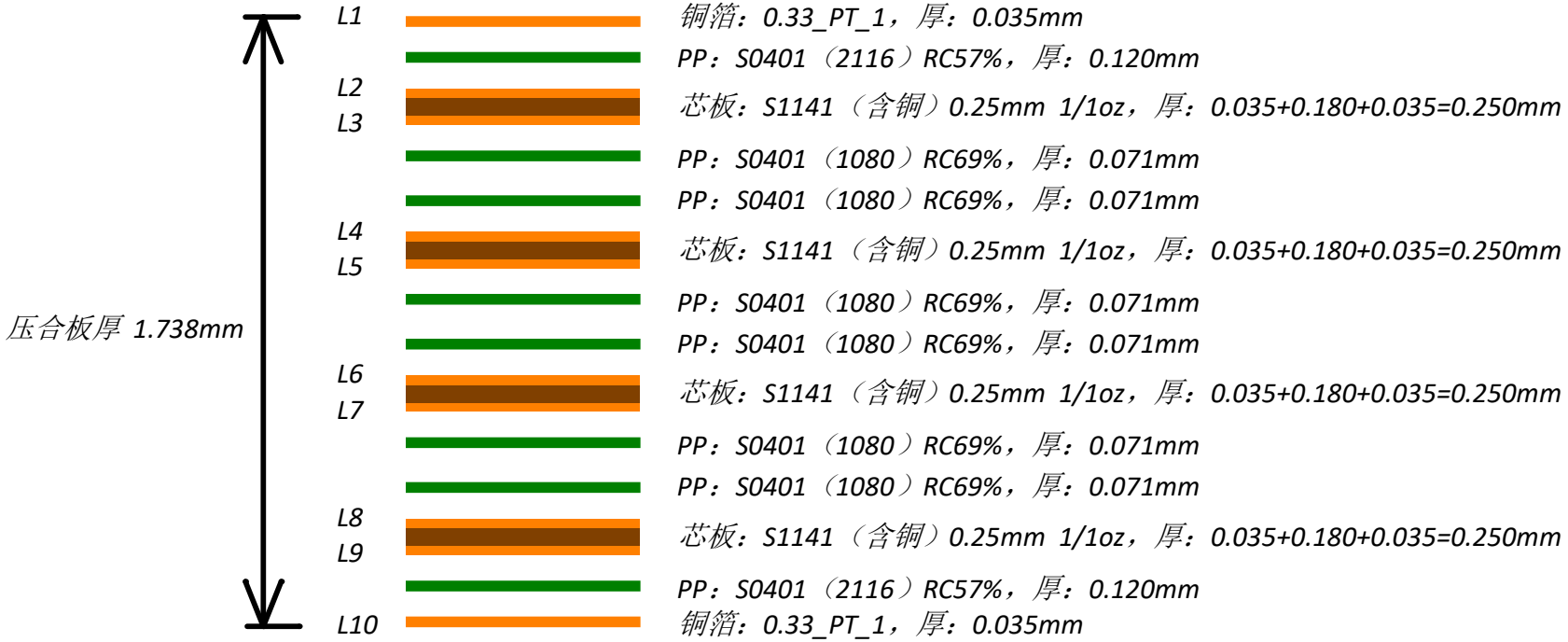
ebf_xc7z010/020 core board



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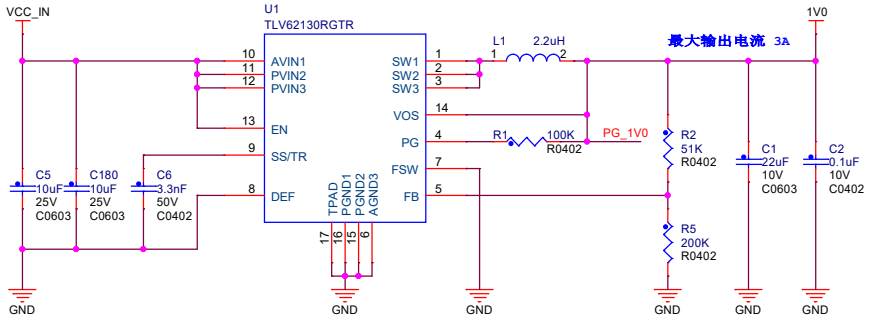
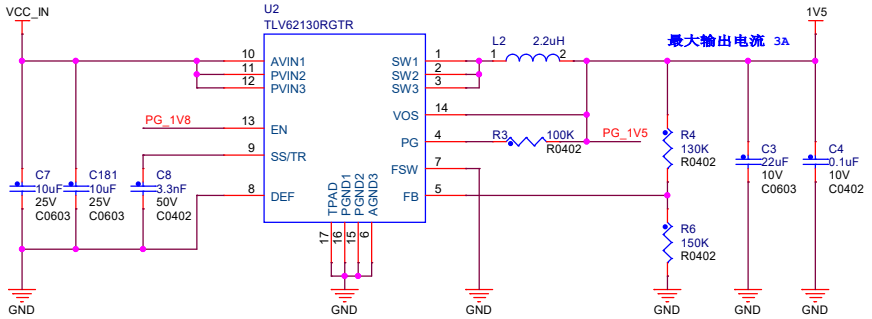
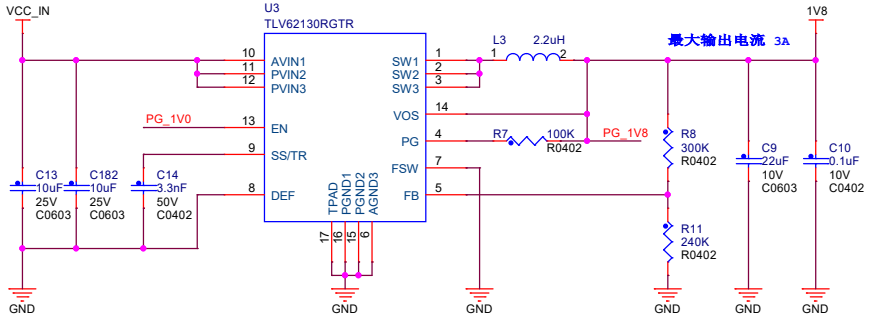
POWER 1.0V



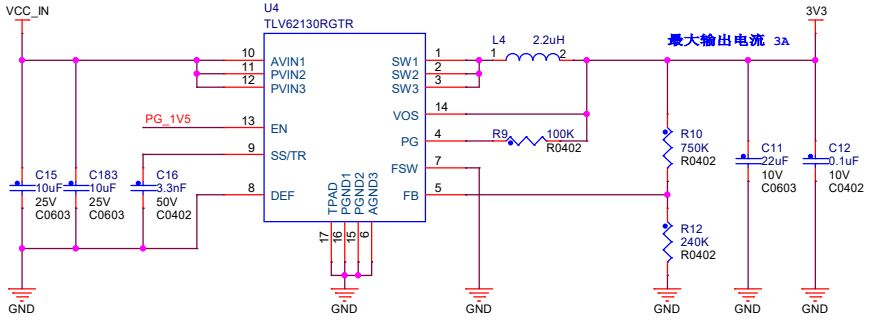
POWER 1.5V



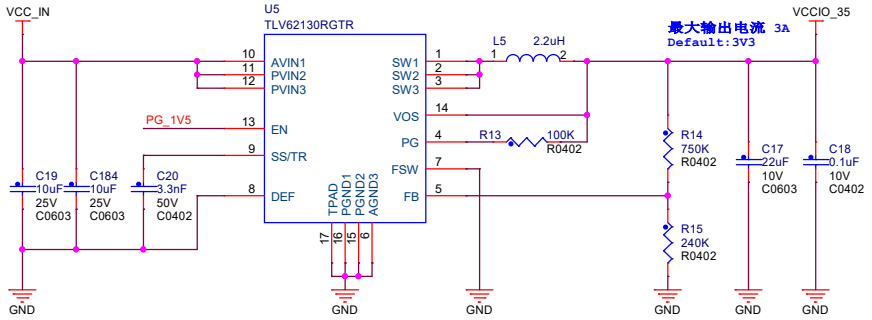
POWER 1.8V



POWER 3.3V



POWER VCCIO_35



Power IN Voltage 5V~12V

Open sequence

1.0V->1.8V->1.5V->3.3V->VCCIO_35

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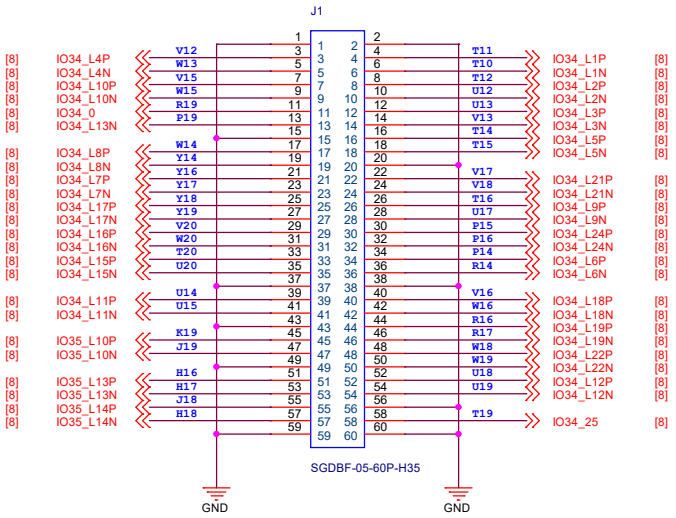
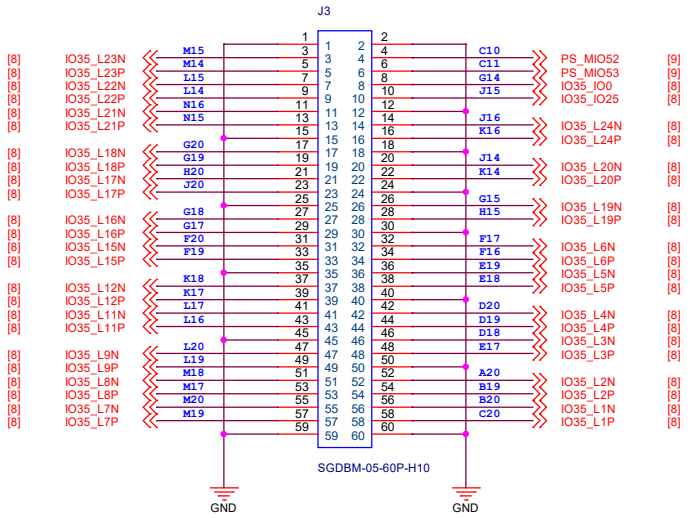
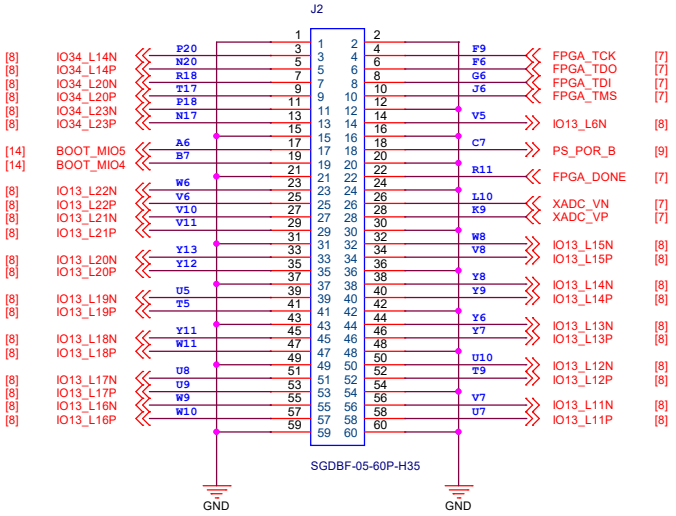
BTB Connector

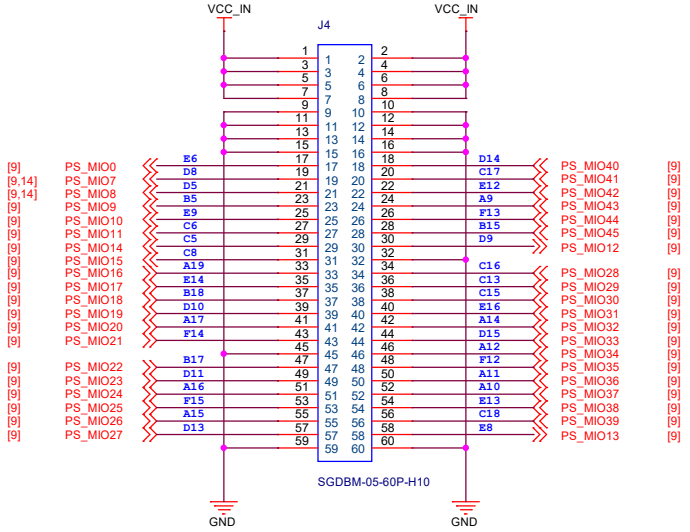
60*4个引脚包含

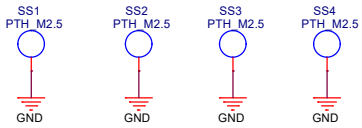
XADC	2
POR	1
DONE	1
PS_IO	42
PL_IO	124
JTAG	4
12V输入	8
GND	55
BOOT	2











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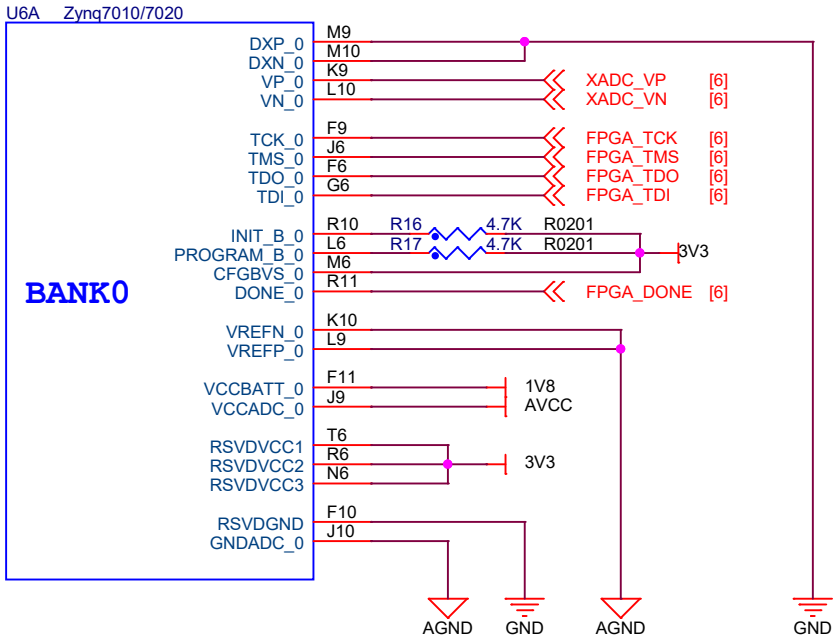
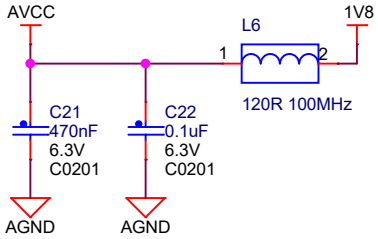
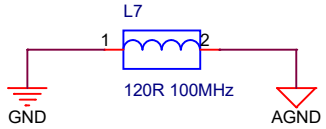
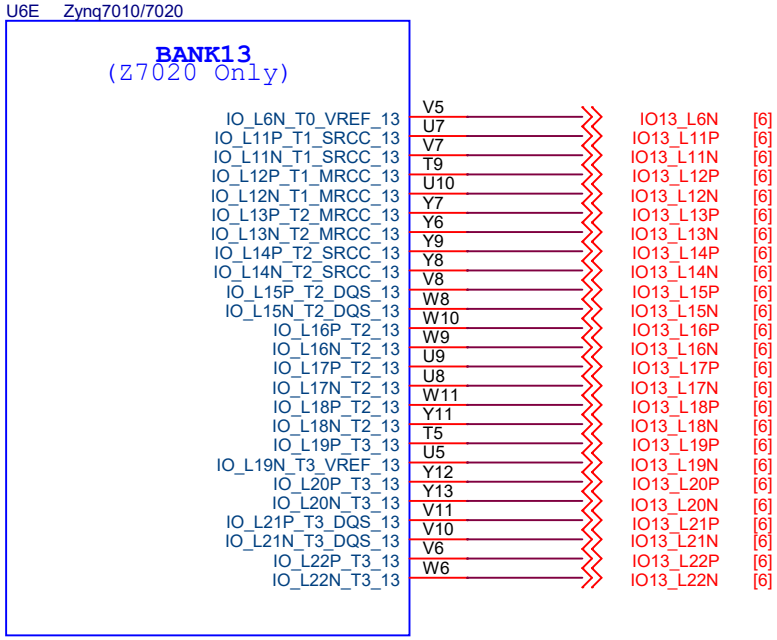
BANK0







BANK13



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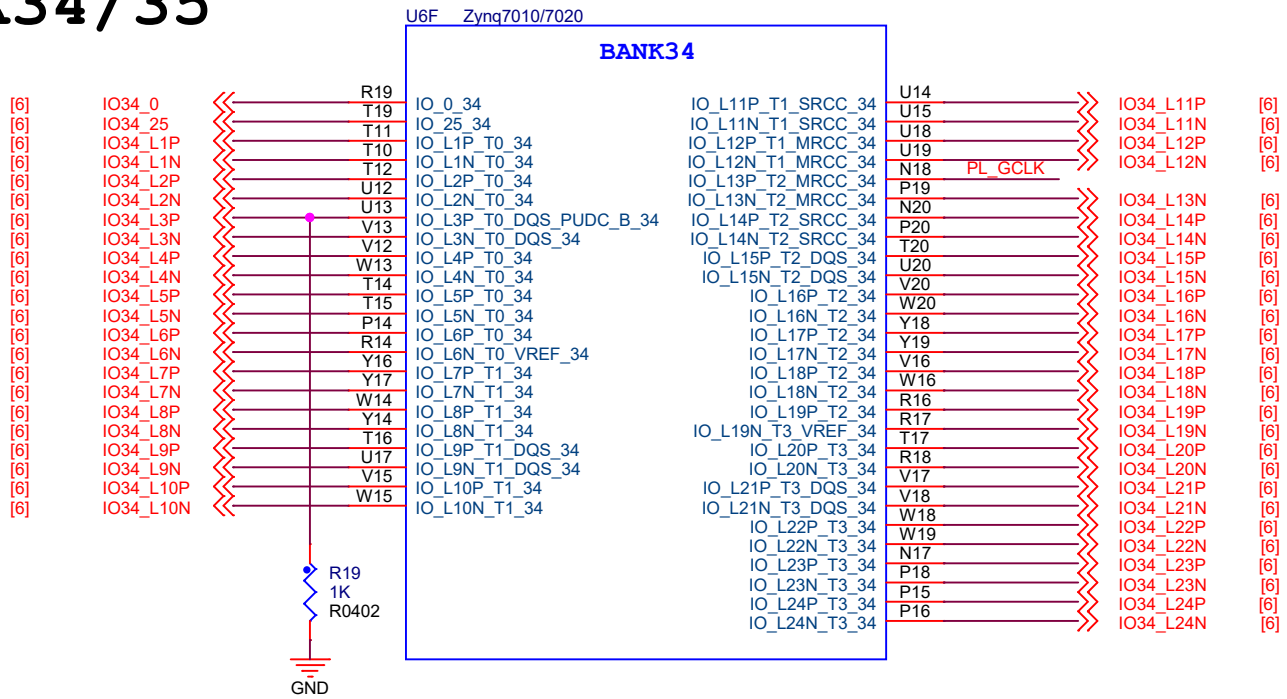
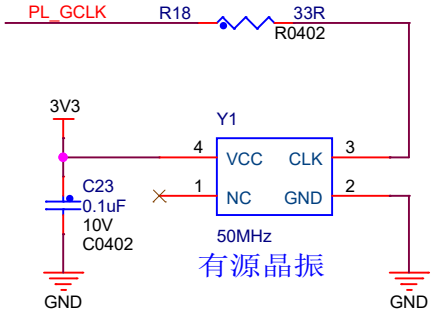
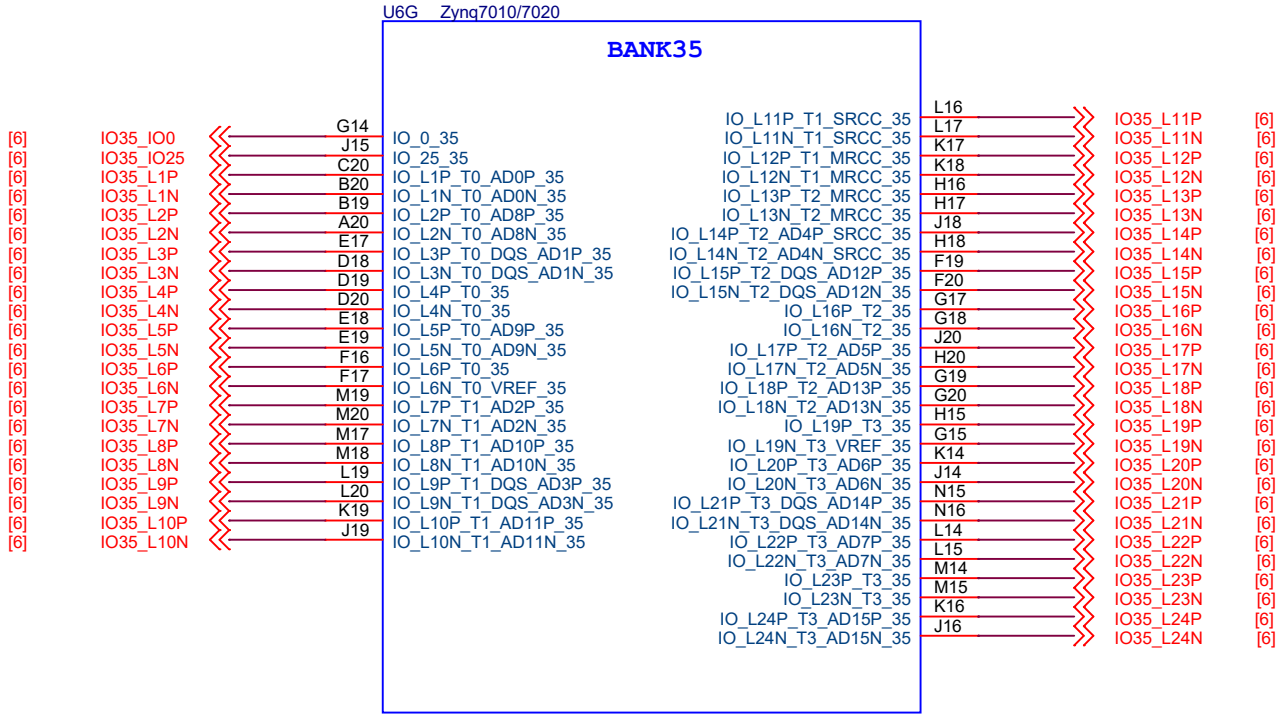
BANK34/35







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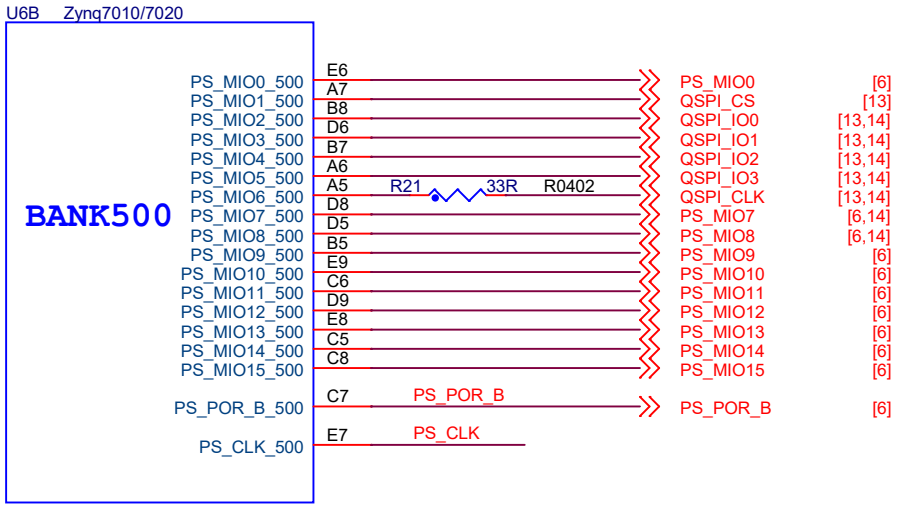
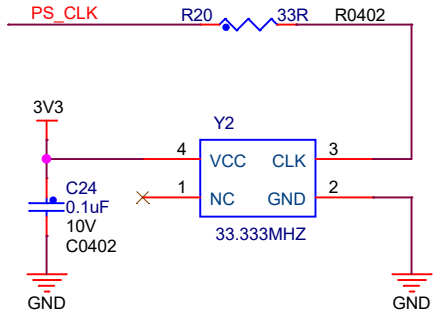
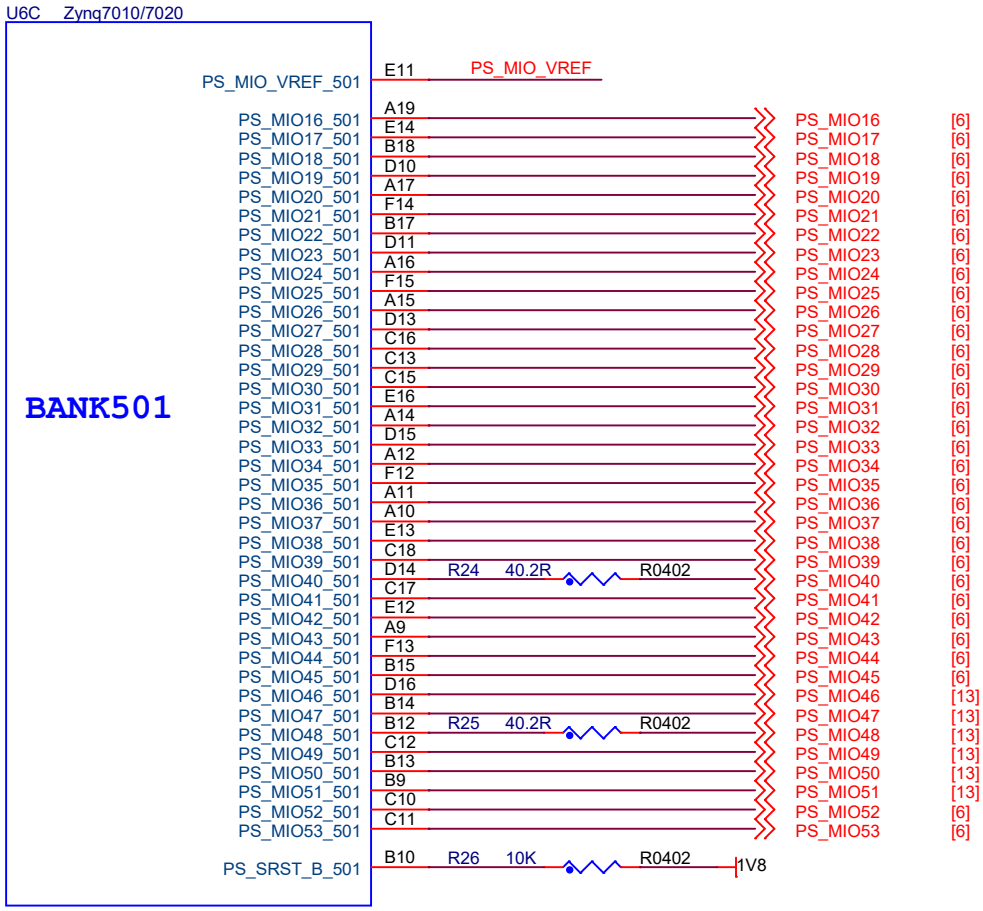
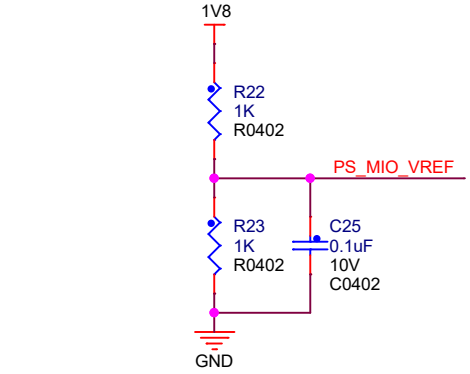
BANK500/501









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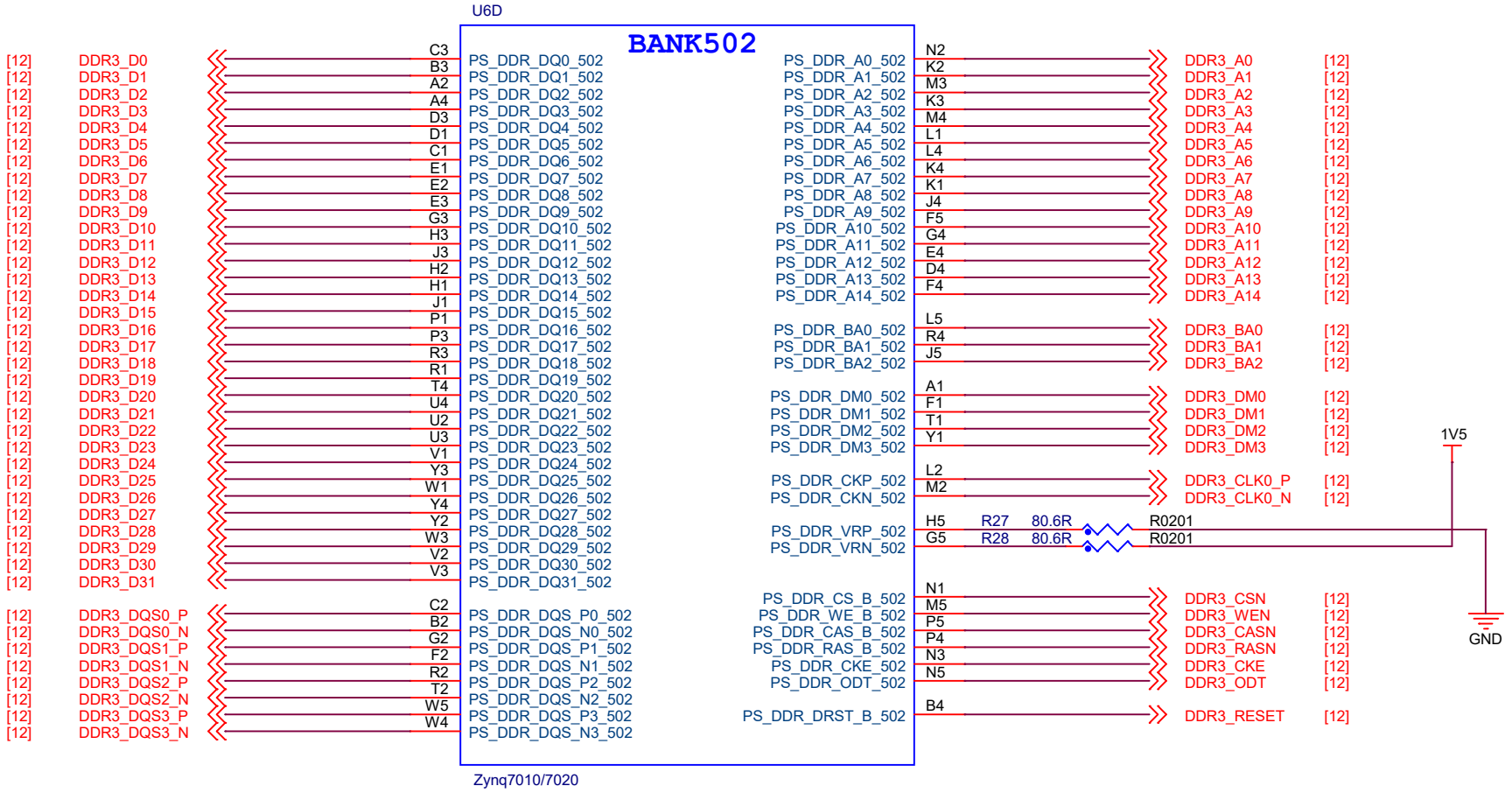
BANK502



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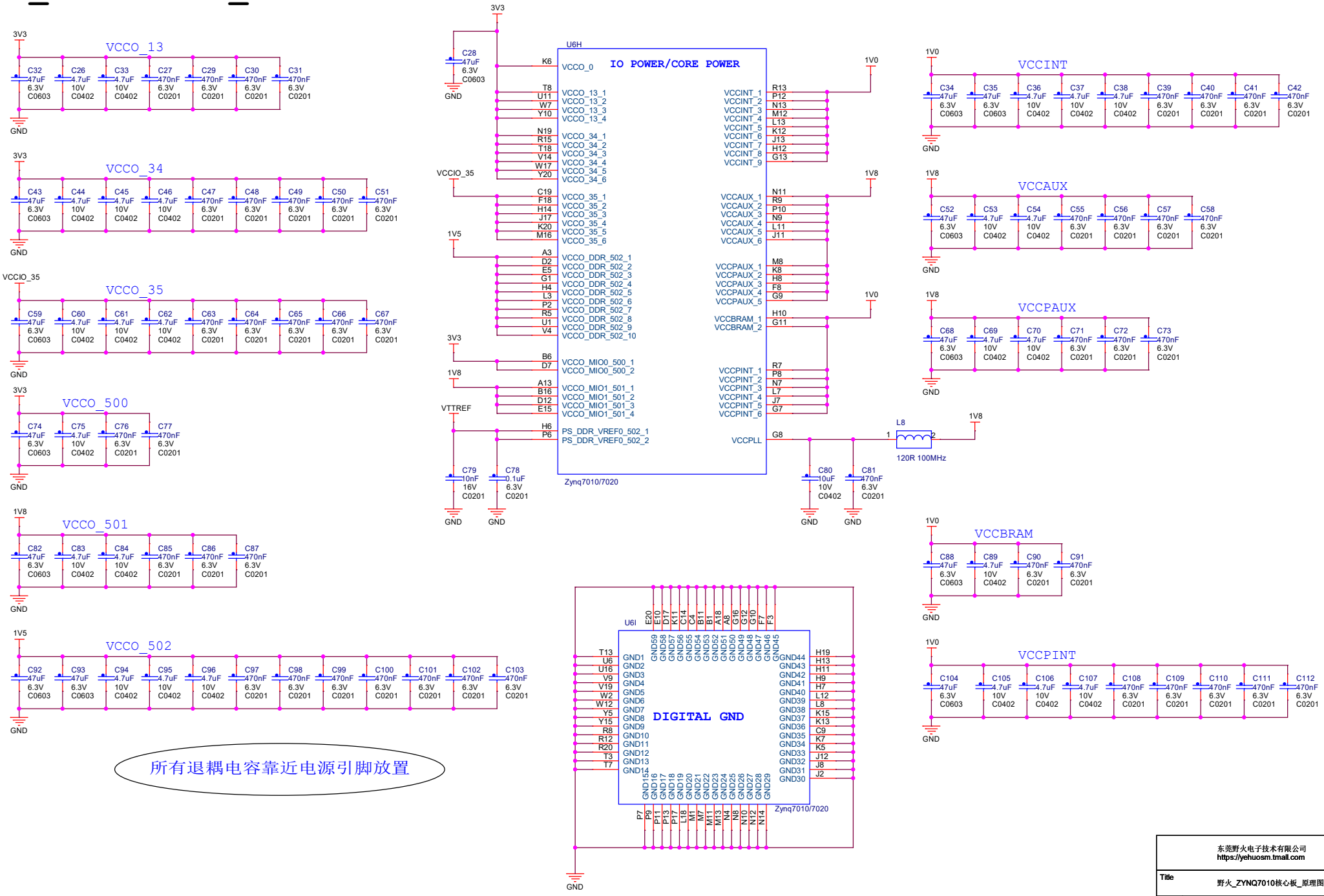
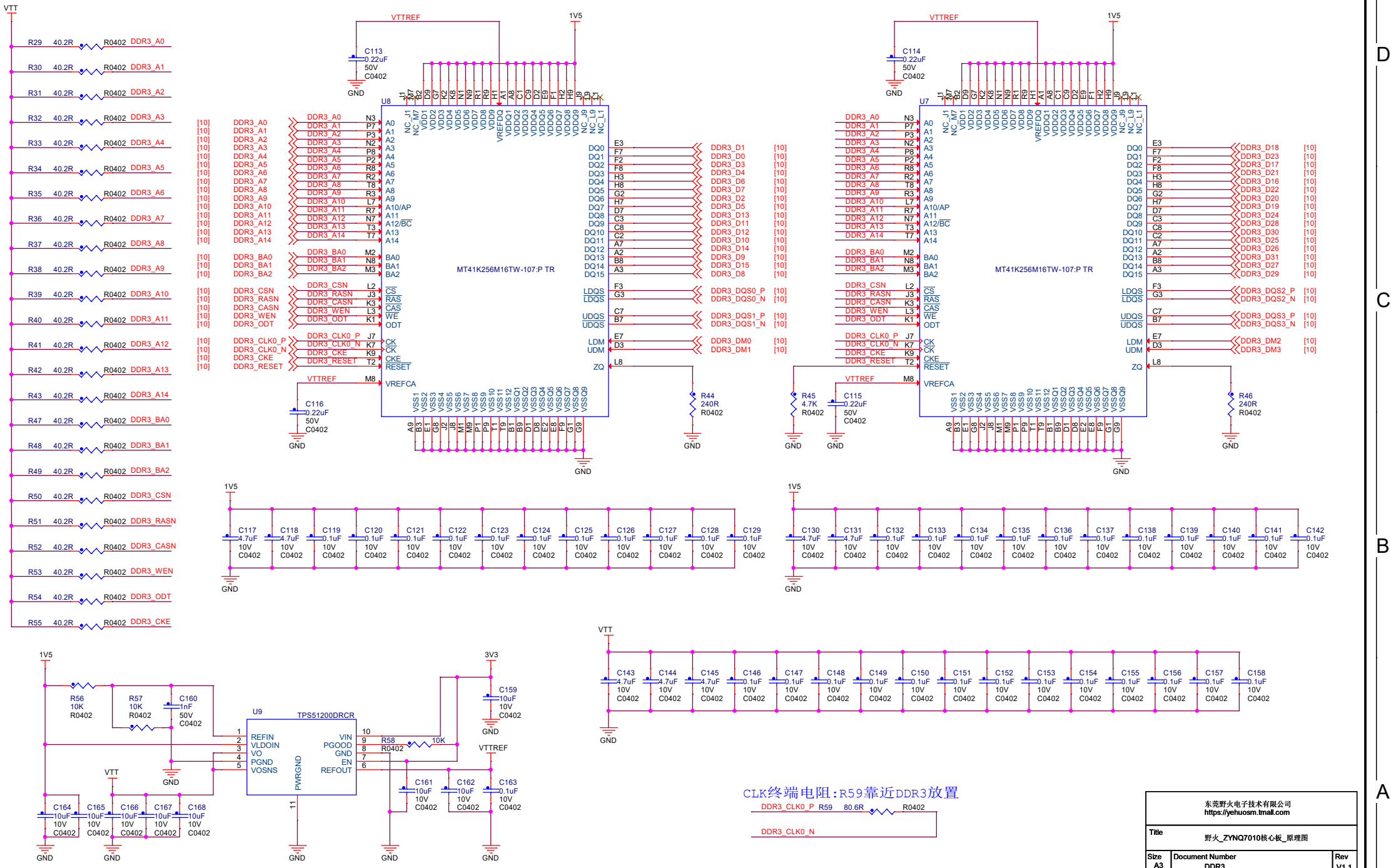
IO_POWER/CORE_POWER



DDR3



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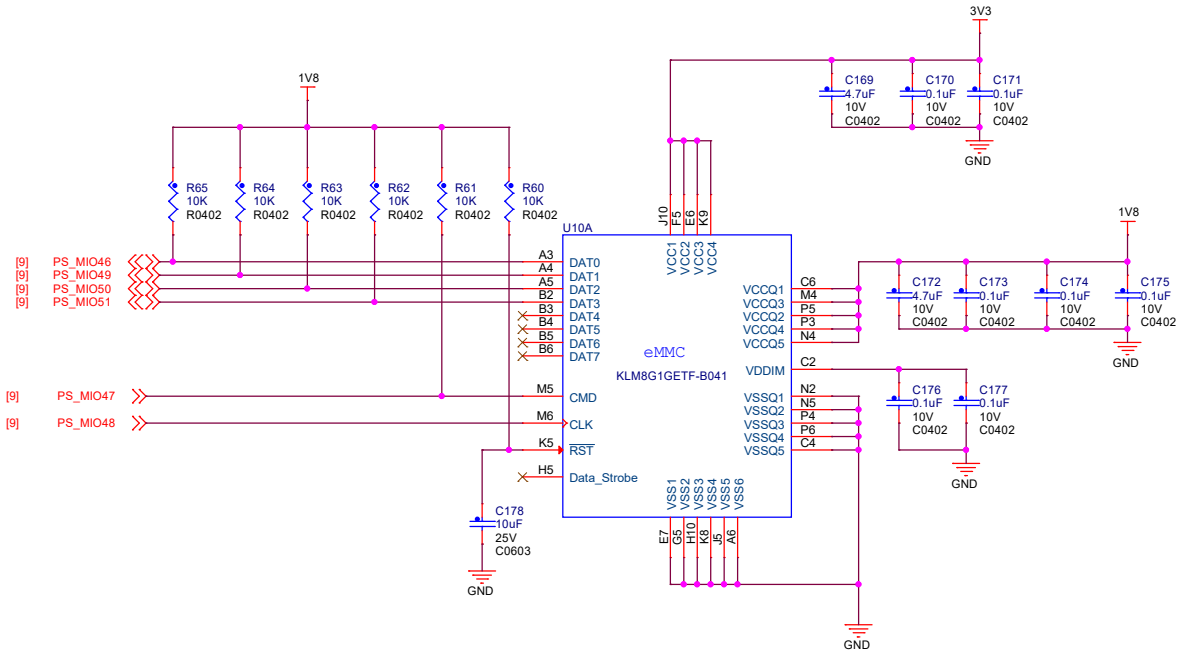
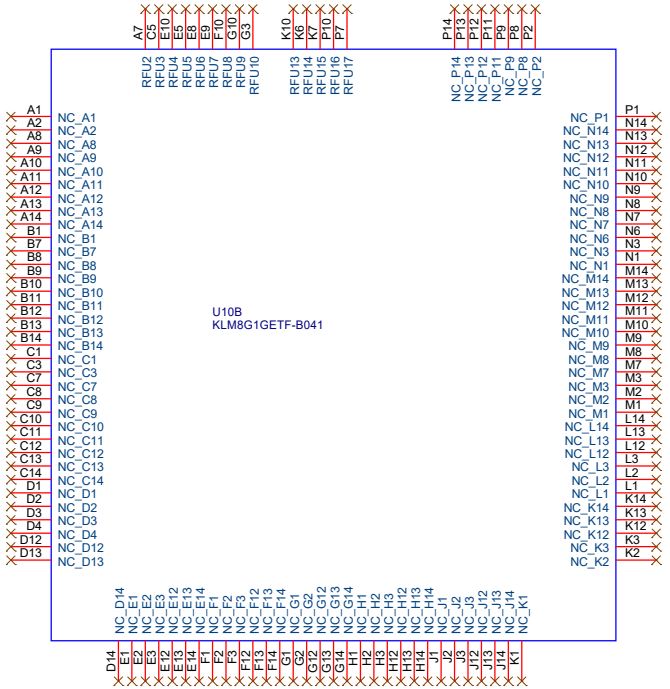
eMMC

默认容量为8G字节





SPI_FLASH

容量：16M字节

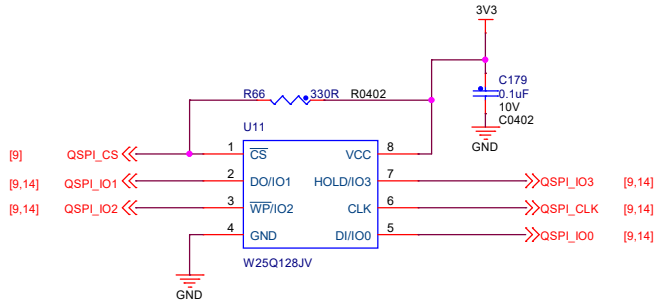


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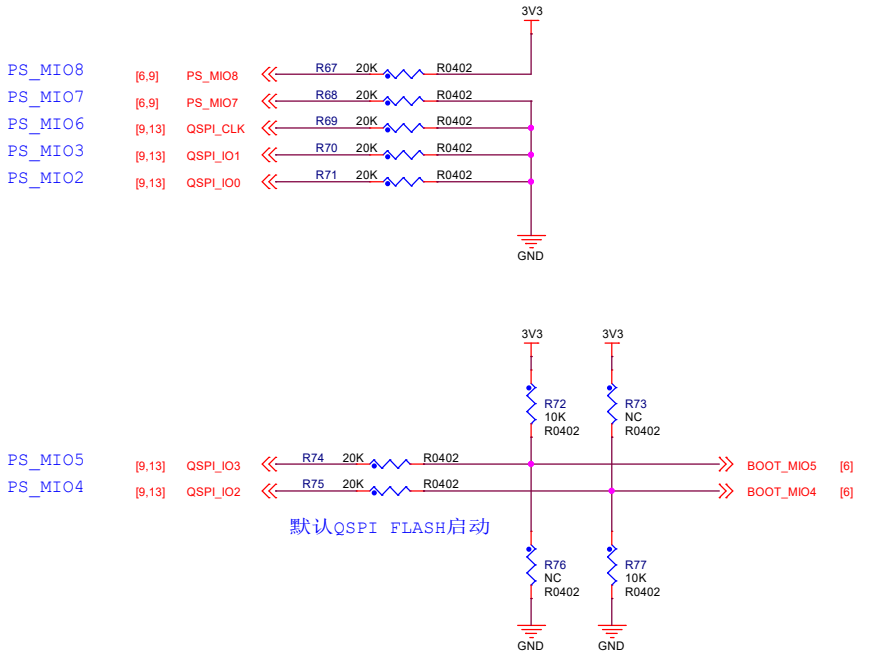
Table 6-4: **Boot Mode MIO Strapping Pins**

Pin-signal / Mode	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]
	VMODE[1]	VMODE[0]	BOOT_MODE[4]	BOOT_MODE[0]	BOOT_MODE[2]	BOOT_MODE[1]	BOOT_MODE[3]
Boot Devices							
JTAG Boot Mode; cascaded is most common(1)				0	0	0	**JTAG Chain Routing(2)** 0: Cascade mode 1: Independent mode
NOR Boot(3)				0	0	1	
NAND				0	1	0	
Quad-SPI(3)				1	0	0	
SD Card				1	1	0	
Mode for all 3 PLLs							
PLL Enabled			0	Hardware waits for PLL to lock, then executes BootROM.			
PLL Bypassed			1	Allows for a wide PS_CLK frequency range.			
MIO Bank Voltage(4)							
	Bank 1	**Bank 0**	Voltage Bank 0 includes MIO pins 0 thru 15. Voltage Bank 1 includes MIO pins 16 thru 53.				
2.5 V, 3.3 V	0	0					
1.8 V	1	1					

Notes:

1. JTAG cascaded mode is most common and is the assumed mode in all the references to JTAG mode except where noted.
2. For secure mode, JTAG is not enabled and MIO[2] is ignored.
3. The Quad-SPI and NOR boot modes support execute-in-place (this support is always non-secure)
4. Voltage Banks 0 and 1 must be set to the same value when an interface spans across these voltage banks. Examples include NOR, 16-bit NAND, and a wide TPIU test port. Other interface configuration may also span the two banks.



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