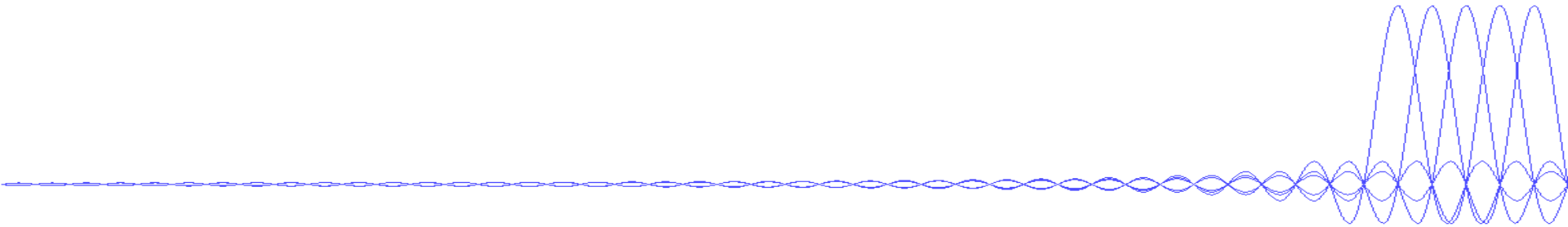
COMPUTER ENGINEERING

UIT
TRƯỜNG ĐẠI HỌC
CÔNG NGHỆ THÔNG TIN

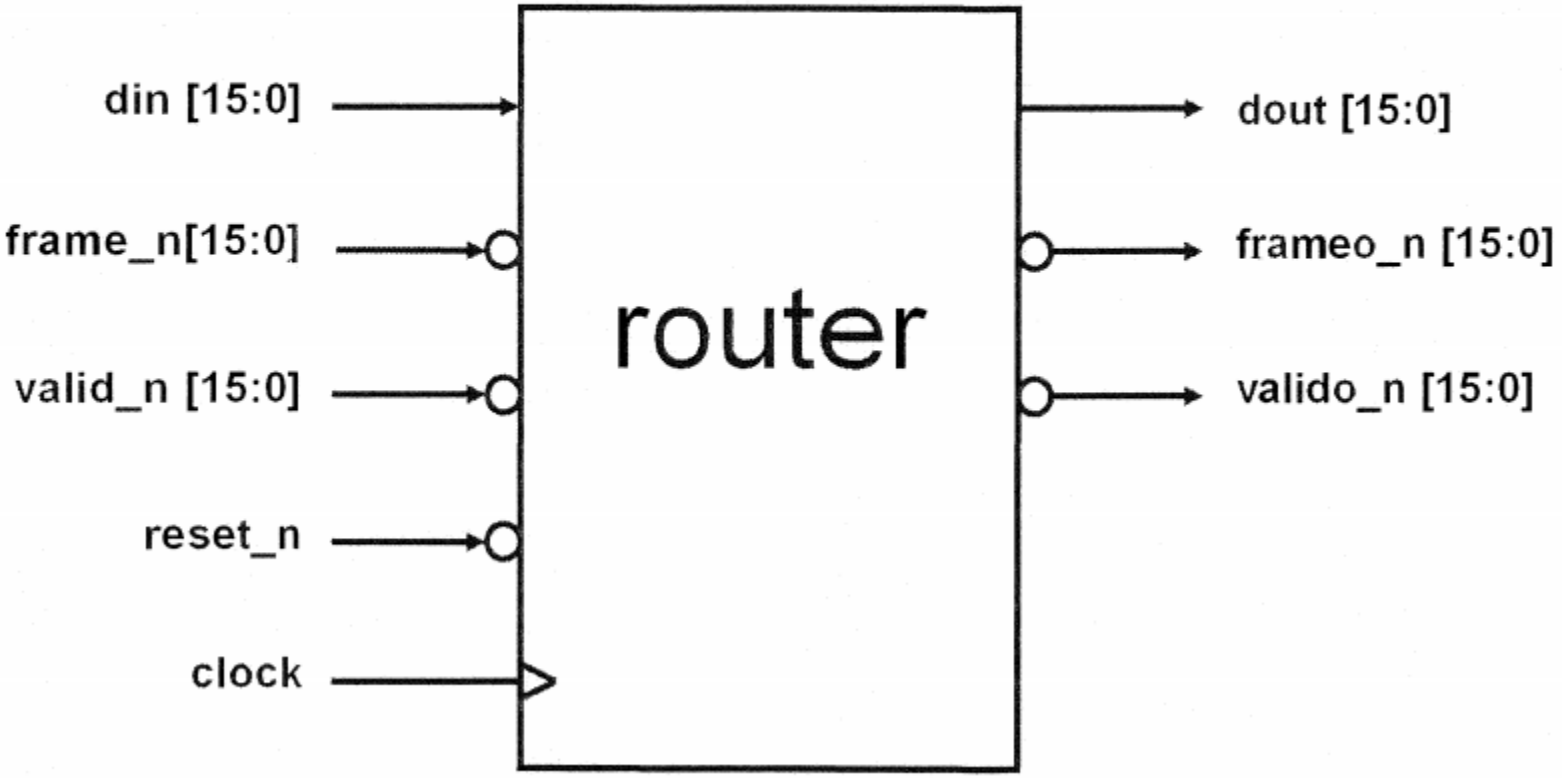
SYSTEMVERILOG VERIFICATION ENVIRONMENT



DUT
Overview

A router:

16 x 16 crosspoint switch



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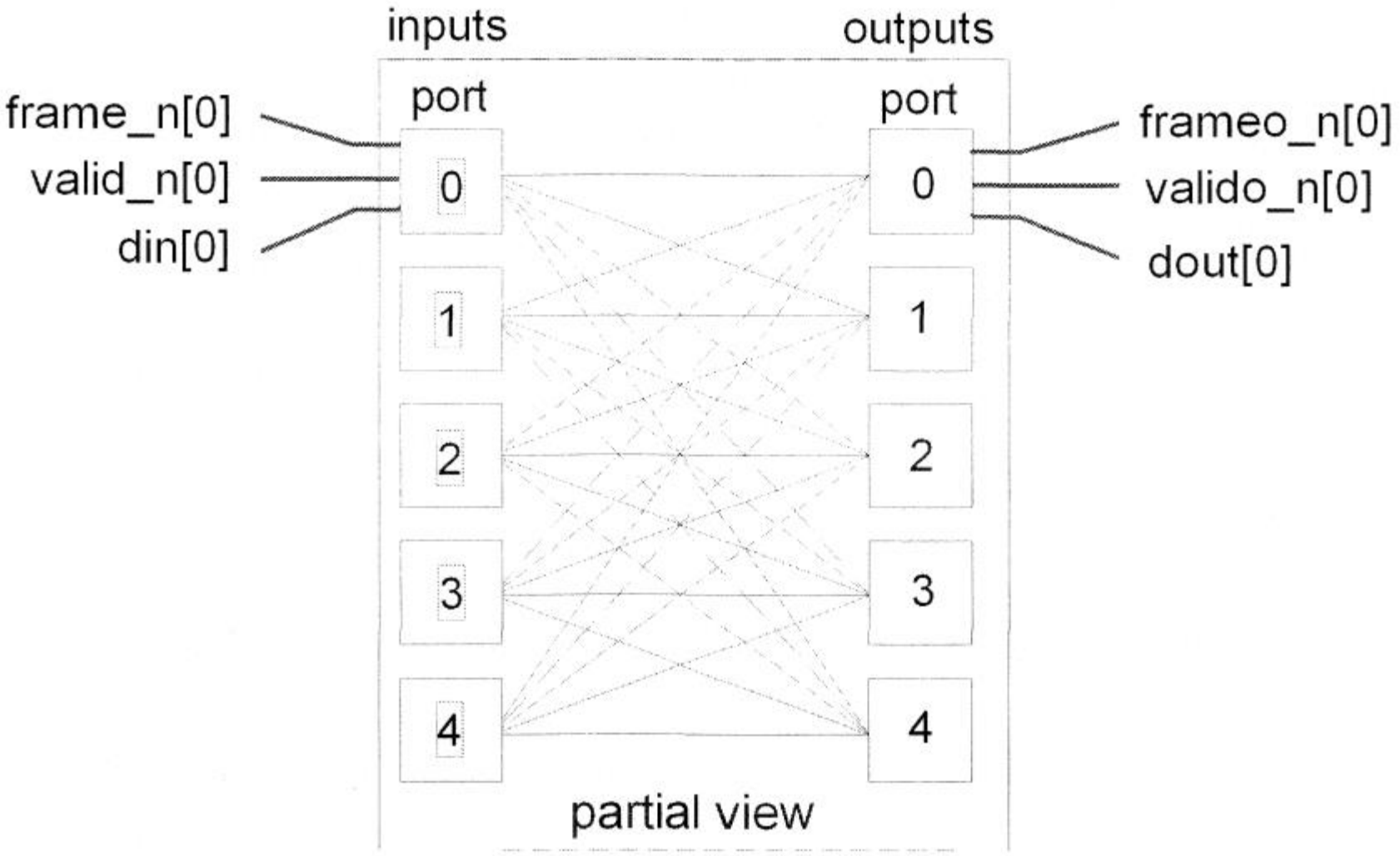
DUT
Description(1)

- The router has 16 input and 16 output ports
  - Each input and output port consists of 3 singles: data, frame, valid
  - These signals are represented in a bit-vector format (din[15:0], dout[15:0], …)

- To driver or sample an individual port, the specific bit position corresponding to the port number must be specified
  - For example, if input port 3 is to be driven, then the corresponding signals shall be din[3], frame_n[3] and valid_n[3]
  - For example, if output port 7 is to be sampled, then the corresponding signals shall be dout[7], frameo_n[7] and valid_n[7]

DUT
Description(2)



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Description (3)

- **Single positive-edge clock**
- **Input and output data are serial (1 bit / clock)**
- **Packets are sent through in variable length:**
  - Each packet is composed of two parts
    - Header
    - Payload
- **Packets can be routed from any input port to any output port on a packet-by-packet basis**
- **No internal buffering or broadcasting (1-to-N)**

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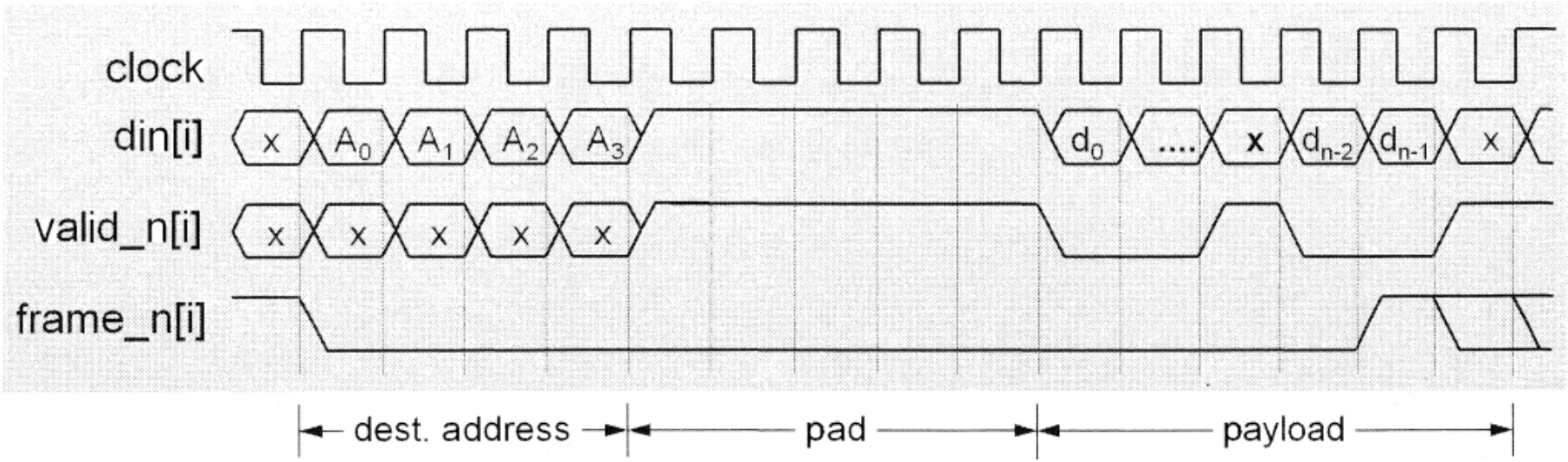
Input packet structure

- **frame_n:**
  - Falling edge indicates first bit of packet
  - Rising edge indicates last bit of packet
- **din:**
  - Header (destination address & padding bits) and payload
- **valid_n:**
  - valid_n is low if payload bit is valid, high otherwise



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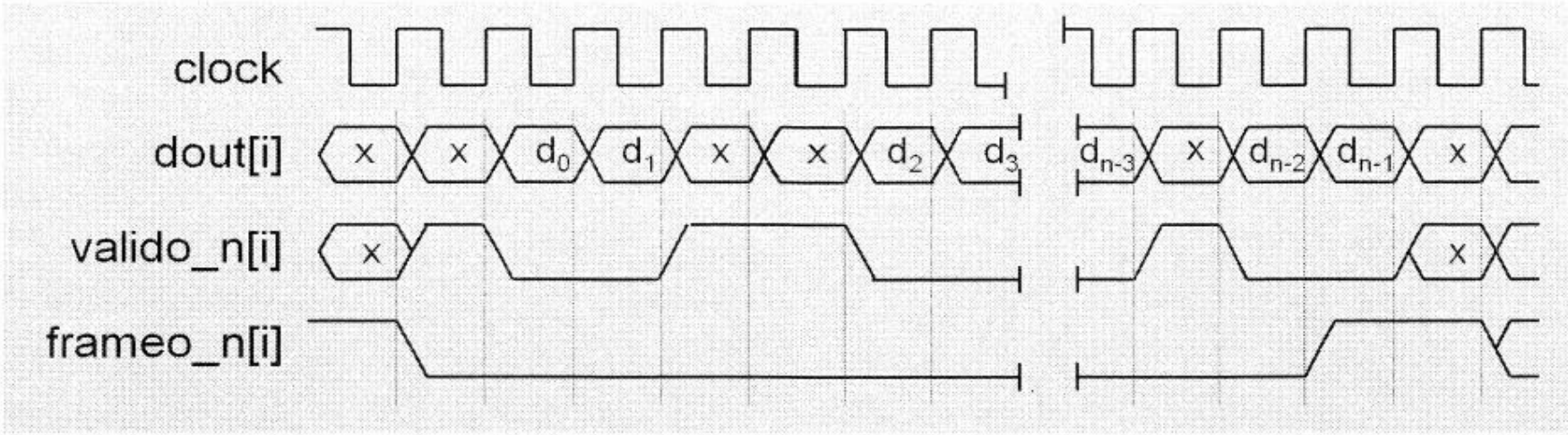
Output packet structure

- **Output activity is indicated by: frameo_n, valido_n, and dout**
- **Data is valid only when:**
  - frameo_n output is low (except for last bit)
  - valido_n output is low
- **Header field is stripped**



DUT
Reset signal

- **While asserting `reset_n`, `frame_n` and `valid_n` must be de-asserted**
- **`reset_n` is asserted for at least one clock cycle**
- **After de-asserting `reset_n`, wait for 15 clocks before sending a packet through the router**