Contributed paper

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Influence of junction parameters on the open circuit voltage decay in solar cells

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Starting from the general equivalent model of a solar cell including junction capacitance and shunt resistance connected with surface recombination of photocarriers, the phenomenon of open circuit voltage decay was analysed. The time decay of a photovoltage is influenced by the junction capacitance time constant to a great extent. The time constants of both depletion layer and diffusion capacitances varying with applied bias voltage were examined. The detailed analysis of these time constants allowed for evaluation of the forward bias voltage that should be applied to c-Si solar cell to minimize this detrimental effect. As it was shown, that voltage bias can be easily generated by the constant illumination, the so-called bias light. Impedance measurements of solar cells in the frequency range 10 Hz–100 kHz and with varying voltage bias allowed for additional characterisation of the junction capacitance and resistance. The measured parameters agree well with these used in model calculation of a photovoltage decay.

Keywords: junction capacitance, open circuit voltage decay, solar cell.

1. Introduction

The minority carriers lifetime τ and the effective surface recombination velocity S_{eff}, important recombination parameters influencing the efficiency of a solar cell, are often determined with the dynamic methods. The known photovoltage decay method, intuitively simple, is often developed for determination of carriers lifetime in the solar cells. However, the results obtained in different laboratories are not consistent in many cases. This can be connected with uncertainty of selecting the relevant decay region. Another obstacle is the influence of cell junction parameters, essentially capacitance, which should be taken into account. The time constant introduced by a junction capacitance causes that the carriers lifetime can be overestimated. The influence of recombination in the junction and leakage caused by shunt resistance lead to underestimation of the lifetime (see Fig. 1). These additional effects can be compensated or even cancelled under certain measurement conditions.

The compensation procedure was analysed in detail by Green in Ref. 1. The analysis was based on the observation that in the continuity equation for the diode with the junction capacitance C_j and the shunt resistance R_{sh}

$$-\frac{V}{R_{sh}} - C_j \frac{dV}{dt} = \frac{dQ_B}{dt} + \frac{Q_B}{\tau_B}\text{s},$$

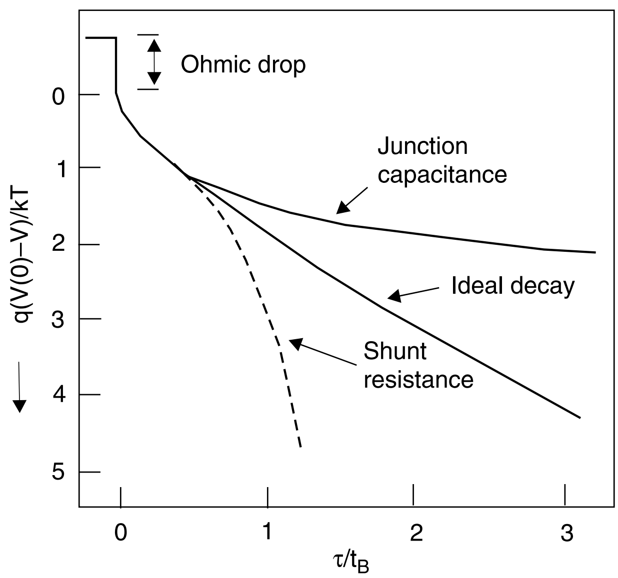

Fig. 1. Schematic description of the open circuit voltage decay for a wide-base diode. The influence of junction capacitance and shunt resistance on the decay are shown.

where Q_B is the excess minority carrier charge within the base, the two terms on the left side have opposite sign during the voltage decay. Examining the differential of the decay and adding some passive elements, it is possible to adjust the degree of cancellation and to get direct reading of estimated carrier lifetime.

The authors performed an analysis of the time constant introduced by junction capacitance, varying with the forward

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voltage applied to the n-p diode, and shunt resistance. The capacitance of the diode under forward voltage bias was considered as consisting of both depletion layer (barrier) capacitance C_j and diffusion capacitance C_d. In conclusion, we determined the magnitude of forward bias voltage, generated by, e.g., the bias light, necessary to avoid the influence of above parameters on the observed voltage decay.

2. Analysis of alternating current model of solar cell

Although the diode model of solar cell is widely known, it is used mostly at the steady state conditions. The alternating current (AC) model, useful in a transient analysis, should include the existing capacitances (see Fig. 2).

When the junction is reverse-biased, the barrier capacitance C_j dominates. For forward-biased conditions there is in addition a significant contribution to junction capacitance from the rearrangement of minority carrier density, the diffusion capacitance C_d. The barrier capacitance for a one-sided abrupt junction with the acceptor concentration N_A depends on the biasing voltage U as follows [2]

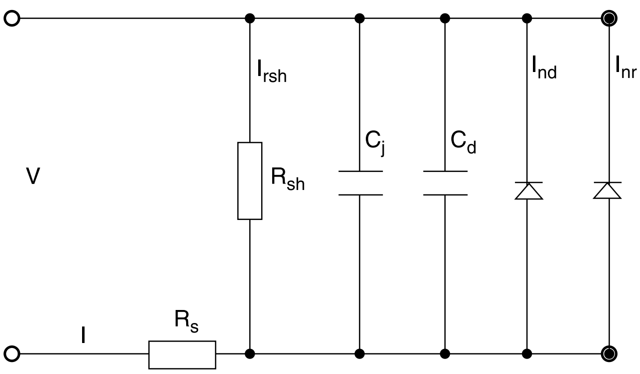

Fig. 2. Equivalent circuit of a solar cell after turning-off the light (I_{ph} = 0); I_{nr} is the recombination current component, I_{nd} is the diffusion current component, R_{sh} is the shunt resistance, R_s is the series resistance, I_{rsh} is the shunt resistance current, C_d is the diffusion capacitance, and C_j is the depletion layer (barrier) capacitance.

$$C_j = \frac{\sqrt{\frac{\varepsilon_0 \varepsilon q N_A}{2V_j}} S}{\left(1 - \frac{U}{V_j}\right)^{1/2}}, \tag{1}$$

where S is the diode area, $\varepsilon_o\varepsilon$ is the electrical permittivity of a semiconductor, q is the elementary charge, and V_j is the built-in potential. A diffusion capacitance can be expressed by the diode current I_D and the time constant τ_F [3]

$$C_d = \frac{q}{kT} \tau_F (I_D + I_S), \tag{2}$$

where I_S is the saturation current and τ_F is related to the minority carriers lifetime τ and the transit time across the diode τ_B as follows

$$\frac{1}{\tau_F} = \frac{1}{\tau} + \frac{1}{\tau_B}. \tag{3}$$

When the base thickness d is greater than the minority carriers diffusion length L_n, the value τ_B^{-1} can be omitted and C_d is then directly proportional to the minority carrier lifetime τ. A diffusion capacitance can be alternatively expressed as a function of bias voltage. The variation of both constituents of junction capacitance with the external voltage is shown in Fig. 3.

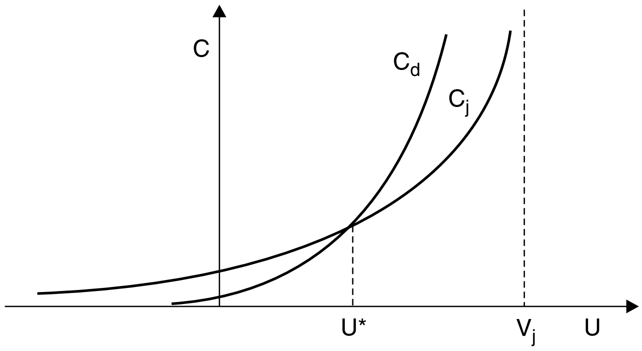

Fig. 3. Variations of C_j and C_d with the external voltage U.

The time constant connected with discharging of the barrier and diffusion capacitances can be written in a form

$$\tau_k = \frac{C_d}{G_F + G_{sh}} + \frac{C_j}{G_F + G_{sh}} = \tau_d + \tau_j, \tag{4}$$

where $G_{sh} = 1/R_{sh}$ is the shunt conductance and G_F is the diode conductance which increases quickly with a positive (forward) voltage

$$G_F = \frac{I_S\left[\exp\left(\frac{U}{nV_T}\right) + 1\right]}{nV_T}, \tag{5}$$

The parameter n is the diode ideality factor and $V_T = kT/q$ is the thermal voltage equal to 25.9 mV for T = 300 K.

3. Model calculations

Taking into account Eqs. (1), (2), and (5) the time constants of Eq. (4) were evaluated as a function of the bias voltage U for crystalline silicon solar cells. Some necessary parameters were taken from Ref. [4]. Typical results of calculations are shown in Figs. 4(a) and 4(b).

As it can be seen from the figures at low forward bias voltages, the barrier capacitance is responsible for the time response. With increasing voltage, the time constant

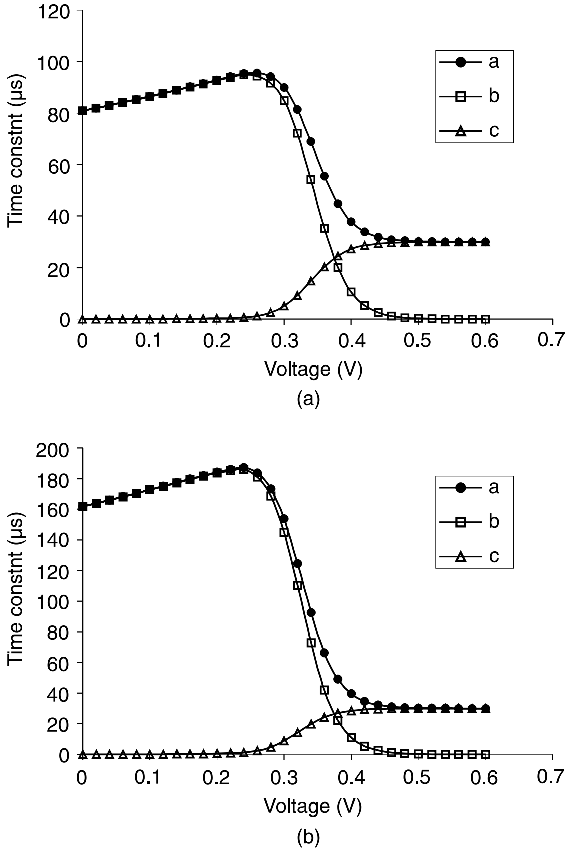

Fig. 4. Calculated time constant of junction capacitance discharge as a function of forward bias voltage for R_{sh} = 100 Ohm (a) and R_{sh} = 200 Ohm (b); designation of the curves: a – total time constant τ_k, b – influence of barrier capacitance τ_j, and c – influence of the diffusion capacitance τ_d.

$C_d/(G_F + G_{sh})$ also increases and for the voltages exceeding ca. 500 mV (for analysed c-Si solar cells) C_d/G_F dominates. This time constant contains information on the minority carriers lifetime τ [Eqs. (2) and (3)]. The dependencies similar to those from Fig. 4 were observed by Bitnar *et al.* [5].

The necessary forward bias voltage can be generated by using the constant illumination (bias light) from, e.g., tungsten halogen lamp. Such a configuration was used by the authors in photovoltage decay experiments, Fig. 5.

Many experiments performed with the above setup [6,7] indicate that junction capacitance time constants are typical not only of c-Si solar cells. Similar features were observed also for a-Si cells, Fig. 6.

This effect should be taken into account in the analysis of the open circuit voltage decay in solar cell structures. The decay of a short circuit current, as it can be expected, is not influenced by the junction capacitance (such a measurement possibility it is also seen in Fig. 6). The current density $j(t)$ that flows out of a solar cell base can be expressed in a form of series [8]

$$j(t) = \sum_{i=1}^{\infty} j_i(0)\exp\left(\frac{-t}{\tau_i}\right)s, \tag{6}$$

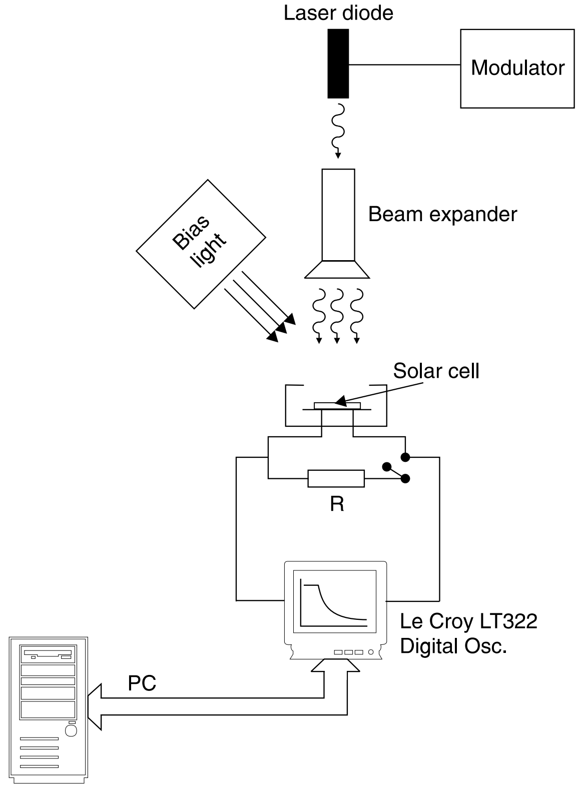

Fig. 5. Experimental setup for photodecay measurements.

where τ_i is the *i-th* mode decay constant. The detailed analysis of that decay for c-Si solar cells indicates [9], that purely exponential decay with the fundamental mode τ_1 is obtained

$$j(t) = j_1(0)\exp\left(\frac{-t}{\tau_1}\right), \tag{7}$$

for the times larger than the minority carrier lifetime. The plot of log $[j(t)]$ vs. t becomes linear, Fig. 7. The fundamental mode τ_1 is related to the minority carrier lifetime τ through

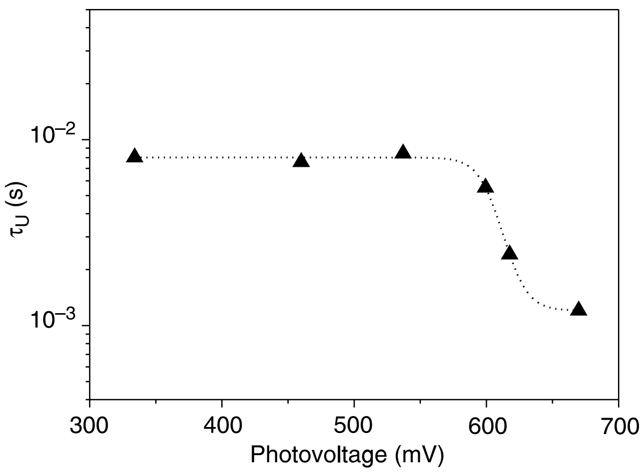

Fig. 6. Photovoltage decay time as a function of bias light (cell photovoltage) for a-Si:H solar cell.

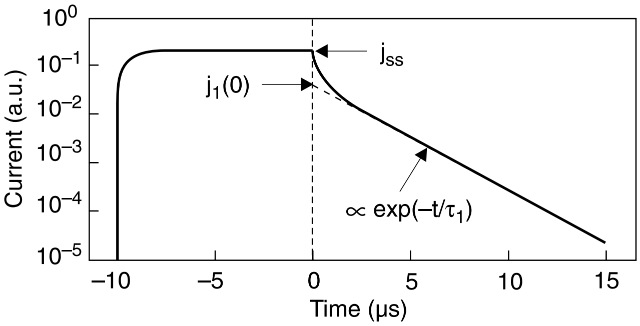

Fig. 7. Typical decay curve for a current density vs. time; j_{ss} is the steady state current density at $t = 0$, extrapolation of a straight line to $t = 0$ yields the intercept $j_1(0)$.

$$\tau/\tau_1 = 1 + w_1^2/w^2, \tag{8}$$

where w_1 fulfils the eigenvalue equation

$$w_1/s = -\tan(w_1). \tag{9}$$

In Eqs (8) and (9), $w = W/L$, $s = WS/D$ (W is the cell thickness, S is the recombination velocity, D is the diffusion constant, and L is the diffusion length).

4. Impedance characteristics

The calculations of the solar cell junction time constants required assumption of a few parameters. Some of them were taken from $I(U)$ solar cell characteristics published in Ref. 4. Numerical values of the junction capacitance $C(U)$ were determined independently from the impedance spectra. The measurements were made using HIOKI 3522-50 impedance analyser equipped with DC voltage bias unit. Negative and positive bias voltages were applied (in the dark) and some measurements were done with illumination.

Introducing the equivalent circuit models, it was possible to fit the impedance spectra and calculate the model parameters. The spectra for crystalline silicon solar cells required only modelling with a simple connection of the resistors and parallel RC circuit. The fitted values of the circuit parameters vary with the applied voltage as it was expected, Figs. 8 and 9.

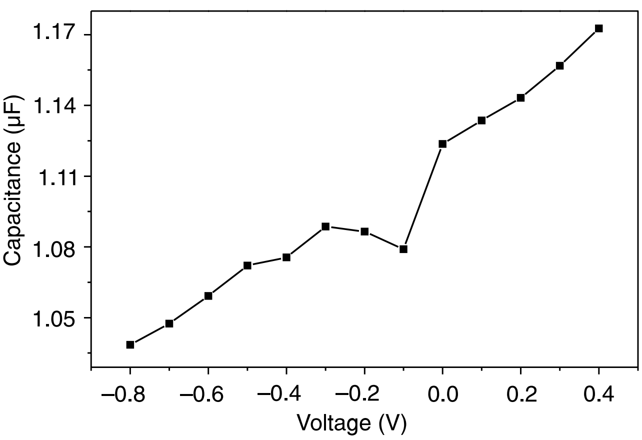

Fig. 8. Variation of junction capacitance of c-Si solar cell with the bias voltage.

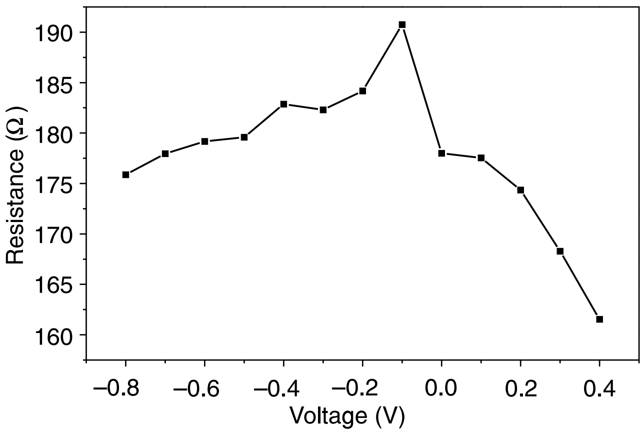

Fig. 9. Variation of junction resistance with the bias voltage for the parallel RC model of c-Si solar cell.

The numerical values of capacitances agree well with these calculated in the photodecay model where the parameters of asymmetrical silicon junction were used. The unexpected behaviour in the zero bias range is presumably influenced by an additional capacitance imposed by interface trapped and fixed charges connected with antireflection and passivating coatings deposited onto silicon wafer. This calls, however, for further investigations.

The concentration of acceptors in the base region was checked using the abrupt junction C-V model, Fig. 10. The determined value $N_A = 1.02\times10^{16}$ cm^{-3} agrees very well with the doping level for 1 Ω cm p-type c-Si wafers used in solar cells technology.

5. Conclusions

A large influence of the p$^+$-n solar cell junction capacitance and shunt resistance on the photvoltage decay time is observed. This influence can be minimised by application of the

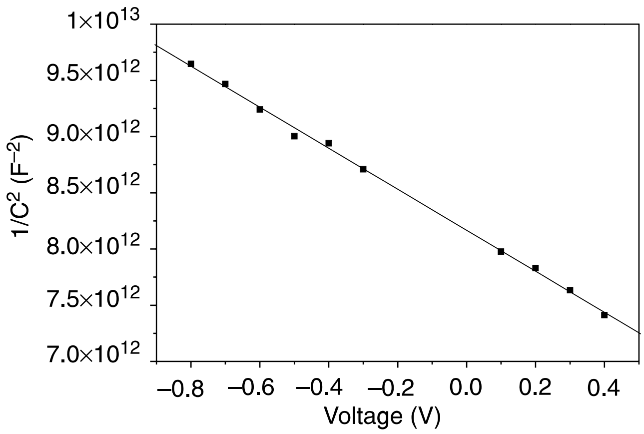

Fig. 10. Dependence of $1/C^2$ vs. bias voltage. From the linear fit one can calculate the concentration of carriers in the solar cell base (after Ref. 2).

bias light. The model calculations indicate that for c-Si solar cells the necessary constant illumination should generate the voltage of the order 500 mV. The decay of a short circuit current is not influenced by the junction time constant.

Impedance measurements of c-Si solar cell indicate that a simple parallel RC equivalent circuit can be used. The fitted values of junction capacitance vary with the applied voltage in agreement with the abrupt asymmetrical junction theory. Numerical values of determined capacitances agree well with these developed in the photodecay model.

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10–13
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E-mail: qd2004@nrc.gc.ca
URL: www.qd2004.com

13–15
SCELL-2004: International Conference on the Physics, Chemistry, and Engineering of Solar Cells, Badajoz, Spain
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16–19
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Topics cover materials, physics, and the technology of recording, as well as fundamental issues.
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17–21
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16–21
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24–28
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30–4 June
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URL: www.wessex.ac.uk/conferences/2004/hpsm04

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7–11
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