Debarghya Debnath E22ECEU0002
Experiment 5

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Implementing 4X1 Multiplexer

4x1 Multiplexer

Design code Structural :

C:/Users/student/Desktop/DD/multi/multi.srcs/sources_1/new/multi.vhd

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity multi is
port(
a1:in std_logic;
a2:in std_logic;
a3:in std_logic;
a4:in std_logic;
s1:in std_logic;
s2:in std_logic;
y:out std_logic);
end multi;

architecture Behavioral of multi is

begin
process(a1,a2,a3,a4,s1,s2) is
begin
y<=(a1 and (not s1)and (not s2) ) or(a2 and(not s1)and (s2)) or (a3 and(s1) and (not s2)) or (a4 and(s1)and(s2));
end process;

end Behavioral;

```

Design Code behavioural :

Project Summary | Schematic | multi.vhd * | testbenchmulti.vhd | Schematic (2) | Schematic (3)

C:/Users/student/Desktop/DD/multi/multi.srcs/sources_1/new/multi.vhd

```

entity multi is
port(
a1:in std_logic;
a2:in std_logic;
a3:in std_logic;
a4:in std_logic;
s1:in std_logic;
s2:in std_logic;
y:out std_logic);
end multi;

architecture Behavioral of multi is

begin
process(a1,a2,a3,a4,s1,s2) is
begin
if s1 = '0' and s2 ='0' then
y<=a1;
elsif s1='0'and s2='1' then
y<=a2;
elsif s1='1'and s2='0' then
y<=a3;
else
y<=a4;
end if;
end process;

```

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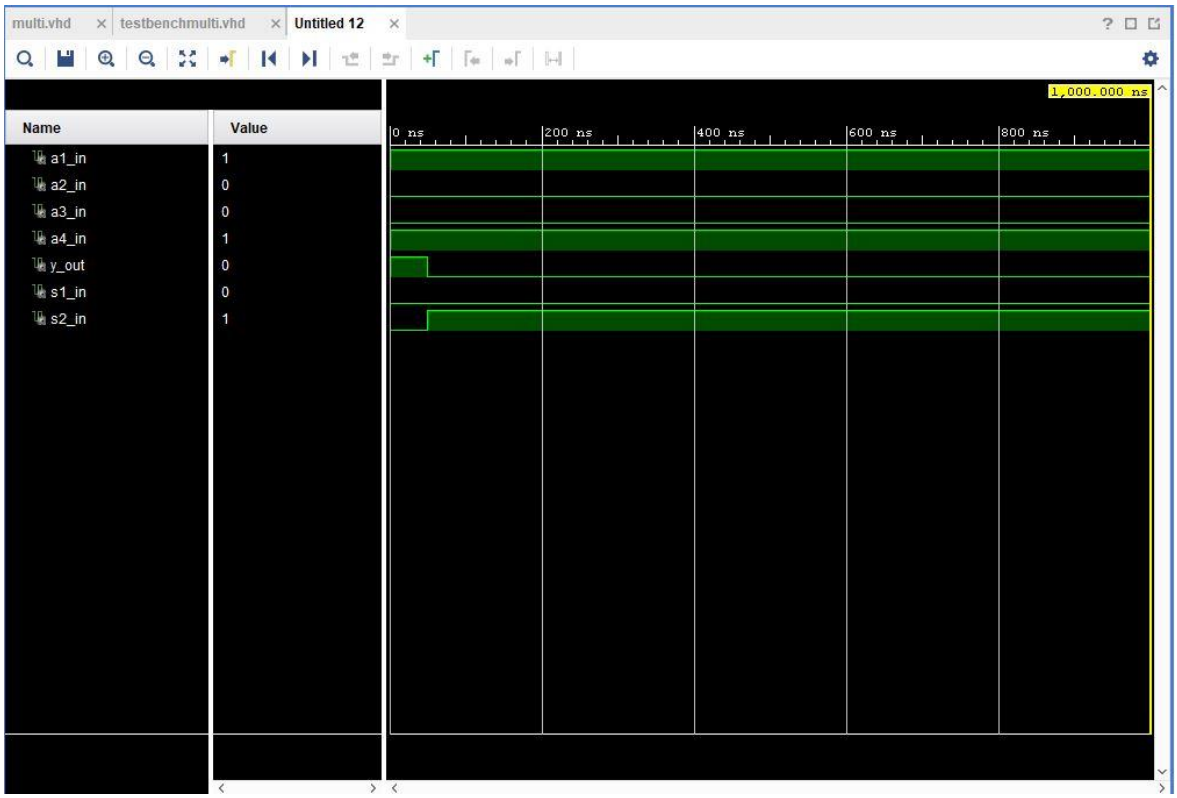
Test Bench:

C:/Users/student/Desktop/DD/multi/multi.srcs/sources_1/new/testbenchmulti.vhd

```
component multi is
port(
a1:in std_logic;
a2:in std_logic;
a3:in std_logic;
a4:in std_logic;
s1:in std_logic;
s2:in std_logic;
y:out std_logic);
end component;
signal a1_in,a2_in,a3_in,a4_in,y_out,s1_in,s2_in:std_logic;
begin
DUT: multi port map(a1_in,a2_in,a3_in,a4_in,s1_in,s2_in,y_out);
process
begin
a1_in<='1';
a2_in<='0';
a3_in<='0';
a4_in<='1';
s1_in<='0';
s2_in<='0';
wait for 50 ns;
a1_in<='1';
a2_in<='0';
a3_in<='0';
a4_in<='1';
s1_in<='0';
s2_in<='1';
wait for 50 ns;
wait;
```

Simulation:



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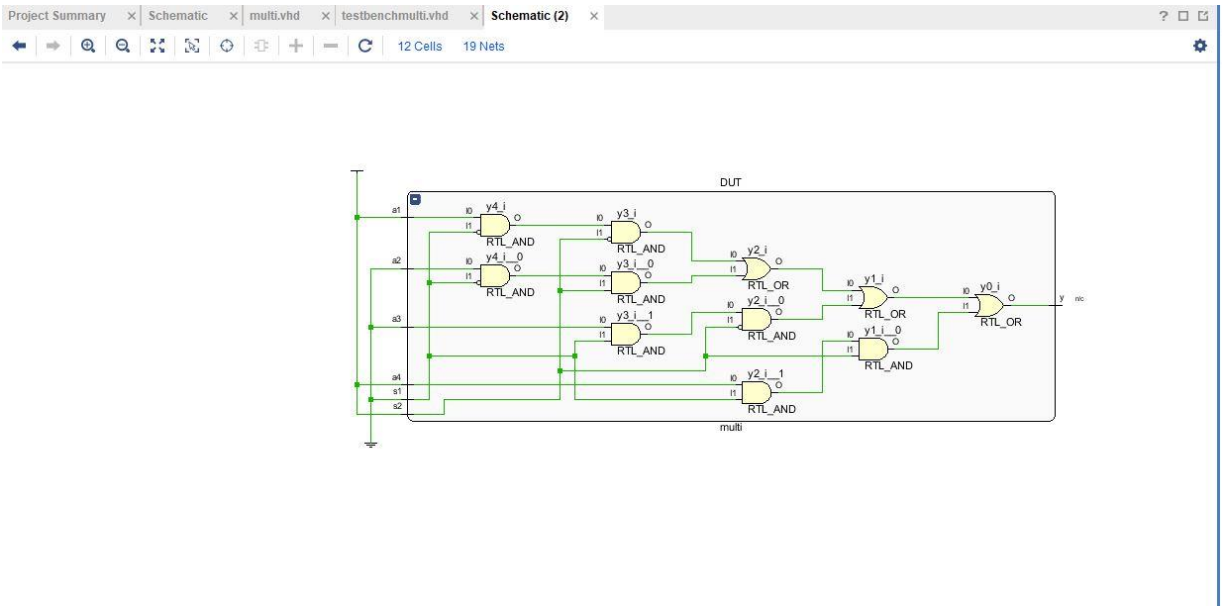
Schematic:



Result:- 4X1 Multiplexer has been implemented successfully and their test results are shown above.