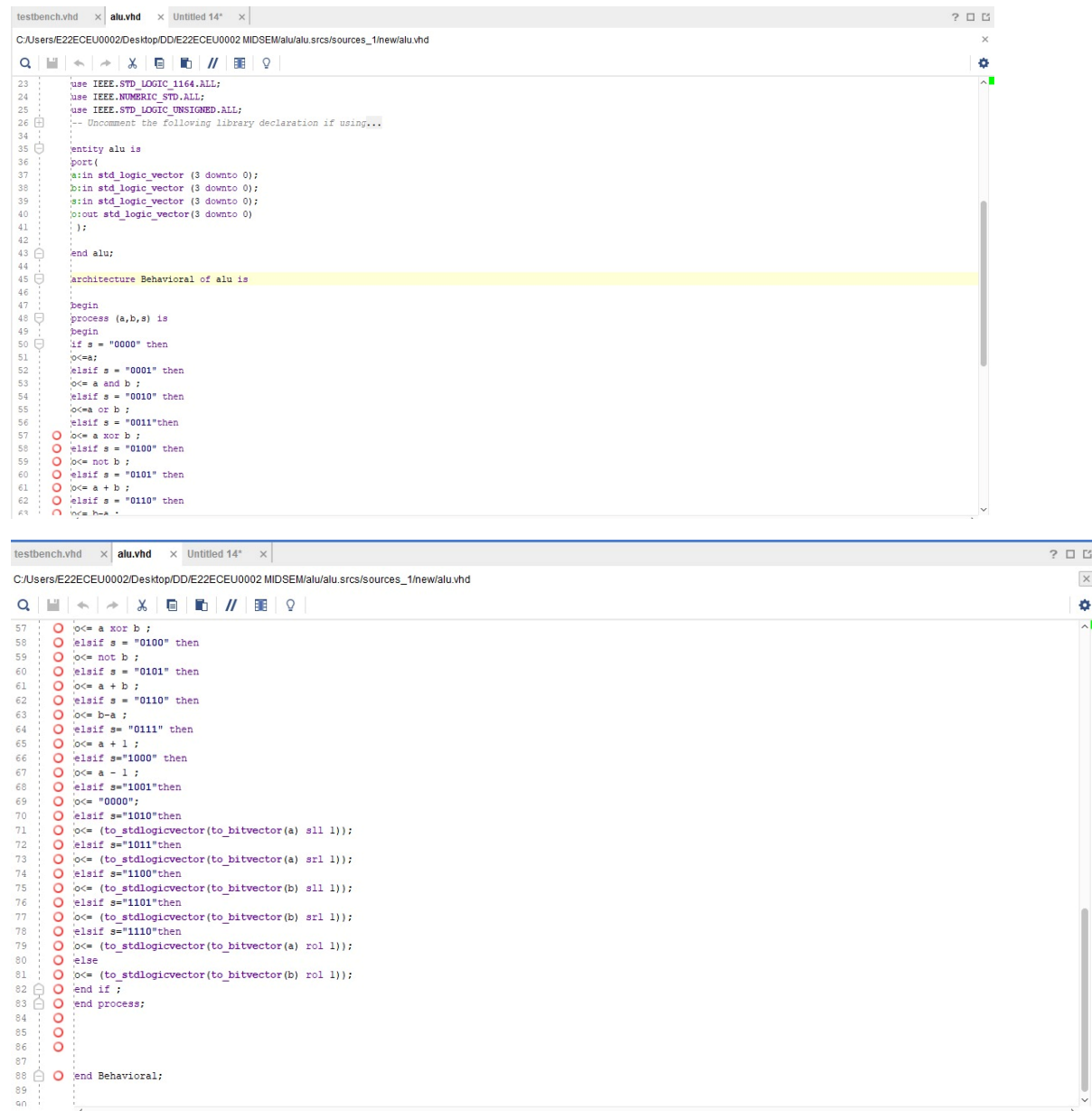


Experiment 11

Implementing 16-bit ALU

Design code:



```
23 use IEEE.STD_LOGIC_1164.ALL;
24 use IEEE.NUMERIC_STD.ALL;
25 use IEEE.STD_LOGIC_UNSIGNED.ALL;
26 -- Uncomment the following library declaration if using...
34
35 entity alu is
36 port(
37   a:in std_logic_vector (3 downto 0);
38   b:in std_logic_vector (3 downto 0);
39   s:in std_logic_vector (3 downto 0);
40   o:out std_logic_vector(3 downto 0)
41 );
42
43 end alu;
44
45 architecture Behavioral of alu is
46
47 begin
48   process (a,b,s) is
49   begin
50     if s = "0000" then
51       o<=a;
52     elsif s = "0001" then
53       o<= a and b ;
54     elsif s = "0010" then
55       o<=a or b ;
56     elsif s = "0011"then
57       o<= a xor b ;
58     elsif s = "0100" then
59       o<= not b ;
60     elsif s = "0101" then
61       o<= a + b ;
62     elsif s = "0110" then
63       o<= b-a ;
64     elsif s="0111" then
65       o<= a + 1 ;
66     elsif s="1000" then
67       o<= a - 1 ;
68     elsif s="1001"then
69       o<= "0000";
70     elsif s="1010"then
71       o<= (to_stdlogicvector(to_bitvector(a) sll 1));
72     elsif s="1011"then
73       o<= (to_stdlogicvector(to_bitvector(a) srl 1));
74     elsif s="1100"then
75       o<= (to_stdlogicvector(to_bitvector(b) sll 1));
76     elsif s="1101"then
77       o<= (to_stdlogicvector(to_bitvector(b) srl 1));
78     elsif s="1110"then
79       o<= (to_stdlogicvector(to_bitvector(a) rol 1));
80     else
81       o<= (to_stdlogicvector(to_bitvector(b) rol 1));
82     end if ;
83   end process;
84
85
86
87
88 end Behavioral;
```

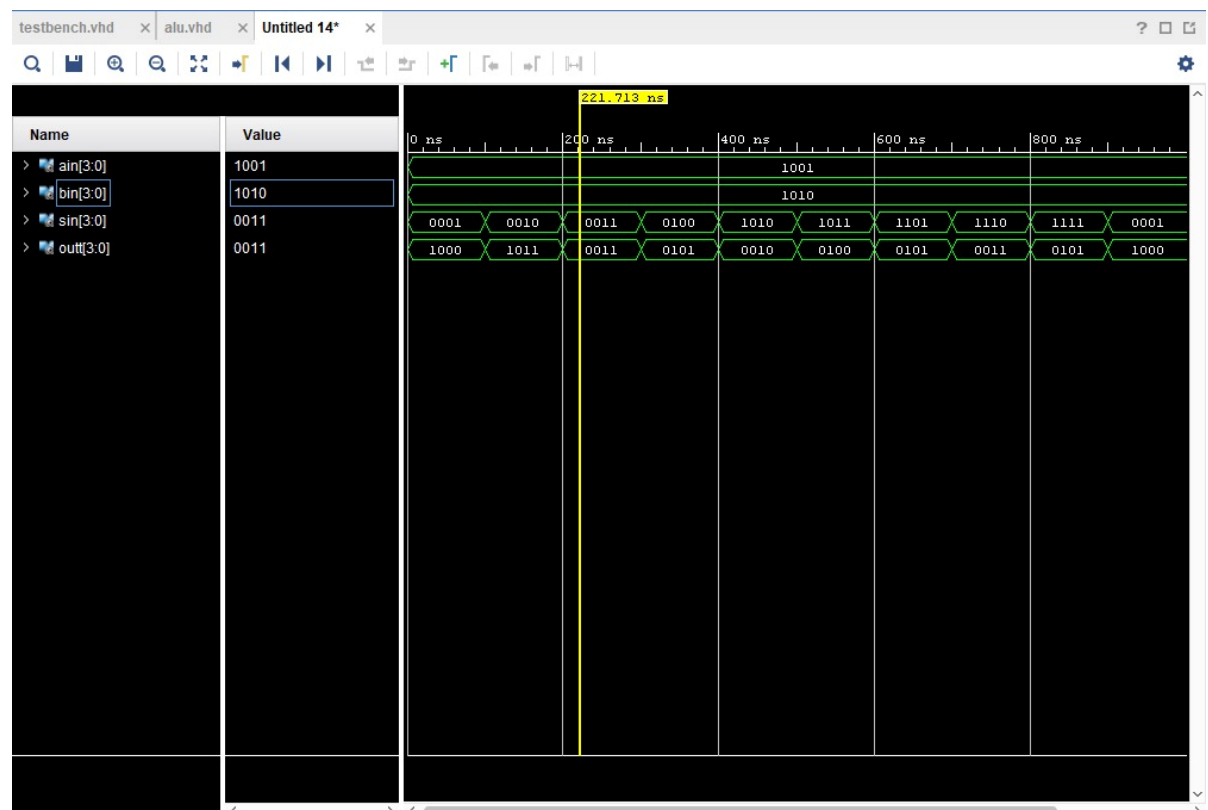
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Experiment 11

Testbench:

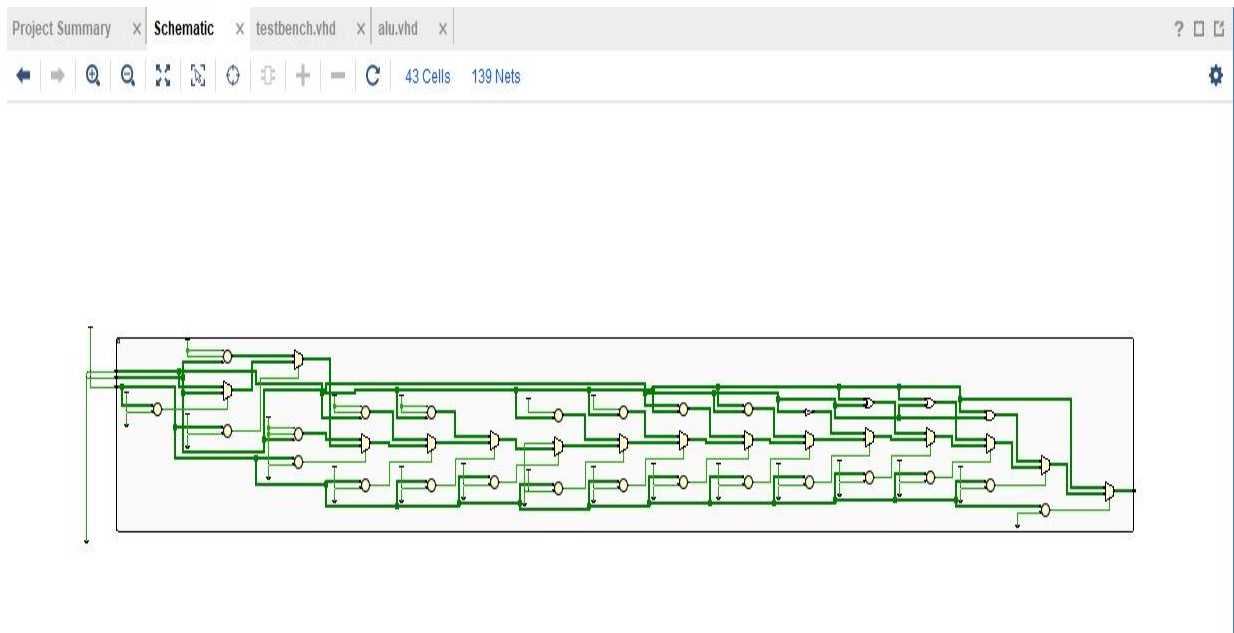
```
testbench.vhd x alu.vhd x Untitled 14* x
C:/Users/E22ECEU0002/Desktop/DD/E22ECEU0002 MIDSEM/alu/alu.srcs/sources_1/new/testbench.vhd

41 port(
42     a:in std_logic_vector (3 downto 0);
43     b:in std_logic_vector (3 downto 0);
44     s:in std_logic_vector (3 downto 0);
45     o:out std_logic_vector(3 downto 0)
46 );
47 end component ;
48 signal ain : std_logic_vector(3 downto 0) := "1001";
49 signal bin : std_logic_vector(3 downto 0) := "1010";
50 signal sin,outt :std_logic_vector(3 downto 0) ;
51 begin
52     OUT : alu port map (ain,bin,sin,outt) ;
53 process
54 begin
55
56     sin<="0001";
57     wait for 100ns;
58
59     sin<="0010";
60     wait for 100ns;
61
62     sin<="0011";
63     wait for 100ns;
64
65     sin<="0100";
66     wait for 100ns;
67
68     sin<="1010";
69     wait for 100ns;
70
71     sin<="1011";
72     wait for 100ns;
73
74     sin<="1101";
```

Simulation:



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Result:- 16 bit ALU has been implemented successfully, and their test results are shown above.