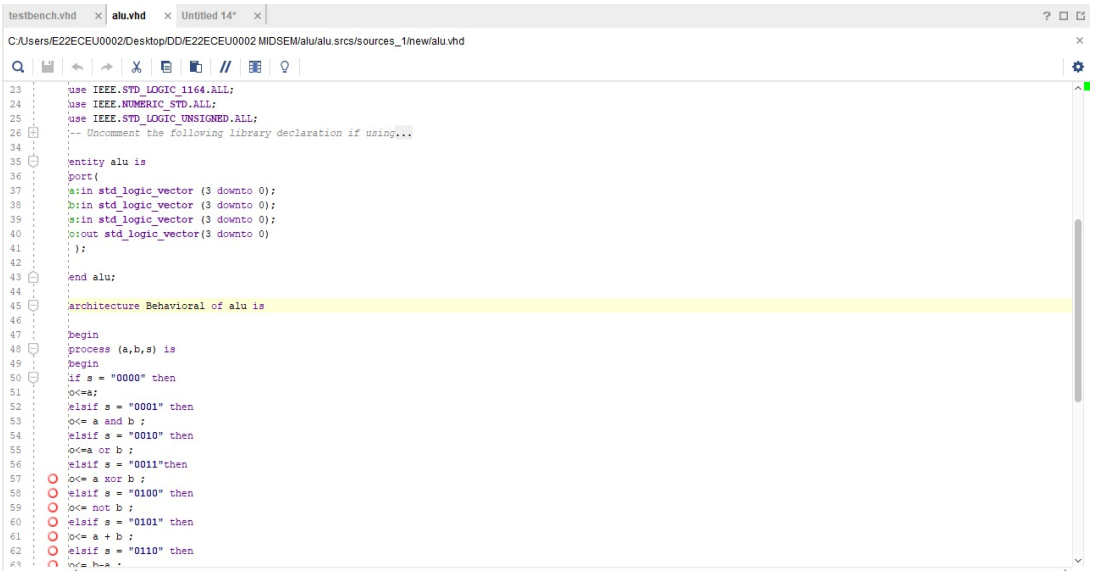
Experiment 11

Implementing 16-bit ALU

Design code:



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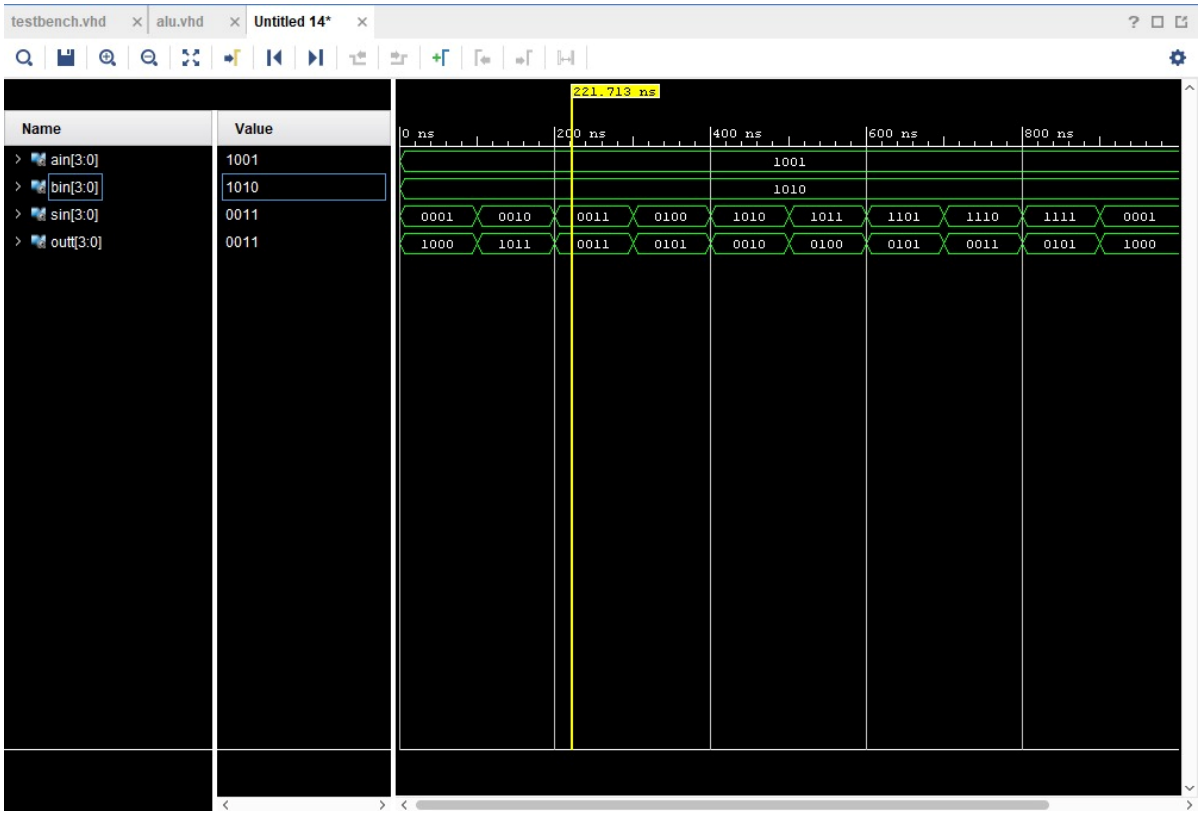
Testbench:

testbench.vhd | alu.vhd | Untitled 14*

C:/Users/E22ECEU0002/Desktop/DD/E22ECEU0002 MIDSEM/alu/alu.srcs/sources_1/new/testbench.vhd

```
41      port(
42      a:in std_logic_vector (3 downto 0);
43      b:in std_logic_vector (3 downto 0);
44      s:in std_logic_vector (3 downto 0);
45      o:out std_logic_vector(3 downto 0)
46       );
47       end component ;
48       signal ain : std_logic_vector(3 downto 0) :="1001";
49       signal bin : std_logic_vector(3 downto 0) :="1010";
50      signal sin,outt :std_logic_vector(3 downto 0) ;
51      begin
52      DUT : alu port map (ain,bin,sin,outt) ;
53      process
54      begin
55
56      sin<="0001";
57      wait for 100ns;
58
59      sin<="0010";
60      wait for 100ns;
61
62      sin<="0011";
63      wait for 100ns;
64
65      sin<="0100";
66      wait for 100ns;
67
68      sin<="1010";
69      wait for 100ns;
70
71      sin<="1011";
72      wait for 100ns;
73
74      sin<="1101";
```

Simulation:



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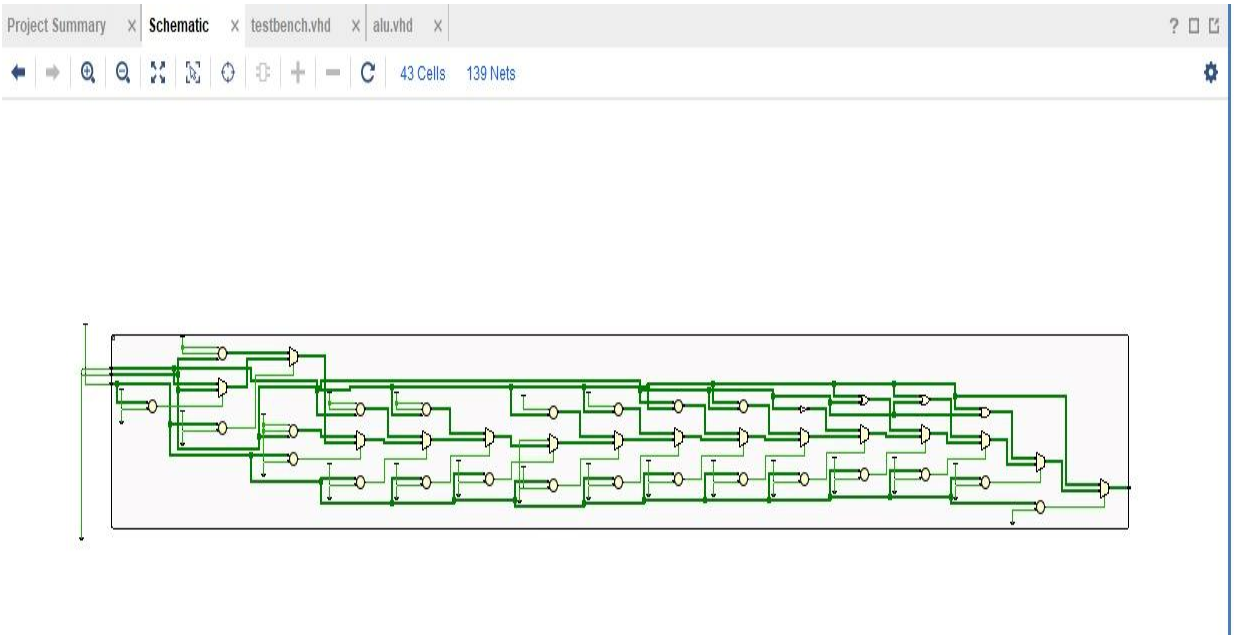

Result:- 16 bit ALU has been implemented successfully, and their test results are shown above.