Experiment 10

Implementing JK FLIP FLOP

Design code:

jkflip.vhd | testbench.vhd | Untitled 8

C:/Users/E22ECEU0002/Desktop/DD/E22ECEU0002 MIDSEM/jkflip/jkflip.srcs/sources_1/new/jkflip.vhd

```
17      -- Additional Comments:
18      --
19      ----------------------------------------------------------------------------------
20
21
22      library IEEE;
23      use IEEE.STD_LOGIC_1164.ALL;
24
25      -- Uncomment the following library declaration if using
26      -- arithmetic functions with Signed or Unsigned values
27      --use IEEE.NUMERIC_STD.ALL;
28
29      -- Uncomment the following library declaration if instantiating
30      -- any Xilinx leaf cells in this code.
31      --library UNISIM;
32      --use UNISIM.VComponents.all;
33
34      entity jkflip is
35      Port (
36      j: in std_logic;
37      k: in std_logic;
38      clk: in std_logic;
39      e: in std_logic;
40      q: inout std_logic
41       );
42      end jkflip;
43
44      architecture Behavioral of jkflip is
45      begin
46      process(j,k,clk,e)is
47      begin
48      if(e='0')then
49      q<='0';
50      elsif(rising_edge(clk))then
51       if (j='1' and k='1')then
52       q<=not q;
53       elsif(j='0' and k='0')or(j='0' and k='1')or(j='1' and k='0')then
54       q<=(j or (q and(not k)));
55       end if;
56      end if;
57      end process;
58      end Behavioral;
59
```

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testbench:

jkflip.vhd | testbench.vhd | Untitled 8

C:/Users/E22ECEU0002/Desktop/DD/E22ECEU0002 MIDSEM/jkflip/jkflip.srcs/sources_

```
42      k: in std_logic;
43      e:in std_logic;
44      clk:in std_logic;
45      q:inout std_logic);
46      end component;
47      signal jin,kin,qlout : std_logic;
48      signal clkin : std_logic :='0' ;
49      signal ein : std_logic :='1' ;
50      signal qout: std_logic :='1';
51      begin
52      DUT: jkflip port map (jin,kin,ein,clkin,qlout);
53      process begin
54      for i in 0 to 10 loop
55      clkin <= not clkin;
56      wait for 10ns;
57      clkin<= clkin;
58      wait for 10ns;
59      end loop;
60      end process;
61
62      process
63      begin
64
65      jin<='1';
66      kin<='0';
67      ein<='1';
68      wait for 30ns;
69      jin<='1';
70      kin<='0';
71      ein<='1';
72      wait for 30ns;
73      jin<='0';
74      kin<='0';
75      ein<='1';
76      wait for 30ns;
77      jin<='1';
78      kin<='1';
79      ein<='1';
80      wait;
81
82      end process;
```

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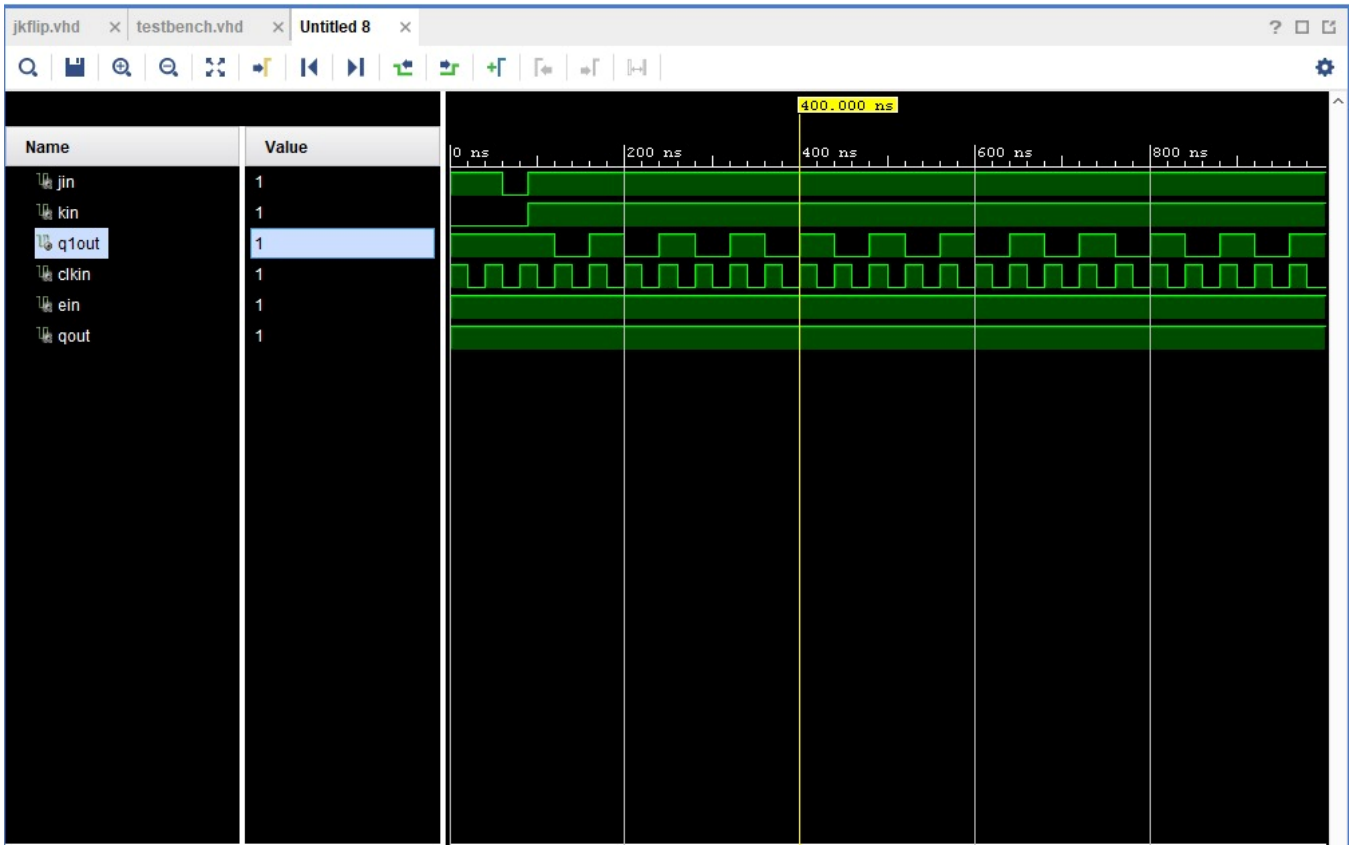
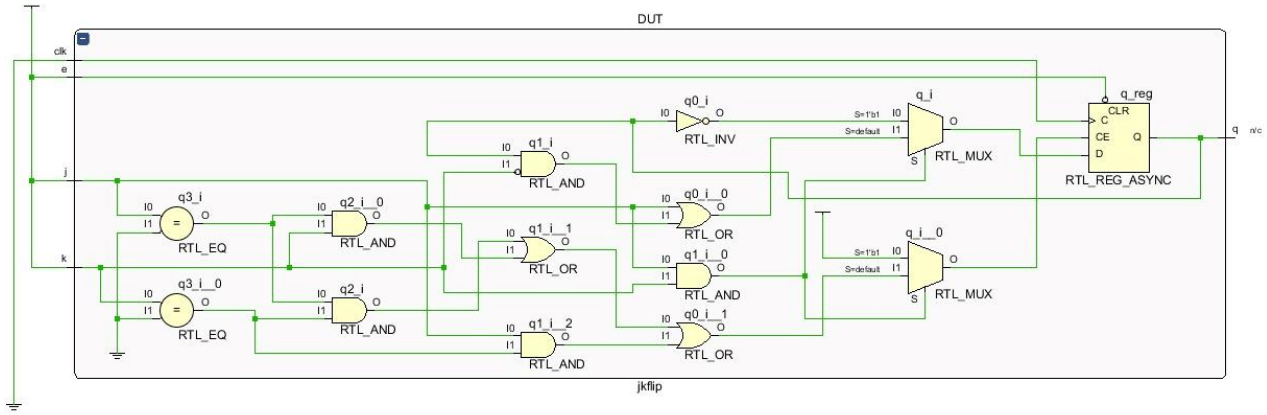
Simulation:





Result:- jk flip flop has been implemented successfully, and their test results are shown above.