Experiment 12

MOD 16 COUNTER

Design code:

Project Summary | contr.vhd | testbench.vhd *

C:/Users/debar/contr/contrr.srcs/sources_1/new/contr.vhd

```
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity contr is
    Port (
    clock:in std_logic;
    reset:in std_logic;
    count:out std_logic_vector(3 downto 0)
    );
end contr;

architecture behavior of contr is
    component jkff
        PORT( clock:in std_logic;
              reset: in std_logic;
              j:in std_logic;
              k:in std_logic;
              q:out std_logic
        );
    end component;

    signal temp: std_logic_vector(3 downto 0):= "0000";

begin
    d0: jkff port map (reset=>reset,clock =>clock, j =>'1',k =>'1',q => temp(0));
```

```
    signal temp: std_logic_vector(3 downto 0):= "0000";

begin
    d0: jkff port map (reset=>reset,clock =>clock, j =>'1',k =>'1',q => temp(0));
    d1: jkff port map (reset=>reset,clock =>temp(0), j =>'1',k =>'1',q => temp(1));
    d2: jkff port map (reset=>reset,clock =>temp(1), j => '1',k =>'1',q => temp(2));
    d3: jkff port map (reset=>reset,clock =>temp(2), j => '1',k =>'1',q => temp(3));
count <= temp;
end behavior;

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity jkff is
    Port ( j:in STD_LOGIC;
           k:in STD_LOGIC;
           clock:in STD_LOGIC;
           reset:in STD_LOGIC;
           q:out STD_LOGIC
    );
```

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```
41          k:in STD_LOGIC;
42          clock:in STD_LOGIC;
43          reset:in STD_LOGIC;
44          q:out STD_LOGIC
45      );
46  end jkff;
47
48  architecture behavior of jkff is
49      signal jk: std_logic_vector(1 downto 0):="00";
50      signal qs: std_logic:='0';
51
52  begin
53      jk<=j & k;
54
55      process (reset, clock)
56      begin
57          if reset='1' then
58              qs<='0';
59          elsif rising_edge(clock) then
60              case jk is
61                  when "00" =>qs<= qs;
62                  when "01" =>qs<= '0';
63                  when "10" =>qs<= '1';
64                  when others =>qs<= not qs;
65              end case;
66          end if;
67      end process;
68
69      q<=qs;
70  end behavior;
71
```

Testbench:-

C:/Users/debar/contrr/contrr.srcs/sources_1/new/testbench.vhd

```
7   end testbench;
8
9   architecture behavior OF testbench is
10    component contr
11    PORT(
12      clock:in std_logic;
13      reset:in std_logic;
14      count:out std_logic_vector(3 downto 0)
15      );
16    end component;
17
18    signal clock:std_logic := '0';
19    signal reset:std_logic := '0';
20    signal count:std_logic_vector(3 downto 0);
21  begin
22    uut: contr PORT MAP(
23      clock=>clock,
24      reset =>reset,
25      count => count
26    );
27
28    process
29    begin
30        wait for 5ns;
31        clock <= not clock;
32    end process;
33
34   process
35    begin
36        reset<='1';
37        wait for 70ns;
38        reset<= not reset;
```

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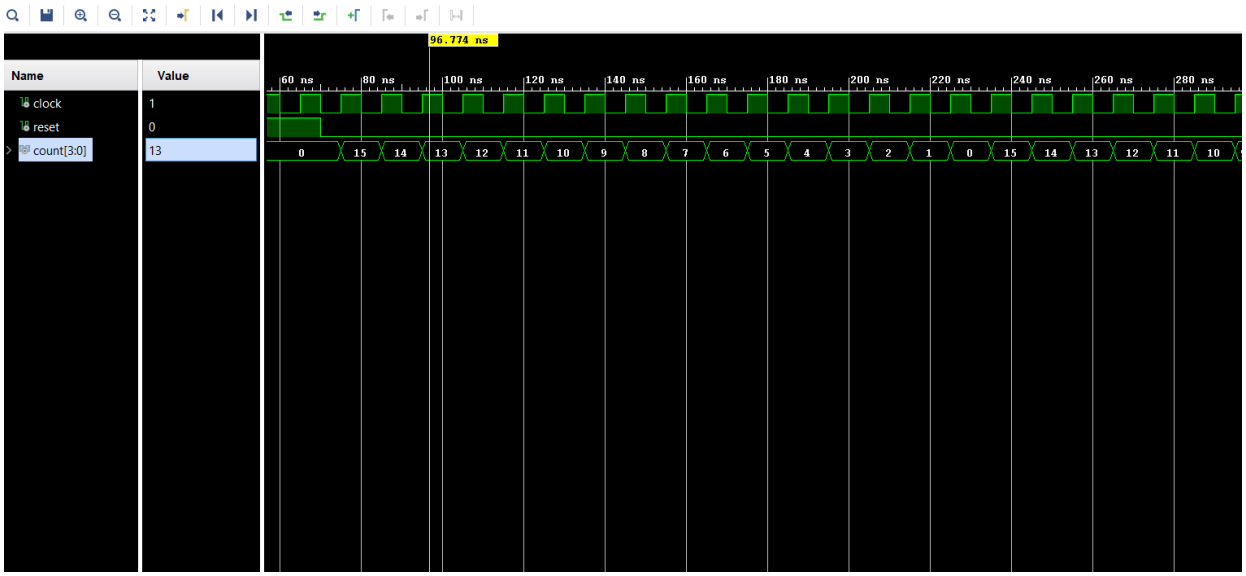
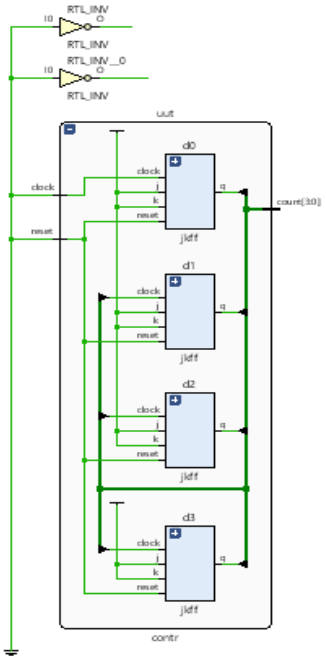
Simulation





result:- MOD 16 Counter has been implemented successfully and their test results are shown above.