Debarghya Debnath E22ECEU0002
Experiment 13

Experiment 13 (Assignment)

Implementing SISO shift register using flip flop

Design code:

Project Summary | Schematic | reg.vhd | testb.vhd

C:/Users/debar/reg/reg.srcs/sources_1/new/reg.vhd

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.all;
3  entity reg is
4  port(
5  d_in :in std_logic;
6  clk : in std_logic;
7  reset :in std_logic;
8  d_out :out std_logic_vector (3 downto 0));
9  end reg;
10 architecture behavior of reg is
11 component dflipflop is
12 port(
13 clk :in std_logic;
14 d_in :in std_logic;
15 reset :in std_logic;
16 d_out :out std_logic);
17 end component dflipflop;
18 signal s : std_logic_vector(3 downto 0);
19 begin
20 u0 :dflipflop port map (clk=>clk,d_in=>d_in,reset=>reset,d_out=>s(0));
21 u1 :dflipflop port map (clk=>clk,d_in=>s(0),reset=>reset,d_out=>s(1));
22 u2 :dflipflop port map (clk=>clk,d_in=>s(1),reset=>reset,d_out=>s(2));
23 u3 :dflipflop port map (clk=>clk,d_in=>s(2),reset=>reset,d_out=>s(3));
24 d_out <= s;
25 end behavior;
26 library IEEE;
27 use IEEE.STD_LOGIC_1164.all;
28 entity dflipflop is
29 port(
30 clk :in std_logic;
```

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```
18 signal s : std_logic_vector(3 downto 0);
19 begin
20 u0 :dflipflop port map (clk=>clk,d_in=>d_in,reset=>reset,d_out=>s(0));
21 u1 :dflipflop port map (clk=>clk,d_in=>s(0),reset=>reset,d_out=>s(1));
22 u2 :dflipflop port map (clk=>clk,d_in=>s(1),reset=>reset,d_out=>s(2));
23 u3 :dflipflop port map (clk=>clk,d_in=>s(2),reset=>reset,d_out=>s(3));
24 d_out <= s;
25 end behavior;
26 library IEEE;
27 use IEEE.STD_LOGIC_1164.all;
28 entity dflipflop is
29 port(
30 clk :in std_logic;
31 d_in :in std_logic;
32 reset :in std_logic;
33 d_out :out std_logic);
34 end dflipflop;
35 architecture behavior of dflipflop is
36 begin
37 process (d_in,clk,reset) is
38 begin
39 if (reset='1') then
40 d_out <= '0';
41 elsif (rising_edge (clk)) then
42 d_out <= d_in;
43 end if;
44 end process ;
45 end behavior;
46
```

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Testbench:

C:/Users/debar/reg/reg.srcs/sources_1/new/testb.vhd

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity testb is
5  end testb;
6
7  architecture behavior of testb is
8  component reg
9  port(
10 d_in :in std_logic;
11 clk :in  std_logic;
12 reset :in std_logic;
13 d_out :out std_logic_vector(3 downto 0)
14 );
15 end component;
16
17 signal d_in:std_logic := '0';
18 signal clk:std_logic := '0';
19 signal reset:std_logic := '0';
20 signal d_out:std_logic_vector(3 downto 0);
21 begin
22 uut:reg port map (
23 d_in => d_in,
24 clk => clk,
25 reset => reset,
26 d_out => d_out
27         );
28
29  process
30 begin
31 clk<='0';
32 wait for 50 ns ;
```

C:/Users/debar/reg/reg.srcs/sources_1/new/testb.vhd

```
20 signal d_out:std_logic_vector(3 downto 0);
21 begin
22 uut:reg port map (
23 d_in => d_in,
24 clk => clk,
25 reset => reset,
26 d_out => d_out
27          );
28
29  process
30 begin
31 clk<='0';
32 wait for 50 ns ;
33 clk<='1';
34 wait for 50 ns;
35 end process;
36
37   process
38    begin
39 reset<='1';
40 wait for 100 ns;
41 reset<='0';
42 wait for 50 ns;
43 d_in<='1';
44 wait for 50 ns;
45 d_in<='0';
46 wait;
47 end process;
48
49 end behavior;
50
```

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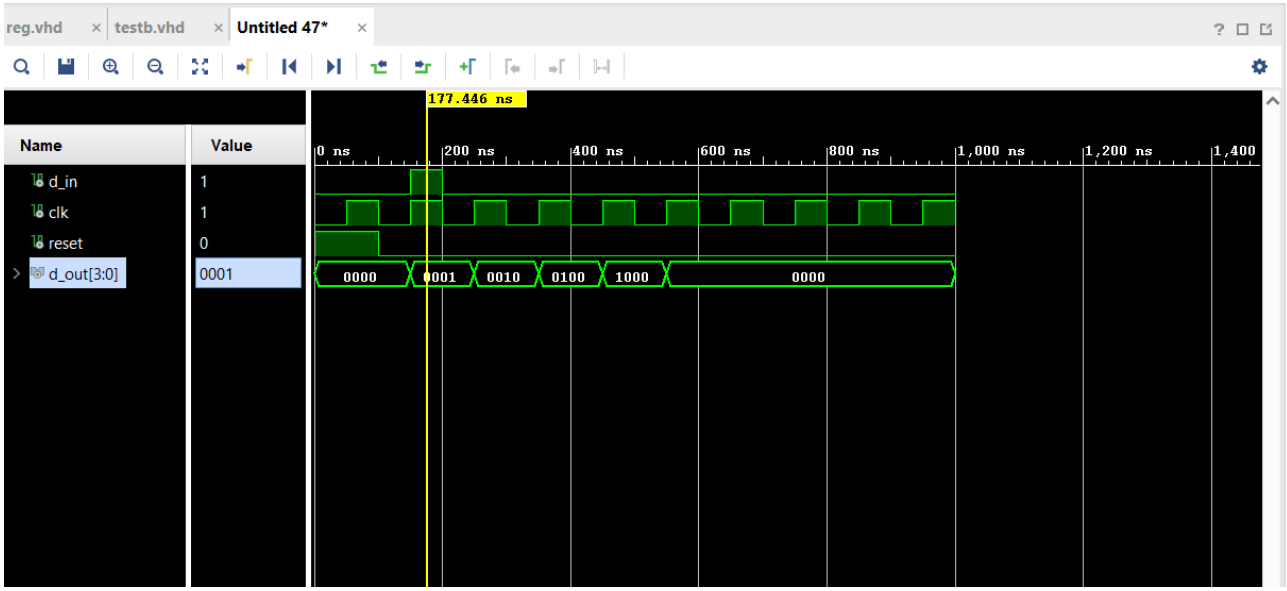
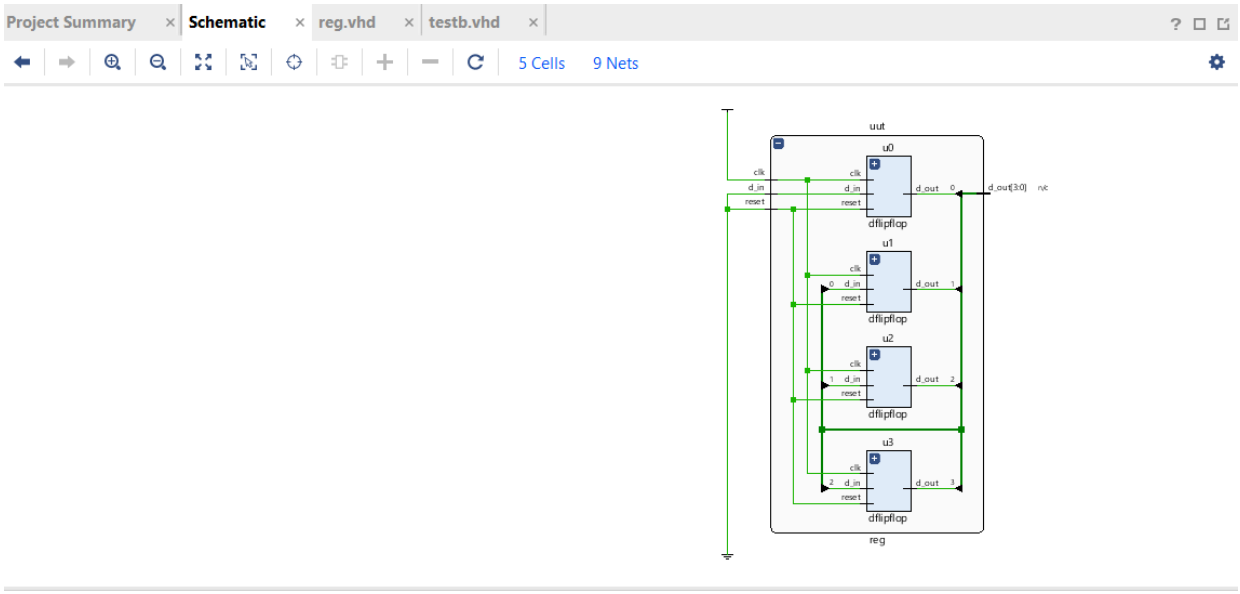
Simulation:



Schematic:



Result:- SISO Shift register has been implemented successfully using flip-flops, and their test results are shown above.