

# Experiment 6

## Implementing 8:1 Multiplexer and 2 to 4 Decoder

### Multiplexer

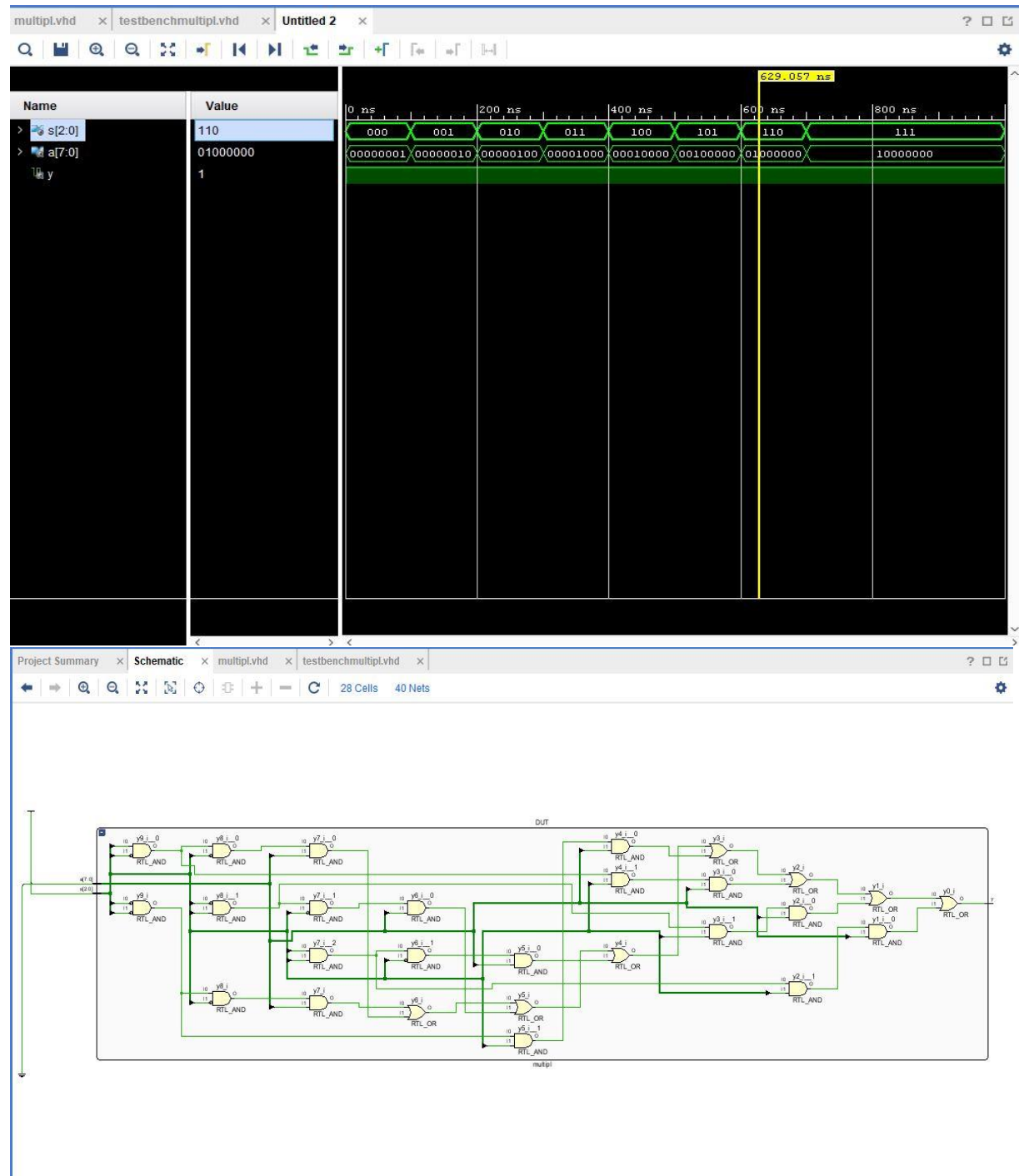
*Design code and testbench:*



```
multipl.vhd x testbenchmultipl.vhd x Untitled 2 x
C:/Users/student/Desktop/DD/multipl/multipl.srcs/sources_1/new/multipl.vhd

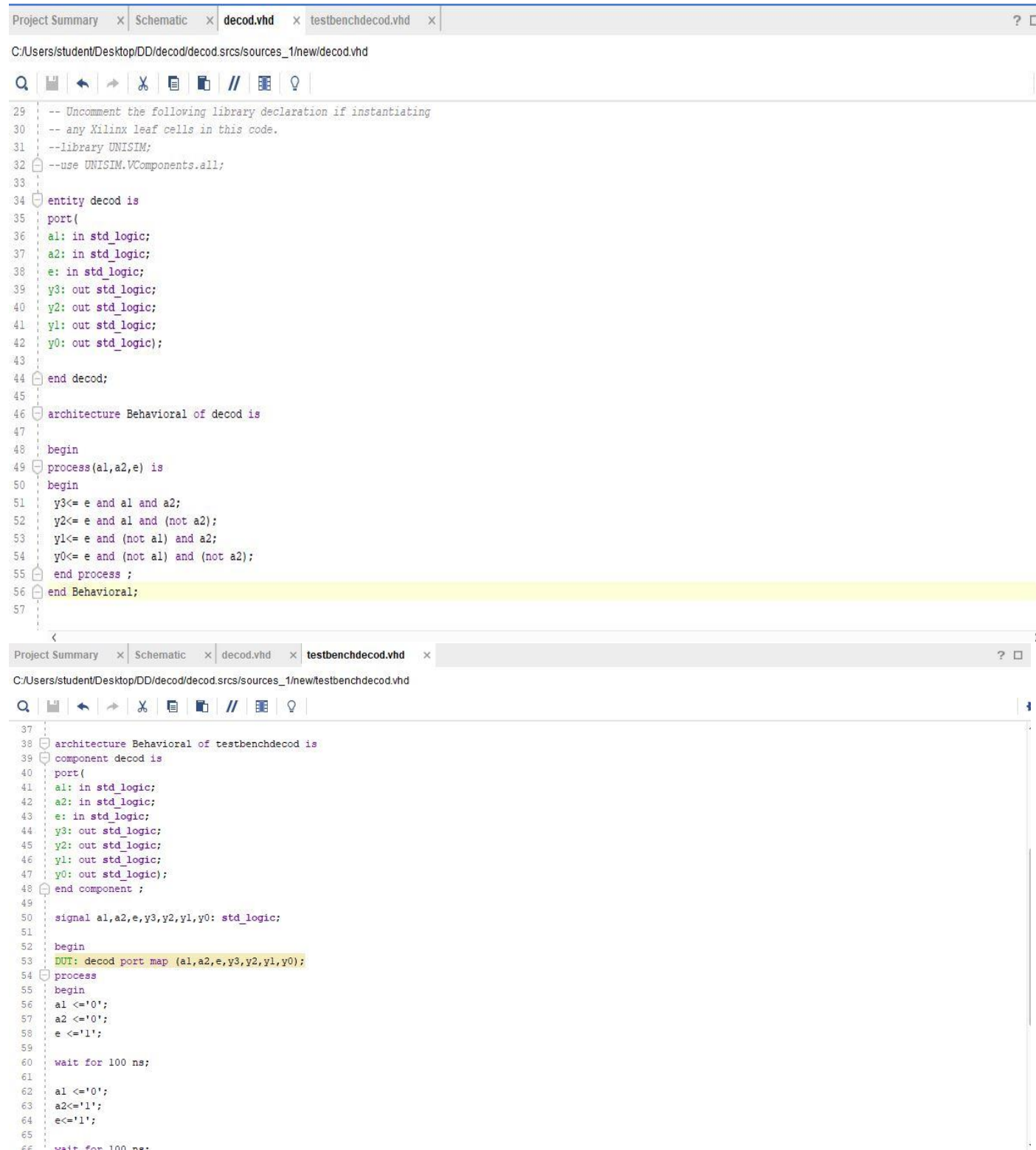
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22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 -- Uncomment the following library declaration if using...
26
27 entity multipl is
28 port(
29 s: in bit_vector(2 downto 0);
30 a: in bit_vector(7 downto 0);
31 y: out bit);
32 end multipl;
33
34 architecture Behavioral of multipl is
35 begin
36 process(s,a) is
37 begin
38 y<=((not s(0)) and (not s(1)) and (not s(2)) and a(0)) or (s(0) and (not s(1)) and (not s(2)) and a(1)) or ((not s(0)) and s(1)
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40 end process;
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42 end Behavioral;
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```

*Simulation:*



## Decoder

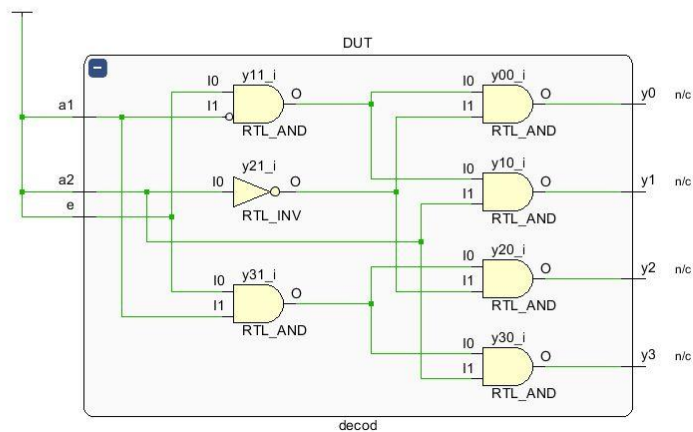
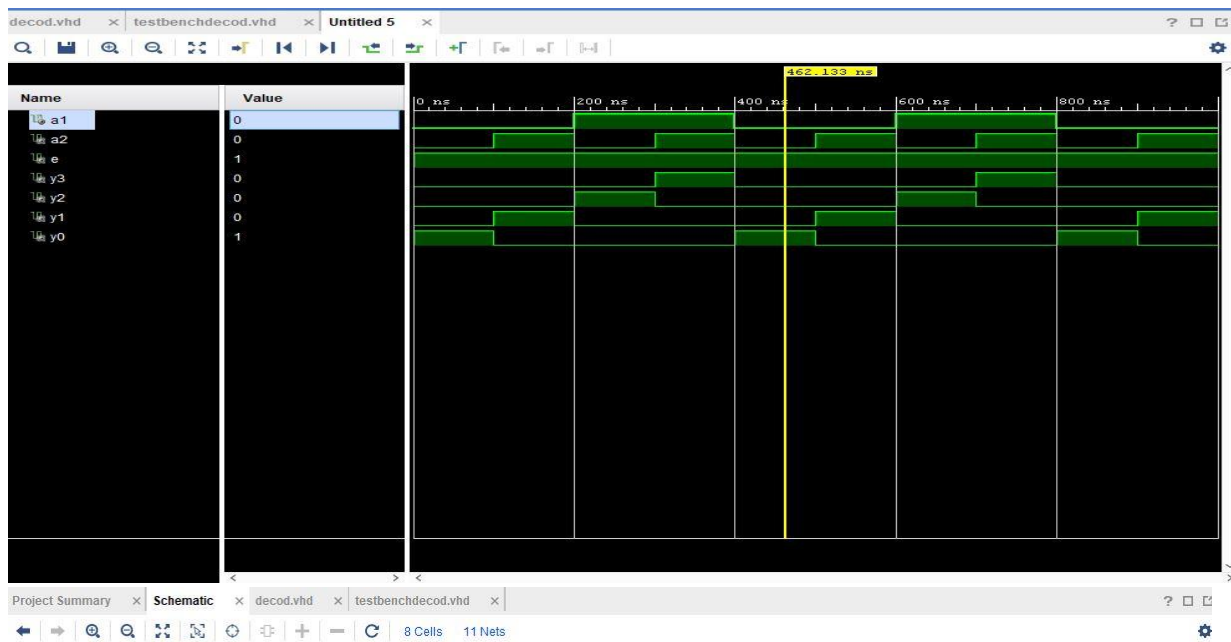
*Design code and testbench:*



The image shows two Verilog files in a code editor. The top file, `decod.vhd`, defines a 3-to-8 decoder entity. The bottom file, `testbenchdecod.vhd`, is a testbench for the decoder.

```
Project Summary x Schematic x decod.vhd x testbenchdecod.vhd x ? □  
C:/Users/student/Desktop/DD/decod/decod.srscs/sources_1/new/decod.vhd  
29 -- Uncomment the following library declaration if instantiating  
30 -- any Xilinx leaf cells in this code.  
31 --library UNISIM;  
32 --use UNISIM.VComponents.all;  
33  
34 entity decod is  
35 port(  
36   a1: in std_logic;  
37   a2: in std_logic;  
38   e: in std_logic;  
39   y3: out std_logic;  
40   y2: out std_logic;  
41   y1: out std_logic;  
42   y0: out std_logic);  
43  
44 end decod;  
45  
46 architecture Behavioral of decod is  
47  
48   begin  
49   process(a1,a2,e) is  
50     begin  
51       y3<= e and a1 and a2;  
52       y2<= e and a1 and (not a2);  
53       y1<= e and (not a1) and a2;  
54       y0<= e and (not a1) and (not a2);  
55     end process ;  
56   end Behavioral;  
57  
Project Summary x Schematic x decod.vhd x testbenchdecod.vhd x ? □  
C:/Users/student/Desktop/DD/decod/decod.srscs/sources_1/new/testbenchdecod.vhd  
37  
38 architecture Behavioral of testbenchdecod is  
39 component decod is  
40 port(  
41   a1: in std_logic;  
42   a2: in std_logic;  
43   e: in std_logic;  
44   y3: out std_logic;  
45   y2: out std_logic;  
46   y1: out std_logic;  
47   y0: out std_logic);  
48 end component ;  
49  
50 signal a1,a2,e,y3,y2,y1,y0: std_logic;  
51  
52 begin  
53   DUT: decod port map (a1,a2,e,y3,y2,y1,y0);  
54 process  
55 begin  
56   a1 <='0';  
57   a2 <='0';  
58   e <='1';  
59  
60   wait for 100 ns;  
61  
62   a1 <='0';  
63   a2<='1';  
64   e<='1';  
65  
66   wait for 100 ns;
```

Simulation:



**Result:-** 8:1 Multiplexer and 2 to 4 Decoder has been implemented successfully and their test results are shown above.