Debarghya Debnath E22ECEU0002
Experiment 9

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Implementing D-Flip flop

Design code:

dflip.vhd | testbench.vhd | Untitled 15

C:/Users/E22ECEU0002/Desktop/E22ECEU0002 MIDSEM/sequetial/sequetial.srcs/sources_1/new/dflip.vhd

```
1  ----------------------------------------------------------------------------...
20
21
22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 -- Uncomment the following library declaration if using...
33
34 entity dflip is
35 port(
36 d:in std_logic;
37 e:in std_logic;
38 clk:in std_logic;
39 ql:out std_logic;
40 q:inout std_logic);
41 end dflip;
42
43 architecture Behavioral of dflip is
44
45 begin
46 process(d,e,clk,q) is
47 begin
48 if e='0' then q<='0';
49 elsif rising_edge(clk) then
50 q<=d;
51 ql<= not q;
52
53 end if;
54 end process;
55 end Behavioral;
56
57
58
59
```

Testbench:

dflip.vhd | testbench.vhd | Untitled 15

C:/Users/E22ECEU0002/Desktop/E22ECEU0002 MIDSEM/sequetial/sequetial.srcs/sources_1/new/testbench.vhd

```
40 port(
41 d:in std_logic;
42 e:in std_logic;
43 clk:in std_logic;
44 ql:out std_logic;
45 q:inout std_logic);
46 end component;
47 signal din,qlout,qout : std_logic;
48 signal clkin : std_logic :='0' ;
49 signal ein : std_logic :='1' ;
50 begin
51 DUT: dflip port map (din,ein,clkin,qlout,qout);
52 process begin
53 for i in 0 to 10 loop
54 clkin <= not clkin;
55 wait for 10ns;
56 clkin<= clkin;
57 wait for 10ns;
58 end loop;
59 end process;
60
61 process
62 begin
63
64 din<='0';
65 ein<='1';
66 wait for 30ns;
67 din<='1';
68 ein<='1';
69 wait;
70
71
72 end process;
73
```

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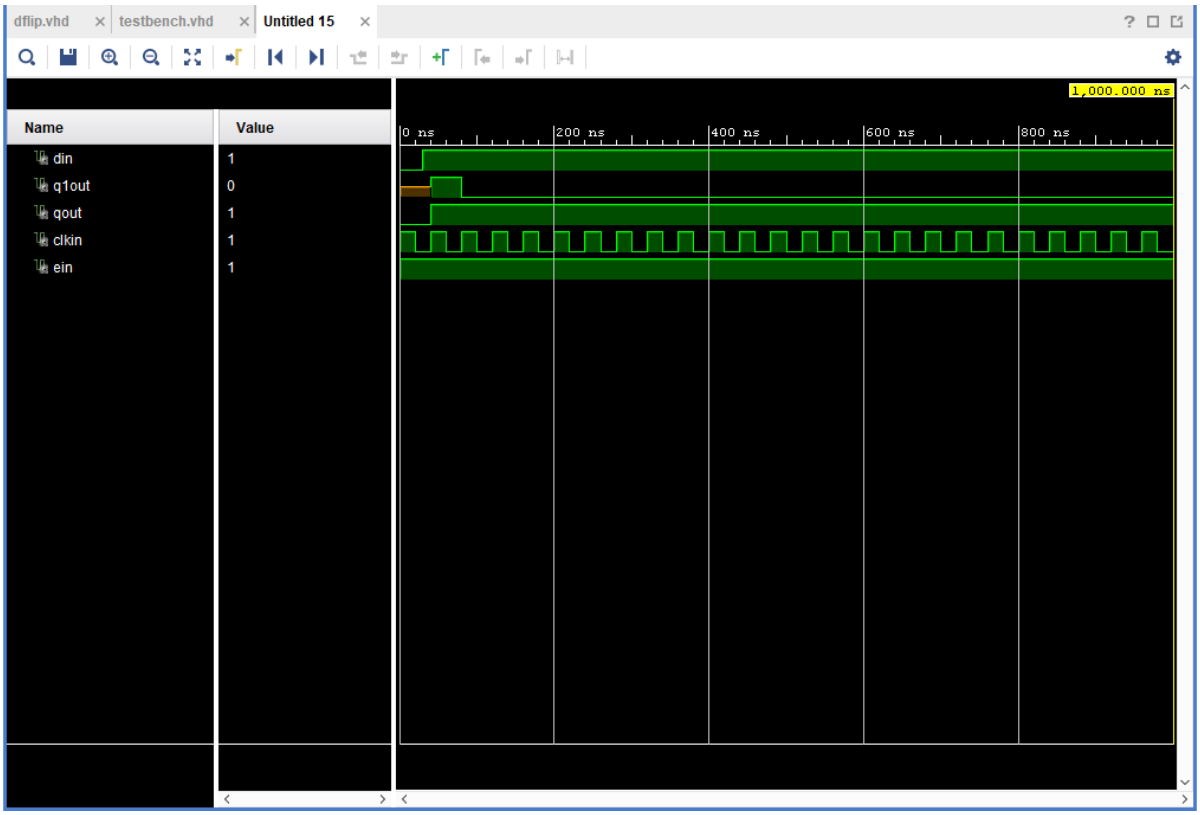
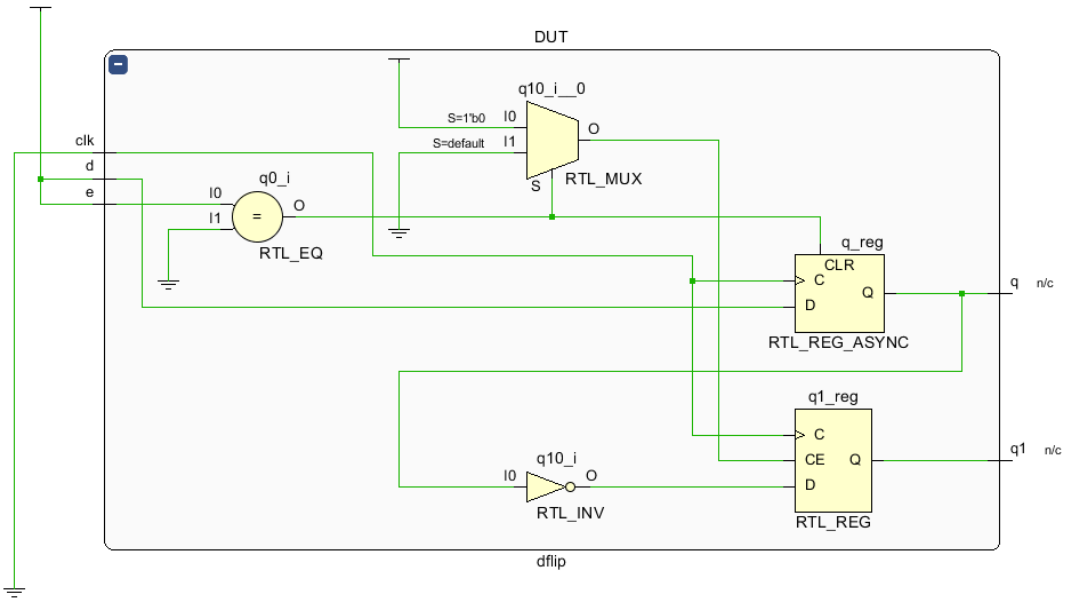
Simulation:





Result:- D-flip flop has been implemented successfully, and their test results are shown above.