Experiment 6

Implementing 8:1 Multiplexer and 2 to 4 Decoder

Multiplexer

Design code and testbench:

multipl.vhd | testbenchmultipl.vhd | Untitled 2

C:/Users/student/Desktop/DD/multipl/multipl.srcs/sources_1/new/multipl.vhd

```
1  ----------------------------------------------------------------------------...
20
21
22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 -- Uncomment the following library declaration if using...
33
34 entity multipl is
35 port(
36 s: in bit_vector(2 downto 0);
37 a: in bit_vector(7 downto 0);
38 y: out bit);
39
40 end multipl;
41
42 architecture Behavioral of multipl is
43
44 begin
45 process(s,a) is
46 begin
47 y<=((not s(0)) and (not s(1)) and (not s(2)) and a(0)) or (s(0) and (not s(1)) and (not s(2)) and a(1)) or ((not s(0)) and  s(1)
48
49 end process;
50
51
52 end Behavioral;
53
54
55
56
57
58
```

```
41 a: in bit_vector(7 downto 0);
42 y: out bit);
43 end component;
44 signal s : bit_vector (2 downto 0);
45 signal a : bit_vector (7 downto 0);
46 signal y : bit;
47
48 begin
49 DUT: multipl port map (s,a,y);
50 process
51 begin
52  s <= "000";
53    a <= "00000001";
54    wait for 100 ns;
55
56    s <= "001";
57    a <= "00000010";
58    wait for 100 ns;
59
60    s <= "010";
61    a <= "00000100";
62    wait for 100 ns;
63
64
65    s <= "011";
66    a <= "00001000";
67    wait for 100 ns;
68
69
70    s <= "100";
71    a <= "00010000";
72    wait for 100 ns;
73
74
```

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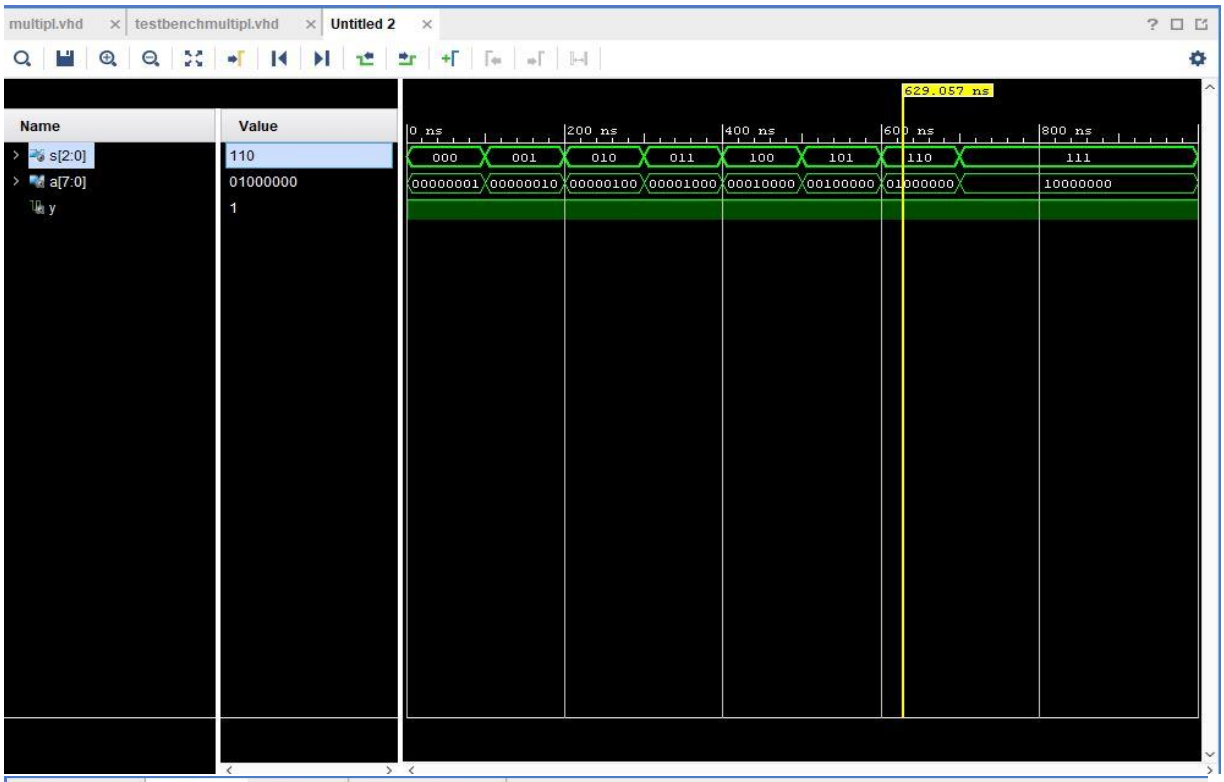
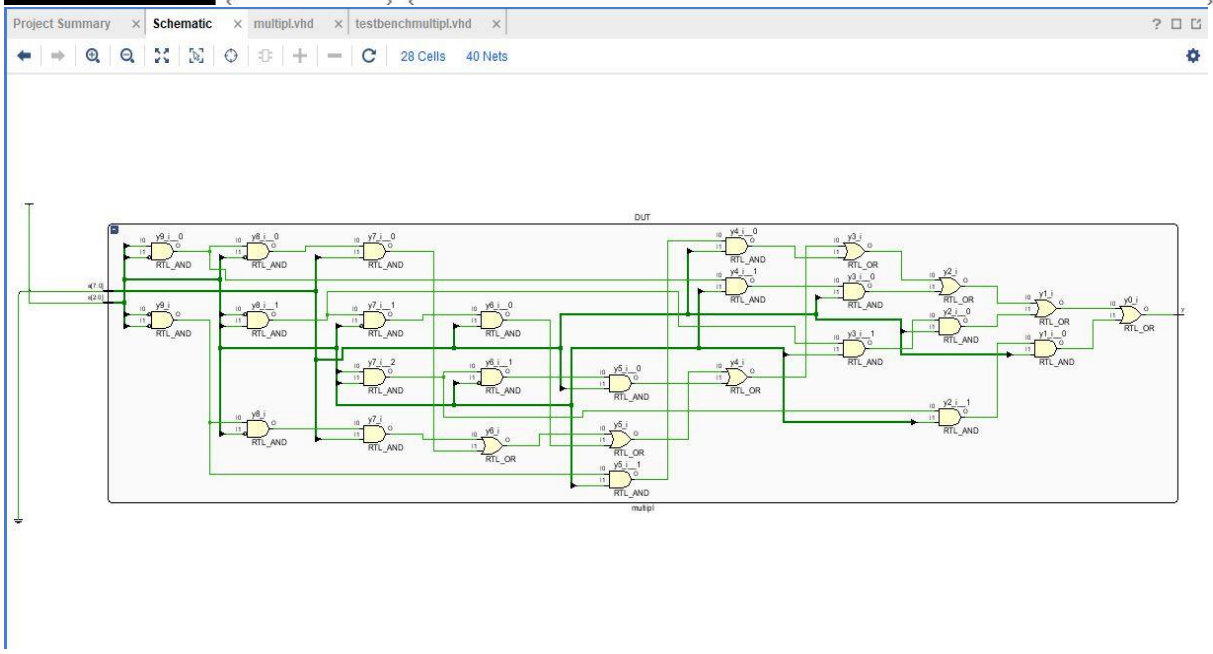
Simulation:





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Decoder

Design code and testbench:

Project Summary | Schematic | decod.vhd | testbenchdecod.vhd

C:/Users/student/Desktop/DD/decod/decod.srcs/sources_1/new/decod.vhd

```
-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity decod is
port(
a1: in std_logic;
a2: in std_logic;
e: in std_logic;
y3: out std_logic;
y2: out std_logic;
y1: out std_logic;
y0: out std_logic);

end decod;

architecture Behavioral of decod is

begin
process(a1,a2,e) is
begin
 y3<= e and a1 and a2;
 y2<= e and a1 and (not a2);
 y1<= e and (not a1) and a2;
 y0<= e and (not a1) and (not a2);
 end process ;
end Behavioral;
```

Project Summary | Schematic | decod.vhd | testbenchdecod.vhd

C:/Users/student/Desktop/DD/decod/decod.srcs/sources_1/new/testbenchdecod.vhd

```

architecture Behavioral of testbenchdecod is
component decod is
port(
a1: in std_logic;
a2: in std_logic;
e: in std_logic;
y3: out std_logic;
y2: out std_logic;
y1: out std_logic;
y0: out std_logic);
end component ;

signal a1,a2,e,y3,y2,y1,y0: std_logic;

begin
DUT: decod port map (a1,a2,e,y3,y2,y1,y0);
process
begin
a1 <='0';
a2 <='0';
e <='1';

wait for 100 ns;

a1 <='0';
a2<='1';
e<='1';

wait for 100 ns;
```

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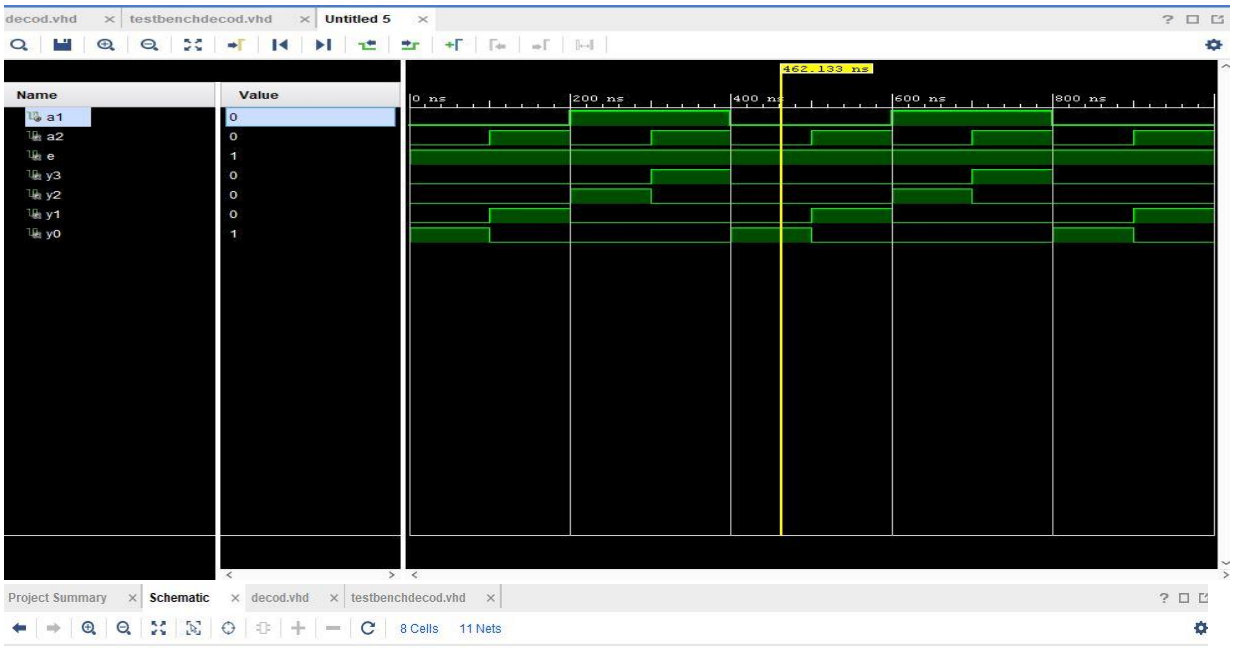
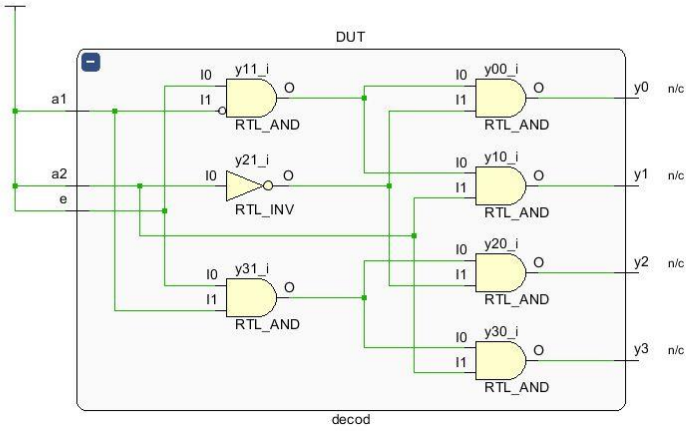
Experiment 6

Simulation:





Result:- 8:1 Multiplexer and 2 to 4 Decoder has been implemented successfully and their test results are shown above.