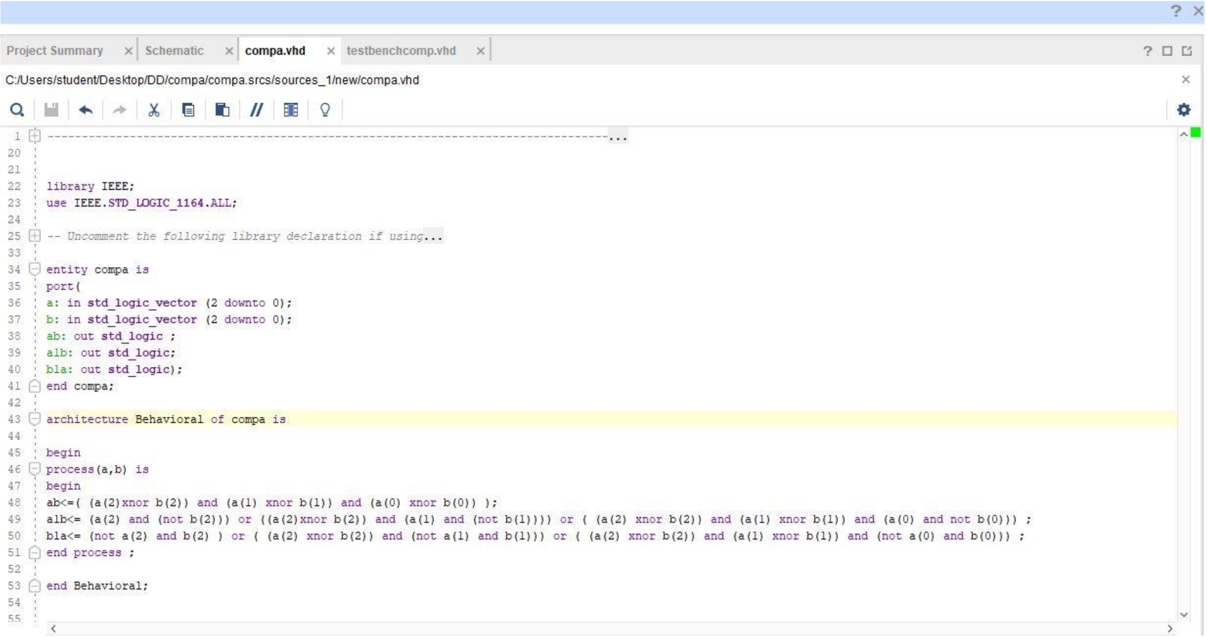
Experiment 7

Implementing 3-bit comparator

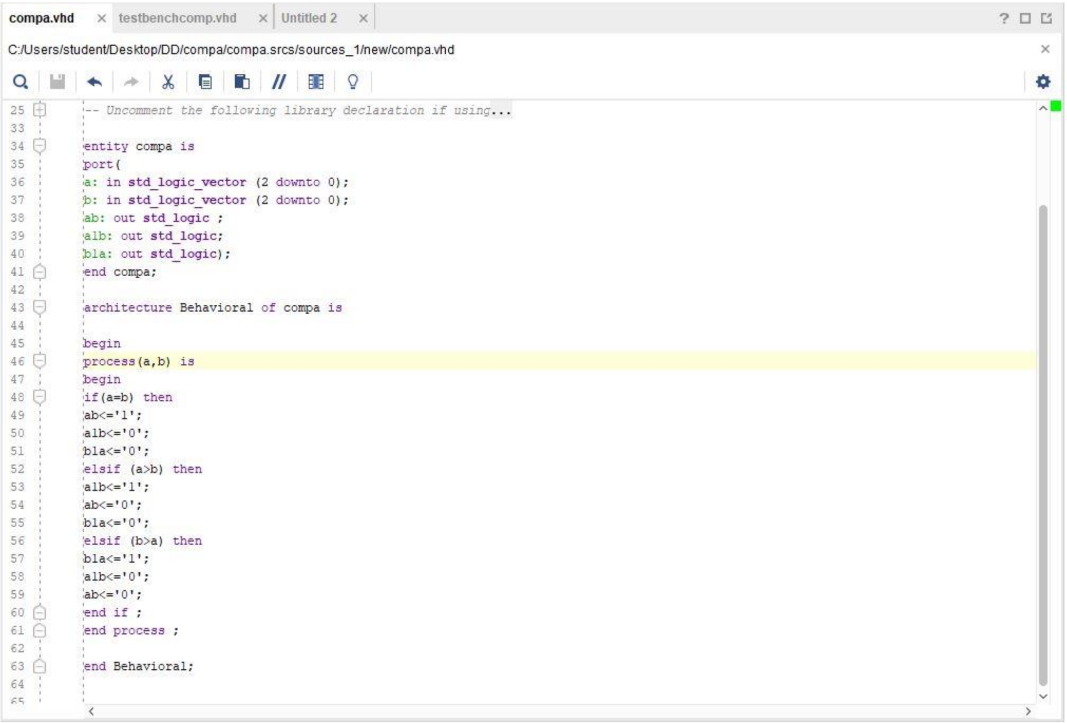
Design code: Structural



C:/Users/student/Desktop/DD/compa/compa.srcs/sources_1/new/compa.vhd

```
-------------------------------------------------------------------------------...


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using...

entity compa is
port(
a: in std_logic_vector (2 downto 0);
b: in std_logic_vector (2 downto 0);
ab: out std_logic ;
alb: out std_logic;
bla: out std_logic);
end compa;

architecture Behavioral of compa is

begin
process(a,b) is
begin
ab<=( (a(2)xnor b(2)) and (a(1) xnor b(1)) and (a(0) xnor b(0)) );
alb<= (a(2) and (not b(2))) or ((a(2)xnor b(2)) and (a(1) and (not b(1)))) or ( (a(2) xnor b(2)) and (a(1) xnor b(1)) and (a(0) and not b(0))) ;
bla<= (not a(2) and b(2) ) or ( (a(2) xnor b(2)) and (not a(1) and b(1))) or ( (a(2) xnor b(2)) and (a(1) xnor b(1)) and (not a(0) and b(0))) ;
end process ;

end Behavioral;
```

Design code: behavioral



C:/Users/student/Desktop/DD/compa/compa.srcs/sources_1/new/compa.vhd

```
-- Uncomment the following library declaration if using...

entity compa is
port(
a: in std_logic_vector (2 downto 0);
b: in std_logic_vector (2 downto 0);
ab: out std_logic ;
alb: out std_logic;
bla: out std_logic);
end compa;

architecture Behavioral of compa is

begin
process(a,b) is
begin
if(a=b) then
ab<='1';
alb<='0';
bla<='0';
elsif (a>b) then
alb<='1';
ab<='0';
bla<='0';
elsif (b>a) then
bla<='1';
alb<='0';
ab<='0';
end if ;
end process ;

end Behavioral;
```

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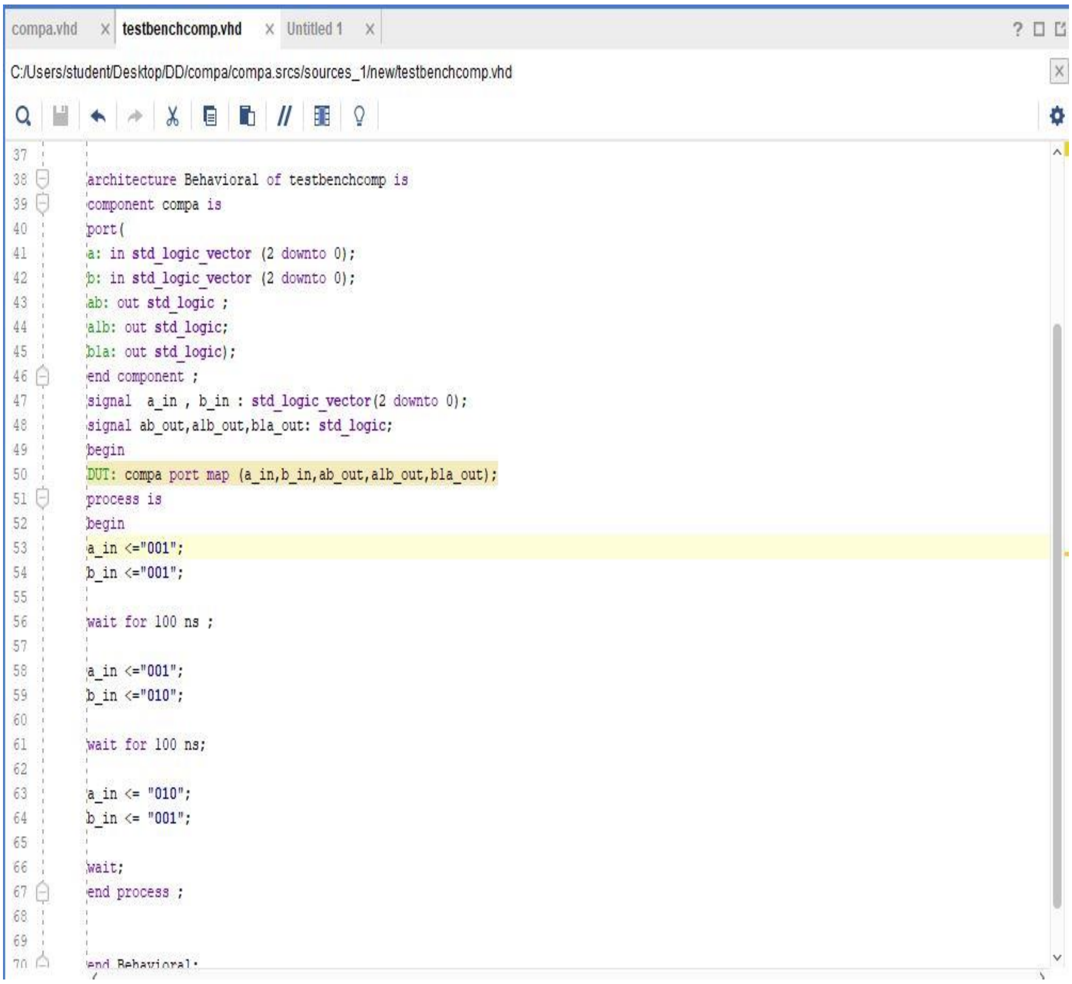
Testbench:



C:/Users/student/Desktop/DD/compa/compa.srcs/sources_1/new/testbenchcomp.vhd

```
architecture Behavioral of testbenchcomp is
component compa is
port(
a: in std_logic_vector (2 downto 0);
b: in std_logic_vector (2 downto 0);
ab: out std_logic ;
alb: out std_logic;
bla: out std_logic);
end component ;
signal  a_in , b_in : std_logic_vector(2 downto 0);
signal ab_out,alb_out,bla_out: std_logic;
begin
DUT: compa port map (a_in,b_in,ab_out,alb_out,bla_out);
process is
begin
a_in <="001";
b_in <="001";

wait for 100 ns ;

a_in <="001";
b_in <="010";

wait for 100 ns;

a_in <= "010";
b_in <= "001";

wait;
end process ;


end Behavioral;
```

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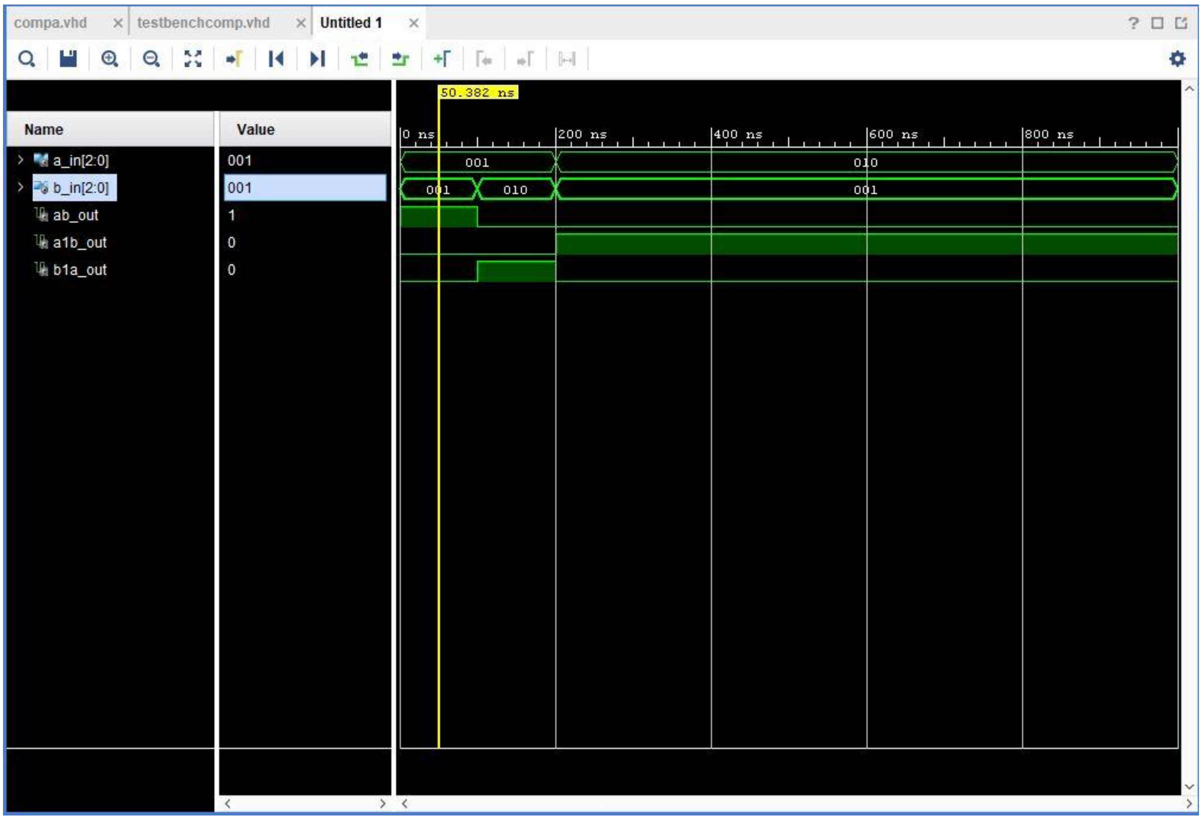
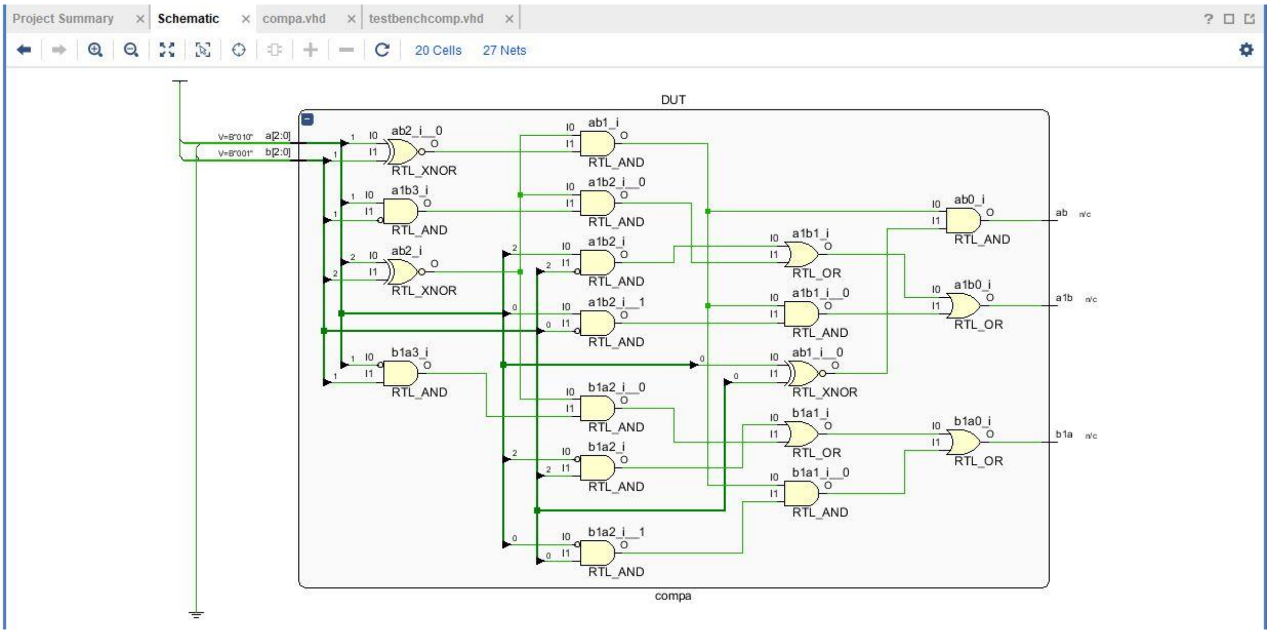
Simulation:



Name	Value
a_in[2:0]	001
b_in[2:0]	001
ab_out	1
a1b_out	0
b1a_out	0



Result:- 3-bit comparator implemented successfully, and their test results are shown above.