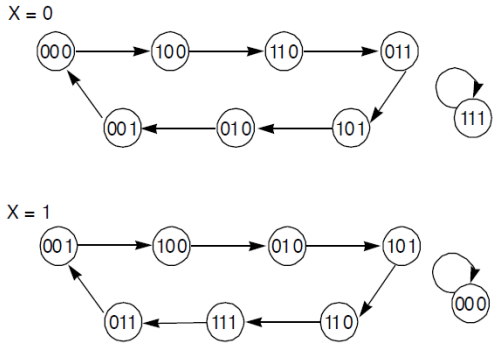
第四章布置习题参考解

4-7

Solution：

Present state			Input	Next state		
A	*B*	*C*	*X*	*A*	*B*	*C*
0	0	0	0	1	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	0	0	1
1	0	0	0	1	1	0
1	0	0	1	0	1	0
1	0	1	0	0	1	0
1	0	1	1	1	1	0
1	1	0	0	0	1	1



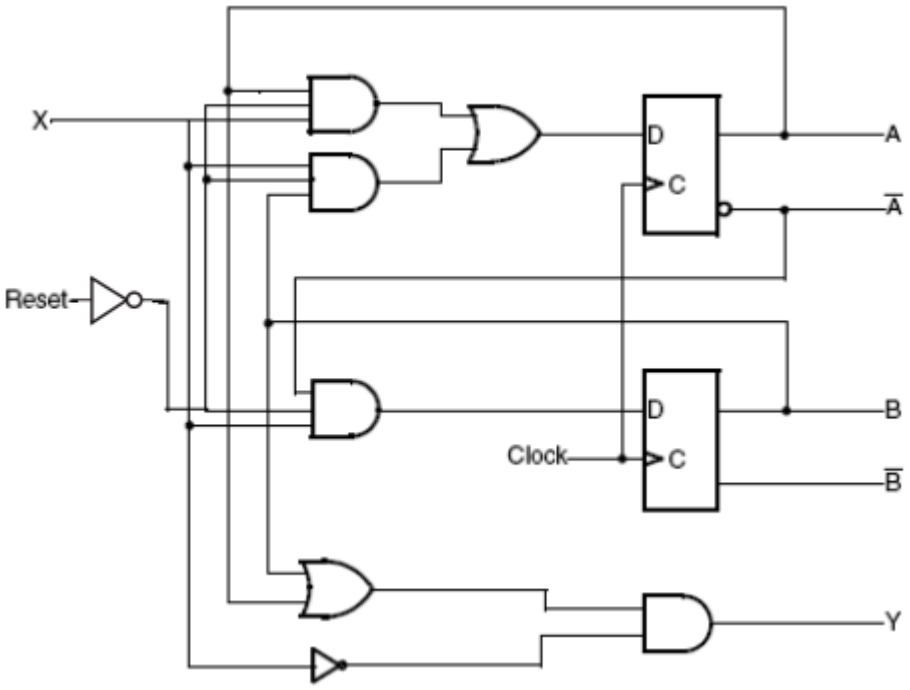
State diagram is the combination of the above two diagrams.

4-9

Present State	**00**	**01**	**00**	**00**	**01**	**11**	**00**	**01**	**11**	**10**	**10**
Input	**1**	**0**	**0**	**1**	**1**	**0**	**1**	**1**	**1**	**1**	**0**
Output	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**
Next State	**01**	**00**	**00**	**01**	**11**	**00**	**01**	**11**	**10**	**10**	**00**

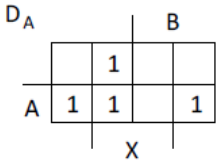
4-12（b）

在触发器输入端前面的每个与门上增加一个输入，接在 Reset 的非门上，当 Reset 为 1 时触发器输入为 0，实现同步复位。

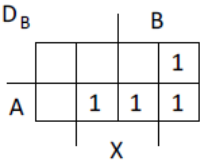


4-13

Present state		Input	Next state	
A	*B*	*X*	*A*	*B*
0	0	0	0	0
0	0	1	1	0
0	1	0	0	1
0	1	1	0	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	0	1



$D_A = A\overline{X} + \overline{B}X$



$D_B = AX + B\overline{X}$

Logic diagram not given.

4-21

穆尔状态图为：

Assumes for E = 0, the output remains

状态表：

Present state	Next State For Input		Output
$D_2D_1D_0$	*E=0*	*E=1*	*Z*
000	001	001	0
001	010	010	1
010	011	011	1
011	100	100	1
100	101	101	1
101	110	110	1
110	111	111	1
111	111	000	0

激励函数和输出函数：

$$D_2(t+1) = D_2\overline{D_1} + D_2\overline{D_0} + \overline{D_2}D_1D_0 + D_2\overline{E} \quad (D_2D_1D_0\overline{E})$$

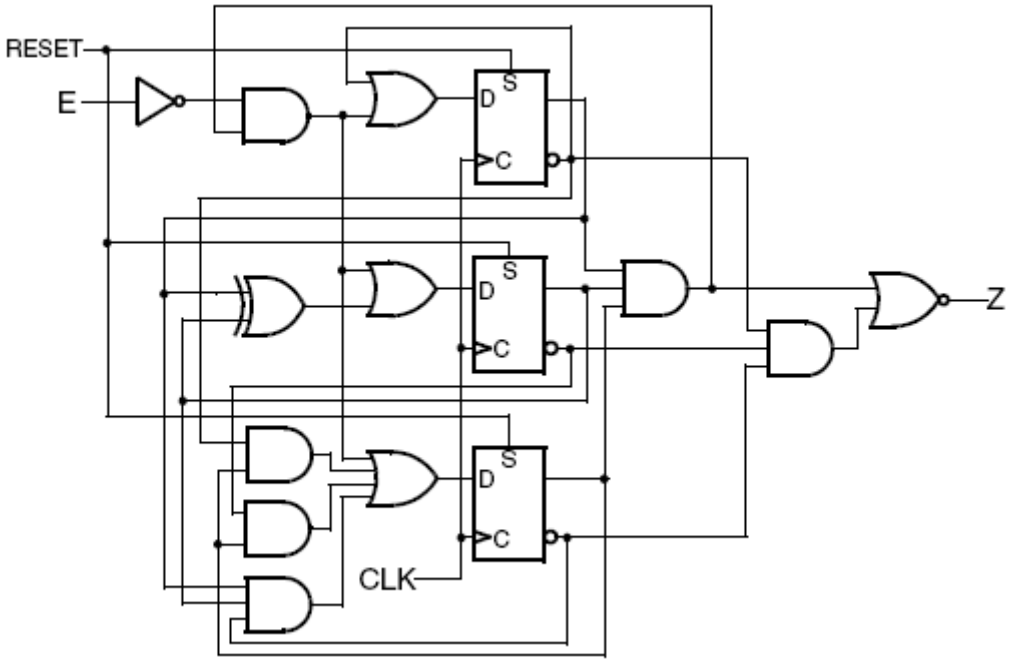
$$D_1(t+1) = D_1\overline{D_0} + \overline{D_1}D_0 + D_2D_0\overline{E} \quad (D_2D_1\overline{E},\quad D_2D_1D_0\overline{E})$$

$$D_0(t+1) = \overline{D_0} + D_2D_1\overline{E} \quad (D_2D_1D_0\overline{E})$$

$$Z = \overline{D_2D_1D_0 + \overline{D_2}\,\overline{D_1}\,\overline{D_0}} = D_1\overline{D_0} + D_2\overline{D_1} + \overline{D_2}D_0 = \overline{D_1}D_0 + \overline{D_2}D_1 + D_2\overline{D_0}$$

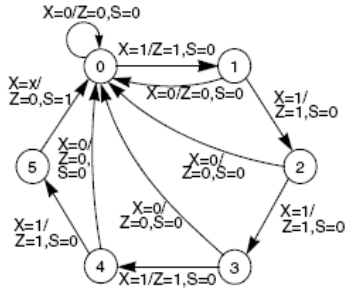
为了能够产生第一个0输出，复位时应该复位到“111”状态，所以Reset信号应该连到所有触发器的异步置位引脚。

电路图：



4-22

按照题意，电路需要能够接受带有停顿的输入序列，出现连续5个“1”以后忽略插入的一位，此时输出Z = 0，S = 1。因此状态图为：



Present state			Input	Next state			Output	
A	*B*	*C*	*X*	*A*	*B*	*C*	*Z*	*S*
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	1	0
0	0	1	0	0	0	0	0	0
0	0	1	1	0	1	0	1	0
0	1	0	0	0	0	0	0	0
0	1	0	1	0	1	1	1	0
0	1	1	0	0	0	0	0	0
0	1	1	1	1	0	0	1	0
1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	1	1	0
1	0	1	0	0	0	0	0	1
1	0	1	1	0	0	0	0	1

$$D_A = A\overline{C}X + BCX$$

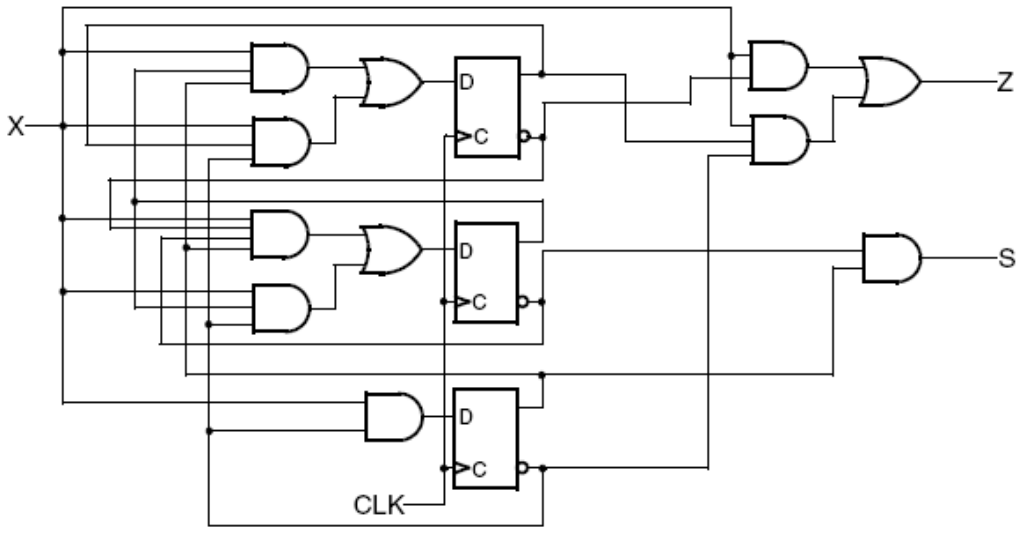
$$D_B = B\overline{C}X + \overline{A}\overline{B}CX$$

$$D_C = \overline{C}X$$

$$Z = \overline{A}X + \overline{C}X = (\overline{A} + \overline{C})X$$

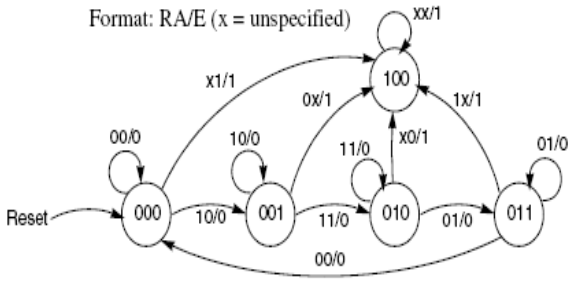
$$S = AC$$

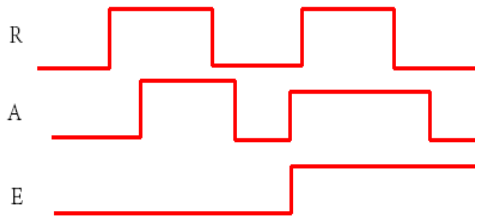
电路图为：



4-25

按照输入RA=00、10、11、01的顺序设立4个状态，表示正常工作时的状态循环，再设立一个异常状态，当出现错误输入时就转到异常状态去。状态图为：





状态表：

Present state			Inputs		Next state			Output
B	*C*	*D*	*R*	*A*	*B*	*C*	*D*	*E*
0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	0	0	1
0	0	0	1	0	0	0	1	0
0	0	0	1	1	1	0	0	1
0	0	1	0	0	1	0	0	1
0	0	1	0	1	1	0	0	1
0	0	1	1	0	0	0	1	0
0	0	1	1	1	0	1	0	0
0	1	0	0	0	1	0	0	1
0	1	0	0	1	0	1	1	0
0	1	0	1	0	1	0	0	1
0	1	0	1	1	0	1	0	0

Present state			Inputs		Next state			Output
B	*C*	*D*	*R*	*A*	*B*	*C*	*D*	*E*
0	1	1	0	0	0	0	0	0
0	1	1	0	1	0	1	1	0
0	1	1	1	0	1	0	0	1
0	1	1	1	1	1	0	0	1
1	0	0	0	0	1	0	0	1
1	0	0	0	1	1	0	0	1
1	0	0	1	0	1	0	0	1
1	0	0	1	1	1	0	0	1

4-29

假设无效的下一状态是不考虑的情况下，列出状态表为：

现态	次态	输出
A B C	A B C	X Y Z

0 0 0	1 0 0	0 0 0
0 0 1	0 0 0	0 0 1
0 1 0	x x x	0 1 0
0 1 1	0 0 1	0 1 1
1 0 0	1 1 0	1 0 0
1 0 1	x x x	1 0 1
1 1 0	1 1 1	1 1 0
1 1 1	0 1 1	1 1 1

a) 根据状态表，可写出激励函数和输出函数：

$$D_A = \overline{C}$$
$$D_B = A$$
$$D_C = B$$
$$X = A$$
$$Y = B$$
$$Z = C$$

电路图略

b) 将$\overline{\text{Rese}}$信号连接至各个触发器的异步复位端。

c)~f) The circuit is suitable for child's toy, but not for life critical applications. In the case of the child's toy, it is the cheapest implementation. If an error occurs the child just needs to reset it. In life critical applications, the immediate detection of errors is critical. The circuit above enters invalid states for some errors. For a life critical application, additional circuitry is needed for immediate detection of the error ($E = A\overline{B}C + \overline{A}B\overline{C}$). This circuit using the design in a), does return from the invalid states to a valid state automatically after one or two clock periods.

4-58

a) 在28ns附近，Clock上升沿之前D1不满足建立时间约束。

b) 在16ns附近，Clock下降沿之后D2不满足保持时间约束；在24ns附近，Clock下降沿之前D2不满足建立时间约束。

4-59

a) The longest direct path delay is from input X through the two XOR gates to the output Y.

$t_{delay} = t_{pdXOR} + t_{pdXOR} = 0.04 + 0.04 = 0.08$ ns

b) The longest path from an external input to a positive clock edge is from input X through the XOR gate and the inverter to the B Flip-flop.

$t_{delay} = t_{pdXOR} + t_{pdINV} + t_{sFF} = 0.04 + 0.01 + 0.02 = 0.07$ ns

c) The longest path delay from the positive clock edge is from Flip-flop A through the two XOR gates to the output Y.

$t_{delay} = t_{pdFF} + 2\, t_{pdXOR} = 0.08 + 2(0.04) = 0.16$ ns

d) The longest path delay from positive clock edge to positive clock edge is from clock on Flip-flop A through the XOR gate and inverter to clock on Flip-flop B.

$t_{delay\text{-clock edge to clock edge}} = t_{pdFF} + t_{pdXOR} + t_{pdINV} + t_{sFF} = 0.08 + 0.04 + 0.01 + 0.02 = 0.15$ ns

e) The maximum frequency is $1/t_{delay\text{- clock edge to clock edge}}$. For this circuit, $t_{delay\text{-clock edge to clock edge}}$ is 0.15 ns, so the maximum frequency is 1/0.15 ns = 6.67 GHz.

Comment: The clock frequency may need to be lower due to other delay paths that pass outside of the circuit into its environment. Calculation of this frequency cannot be performed in this case since data for paths through the environment is not provided.