DDCO MINI PROJECT-PHASE 2

GROUP NO:11

TITLE: DESIGN AND IMPLEMENT A SEQUENCE GENERATOR

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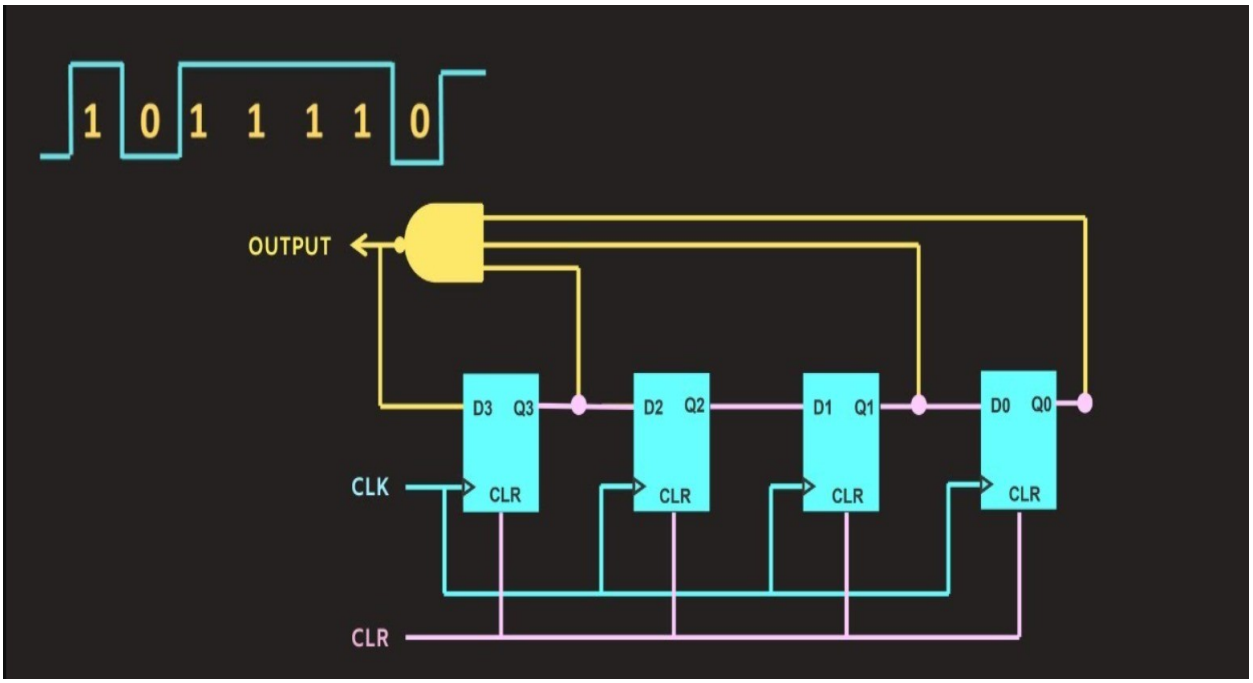
ABSTRACT:

A 4-bit sequence generator using D flip-flops is a sequential digital circuit designed to generate a binary counting sequence from 0000 to 1111 (0 to 15 in decimal) in synchronization with a clock signal. The circuit uses four D flip-flops, where each flip-flop represents one bit of the binary sequence. The D flip-flops are arranged in a chain to form a binary counter, with the output of one flip-flop connected to the input of the next.

The circuit is driven by a clock signal that triggers state changes on each rising edge, making the output increment by 1 with each clock pulse. A reset signal is used to initialize the flip-flops and set the output to 0000, ensuring the counter starts from the beginning of the sequence. As the clock progresses, the circuit produces a continuous binary count, which can be used in applications like timers, counters, or sequence detection.

This design is fundamental in digital electronics, providing a basic yet versatile method for generating binary sequences. The simplicity and efficiency of D flip-flops make this approach ideal for implementing small-scale binary counters, often used in microcontrollers, digital clocks, and other timing-related circuits.

CIRCUIT:



Code:

sequence_generator.v

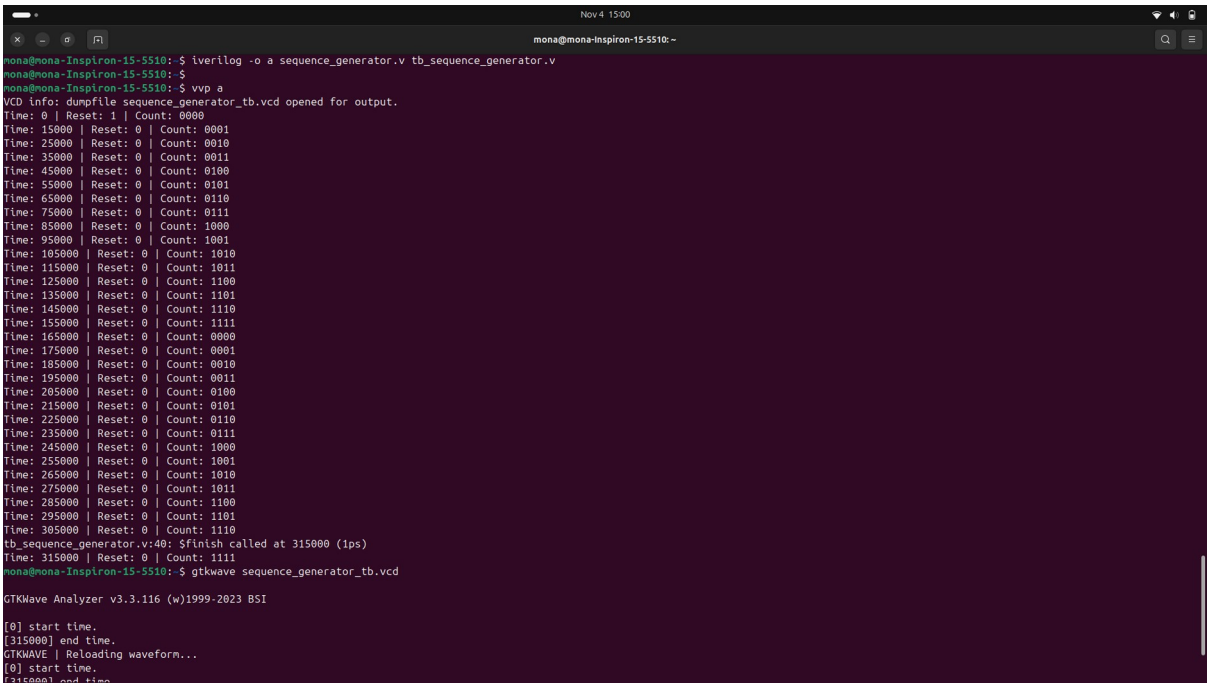
```
module sequence_generator (
    input wire clk,
    input wire reset,
    output reg [3:0] count
);
    always @(posedge clk or posedge reset) begin
        if (reset) begin
            count <= 4'b0000;
        end else begin
            count <= count + 1;
        end
    end

endmodule
```

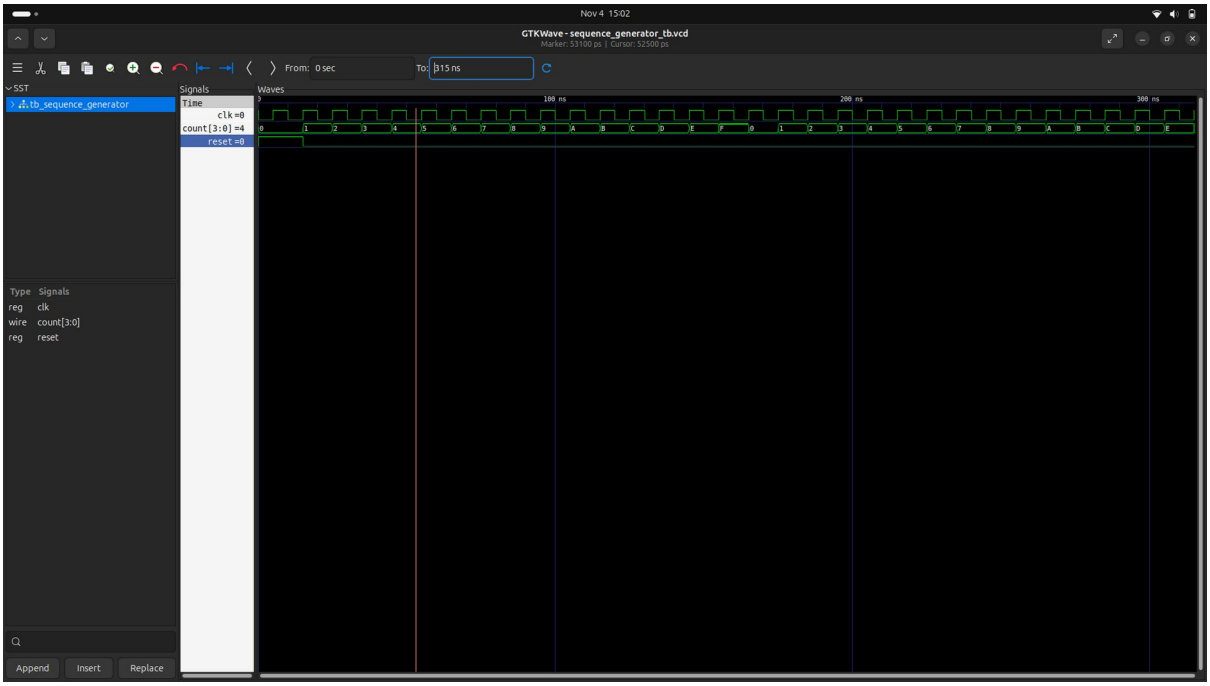
tb_sequence_generator.v

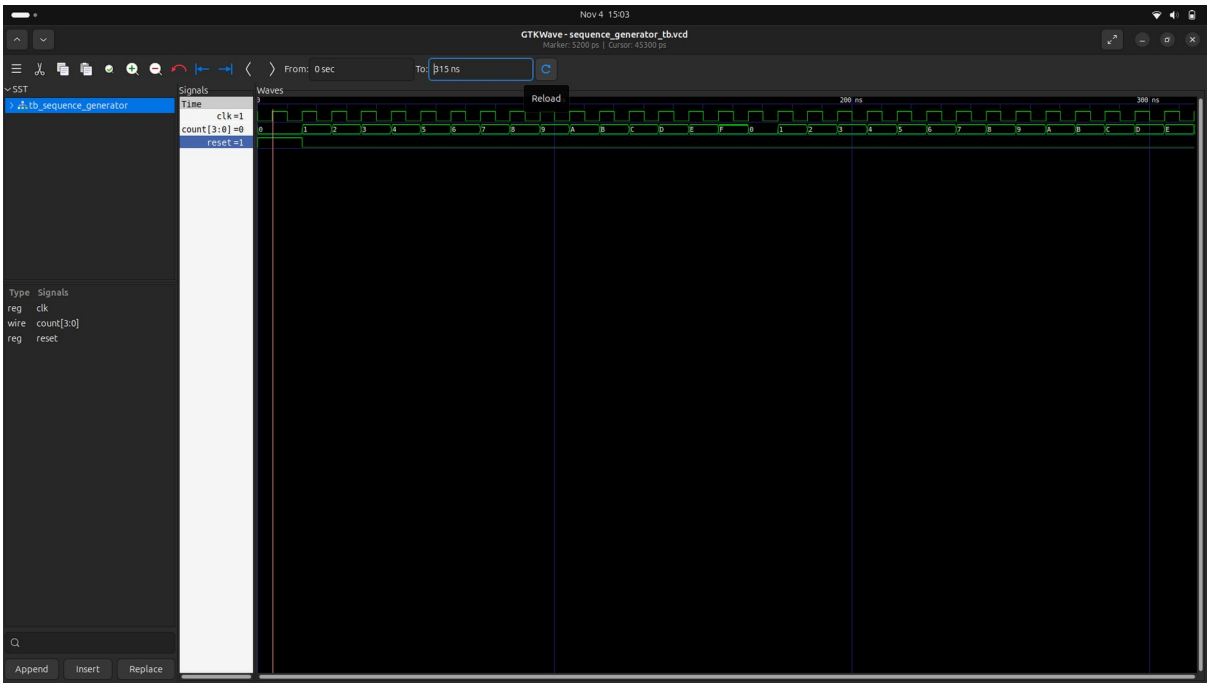
```
`timescale 1ns / 1ps
module tb_sequence_generator;

    reg clk;
    reg reset;
    wire [3:0] count;
    sequence_generator uut (
        .clk(clk),
        .reset(reset),
        .count(count)
    );
    initial begin
        clk = 0;
        forever #5 clk = ~clk;
    end
```

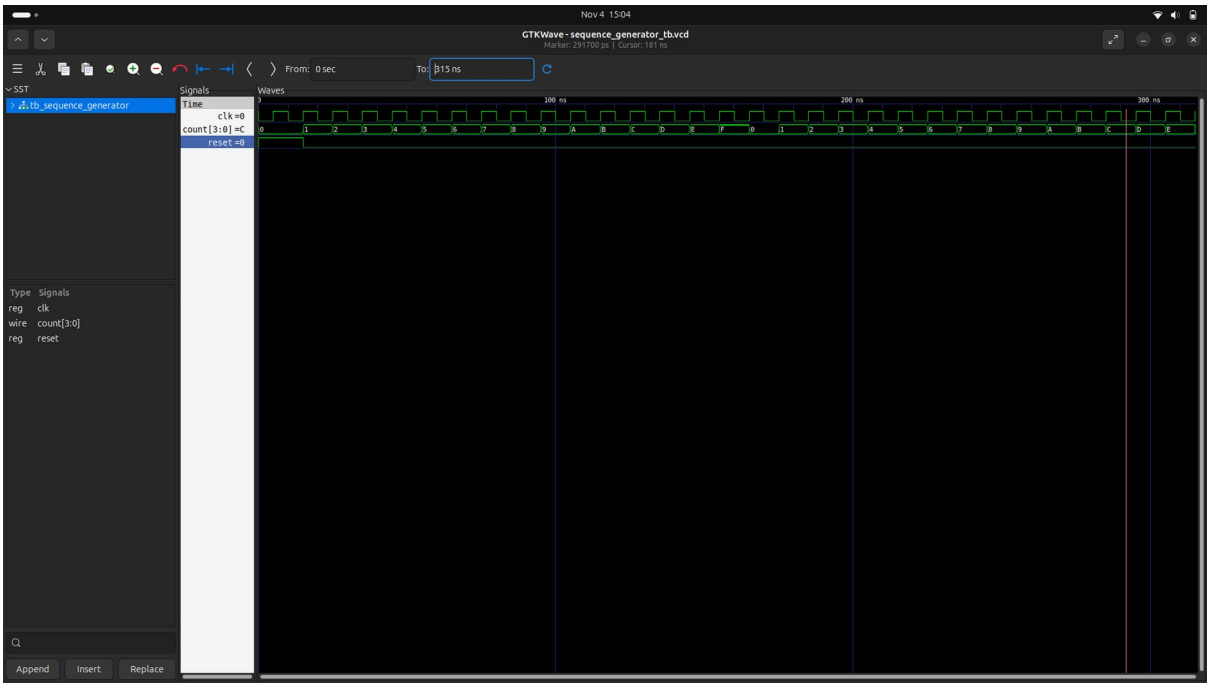
```
    initial begin
        $monitor("Time: %0t | Reset: %b | Count: %b", $time, reset, count);
        $dumpfile("sequence_generator_tb.vcd"); // Set output VCD file name
        $dumpvars(0, tb_sequence_generator);    // Dump variables in the current module
        reset = 1;
        #15;
        reset = 0;
        #300;
        $finish;
    end

endmodule
```

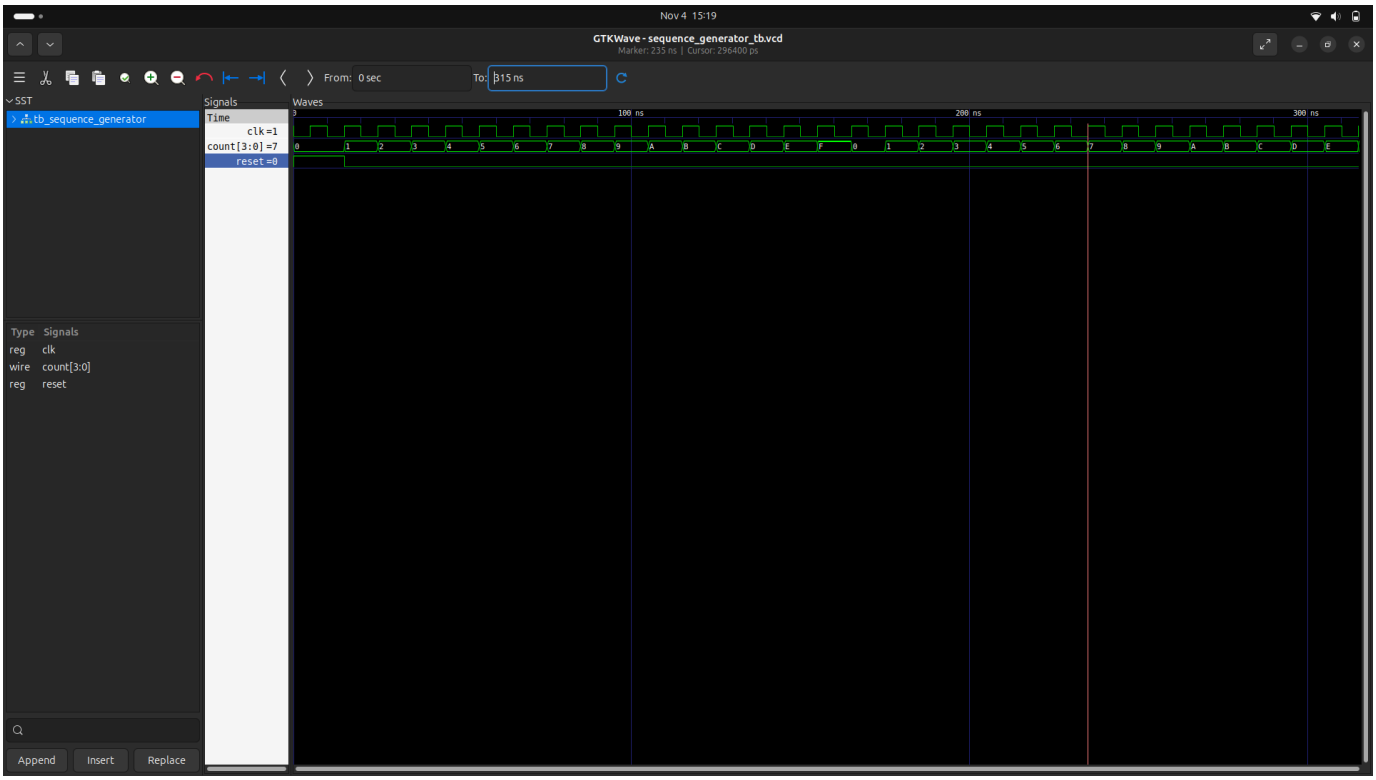
OUTPUT:




Nov 4 15:02
GTKWave - sequence_generator_tb.vcd
From: 0 sec
To: 315 ns
SST
tb_sequence_generator
Signals
Waves
Time
clk=0
count[3:0]=4
reset=0
100 ns
200 ns
300 ns
Type Signals
reg clk
wire count[3:0]
reg reset
Append
Insert
Replace


Nov 4 15:03
GTKWave - sequence_generator_tb.vcd
From: 0 sec
To: 315 ns
Reload
SST
tb_sequence_generator
Signals
Waves
Time
clk=1
count[3:0]=0
reset=1
200 ns
300 ns
Type Signals
reg clk
wire count[3:0]
reg reset
Append
Insert
Replace


Nov 4 15:04
GTKWave - sequence_generator_tb.vcd
Marker: 291700 ps | Cursor: 181 ns
From: 0 sec
To: 315 ns
SST
tb_sequence_generator
Signals
Time
clk =0
count[3:0] =C
reset =0
Waves
100 ns
200 ns
300 ns
Type Signals
reg clk
wire count[3:0]
reg reset
Append
Insert
Replace


Nov 4 15:19
GTKWave - sequence_generator_tb.vcd
Marker: 235 ns | Cursor: 296400 ps
From: 0 sec
To: 315 ns
SST
tb_sequence_generator
Signals
Time
clk =1
count[3:0] =7
reset =0
Waves
100 ns
200 ns
300 ns
Type Signals
reg clk
wire count[3:0]
reg reset
Append
Insert
Replace

Disclaimer:

The programs and output submitted are duly written, verified and executed by us.
We have not copied from any of our peers nor from external resources such as the internet. If found plagiarized, we will abide with the disciplinary action of the University.

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THANK YOU!