



END SEMESTER ASSESSMENT (ESA)
B.TECH. (CSE)
III SEMESTER

**UE23CS251A – DIGITAL DESIGN & COMPUTER
ORGANIZATION LABORATORY**

PROJECT REPORT
ON

“TITLE OF THE PROJECT.”
Team No.

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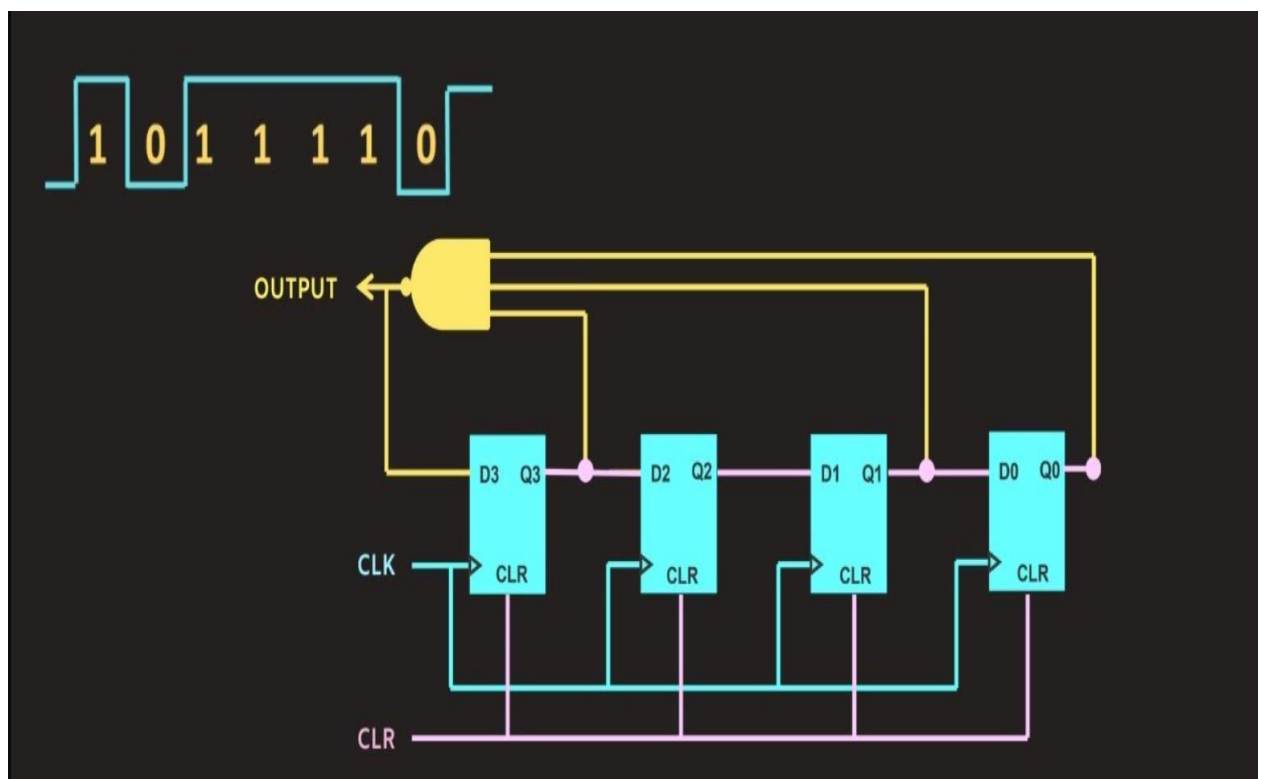
ABSTRACT OF THE PROJECT:

A 4-bit sequence generator using D flip-flops is a sequential digital circuit designed to generate a binary counting sequence from 0000 to 1111 (0 to 15 in decimal) in synchronization with a clock signal. The circuit uses four D flip-flops, where each flip-flop represents one bit of the binary sequence. The D flip-flops are arranged in a chain to form a binary counter, with the output of one flip-flop connected to the input of the next.

The circuit is driven by a clock signal that triggers state changes on each rising edge, making the output increment by 1 with each clock pulse. A reset signal is used to initialize the flip-flops and set the output to 0000, ensuring the counter starts from the beginning of the sequence. As the clock progresses, the circuit produces a continuous binary count, which can be used in applications like timers, counters, or sequence detection.

This design is fundamental in digital electronics, providing a basic yet versatile method for generating binary sequences. The simplicity and efficiency of D flip-flops make this approach ideal for implementing small-scale binary counters, often used in microcontrollers, digital clocks, and other timing-related circuits.

CIRCUIT DIAGRAM:



MAIN VERILOG CODE:

sequence_generator.v

```
module sequence_generator (
    input wire clk,
    input wire reset,
    output reg [3:0] count
);
    always @(posedge clk or posedge reset) begin
        if (reset) begin
            count <= 4'b0000;
        end else begin
            count <= count + 1;
        end
    end
endmodule
```

TEST BENCH FILE:

```
`timescale 1ns / 1ps
module tb_sequence_generator;

    reg clk;
    reg reset;
    wire [3:0] count;
    sequence_generator uut (
        .clk(clk),
        .reset(reset),
        .count(count)
    );
    initial begin
        clk = 0;
        forever #5 clk = ~clk;
    end
    initial begin
        $monitor("Time: %0t | Reset: %b | Count: %b", $time, reset, count);
        $dumpfile("sequence_generator_tb.vcd"); // Set output VCD file name
        $dumpvars(0, tb_sequence_generator); // Dump variables in the current
module
    reset = 1;
    #15;
    reset = 0;
    #300;
    $finish;
end
endmodule
```

SCREEN SHOT OF THE OUTPUT:

```
mona@mona-Inspiron-15-5510:~$ verilog -o a sequence_generator.v tb_sequence_generator.v
mona@mona-Inspiron-15-5510:~$
mona@mona-Inspiron-15-5510:~$ vvp a
VCD info: dumpfile sequence_generator_tb.vcd opened for output.
Time: 0 | Reset: 1 | Count: 0000
Time: 15000 | Reset: 0 | Count: 0001
Time: 25000 | Reset: 0 | Count: 0010
Time: 35000 | Reset: 0 | Count: 0011
Time: 45000 | Reset: 0 | Count: 0100
Time: 55000 | Reset: 0 | Count: 0101
Time: 65000 | Reset: 0 | Count: 0110
Time: 75000 | Reset: 0 | Count: 0111
Time: 85000 | Reset: 0 | Count: 1000
Time: 95000 | Reset: 0 | Count: 1001
Time: 105000 | Reset: 0 | Count: 1010
Time: 115000 | Reset: 0 | Count: 1011
Time: 125000 | Reset: 0 | Count: 1100
Time: 135000 | Reset: 0 | Count: 1101
Time: 145000 | Reset: 0 | Count: 1110
Time: 155000 | Reset: 0 | Count: 1111
Time: 165000 | Reset: 0 | Count: 0000
Time: 175000 | Reset: 0 | Count: 0001
Time: 185000 | Reset: 0 | Count: 0010
Time: 195000 | Reset: 0 | Count: 0011
Time: 205000 | Reset: 0 | Count: 0100
Time: 215000 | Reset: 0 | Count: 0101
Time: 225000 | Reset: 0 | Count: 0110
Time: 235000 | Reset: 0 | Count: 0111
Time: 245000 | Reset: 0 | Count: 1000
Time: 255000 | Reset: 0 | Count: 1001
Time: 265000 | Reset: 0 | Count: 1010
Time: 275000 | Reset: 0 | Count: 1011
Time: 285000 | Reset: 0 | Count: 1100
Time: 295000 | Reset: 0 | Count: 1101
Time: 305000 | Reset: 0 | Count: 1110
tb_sequence_generator.v:40: $finish called at 315000 (1ps)
Time: 315000 | Reset: 0 | Count: 1111
mona@mona-Inspiron-15-5510:~$ gtkwave sequence_generator_tb.vcd

GTKWave Analyzer v3.3.116 (w)1999-2023 BSI

[0] start time.
[315000] end time.
GTKWAVE | Reloading waveform...
[0] start time.
[315000] end time.
```

