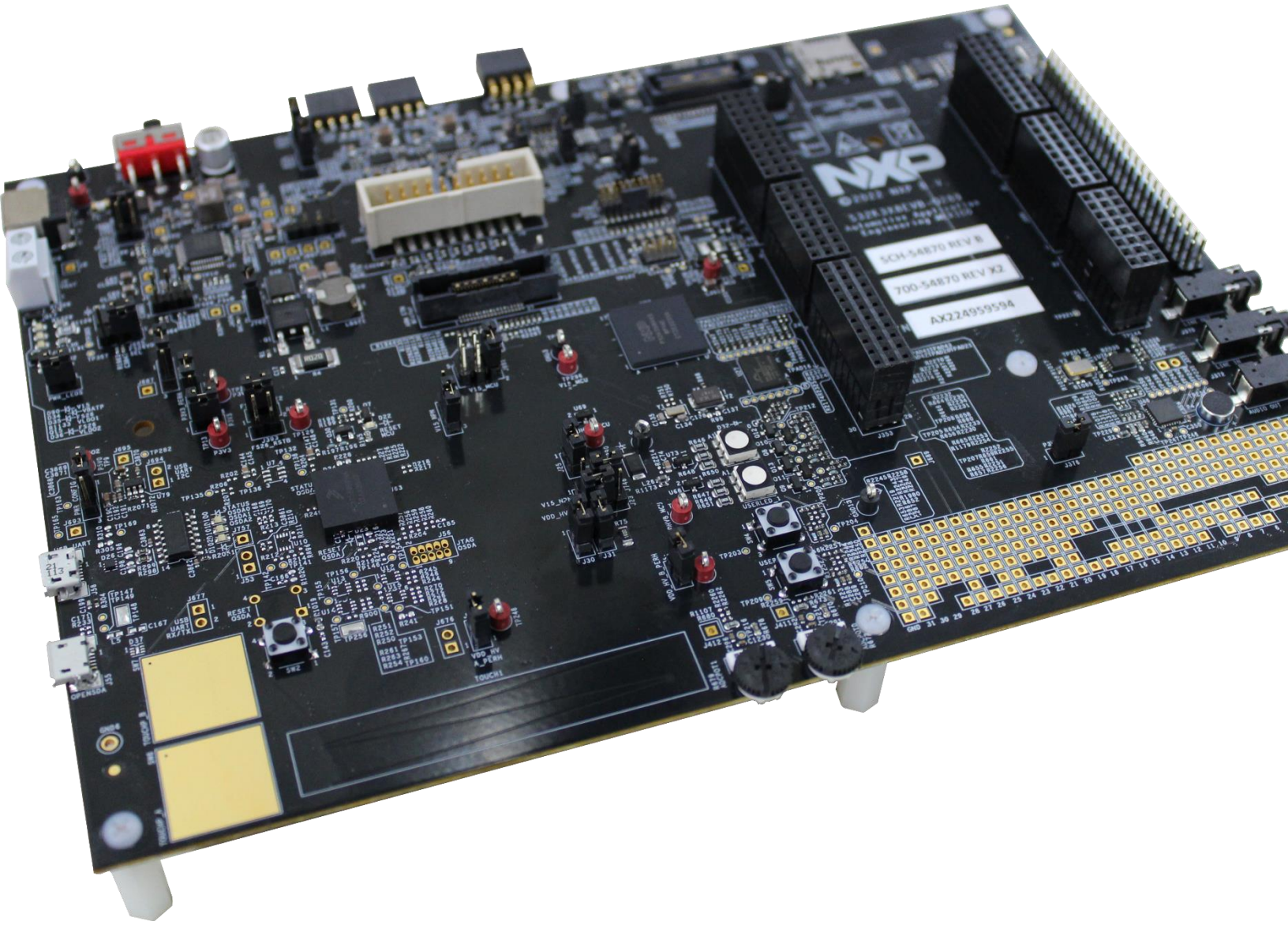
S32K3X8EVB-Q289

Customer Evaluation Board for S32K3x8 MCUs
Hardware User Manual



1 Table of contents

2 Definitions, Acronyms, and Abbreviations

The following list defines the abbreviations used in this document.

CD	Compact Disk
CMOS	Complementary Metal Oxide Semiconductor
CPLD	Custom Programmed Logic Devices
CPU	Central Processing Unit
CSI	Camera Sensor Imaging
CSPI	Configurable Serial Peripheral Interface
DDR	Double Data Rate
DIP	Dual In-line Package
EEPROM	Electrically Erasable Programmable Read Only Memory
EPROM	Erasable Programmable Read Only Memory
GPIO	General Purpose Input/output
GPO	General Purpose Output
I2C	Inter-Integrated Circuit
ICE	In-Circuit Emulator
I/O	Input/output
JTAG	Joint Test Access Group
LAN	Local Area Network
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MB	Megabyte
MCU	Microcontroller Unit
MMC	Multi-Media Card
MCP	Multi-chip product
MS	Memory Stick
NVRAM	Non-volatile Random-Access Memory
PC	Personal Computer
PCB	Printed Circuit Board
PHY	Physical interface
POR	Power on Reset
PSRAM	Pseudo Random Access Memory
PWR	Power
PWM	Pulse Width Modulation
QVGA	Graphics Adapter
RAM	Random Access Memory
SD	SanDisk (Smart Media)
SDRAM	Synchronous Dynamic Random-Access Memory
SI	System International (international system of units and measures)
SIMM	Single In-Line Memory Module
SPST	Single Pole Single Throw
TFT	Thin Film Transistor
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus.
HW	Hardware.
POP	Populate – Component placed
DNP	Do not populate – Component removed

3 S32K3X8EVB-Q289 - Block Diagram

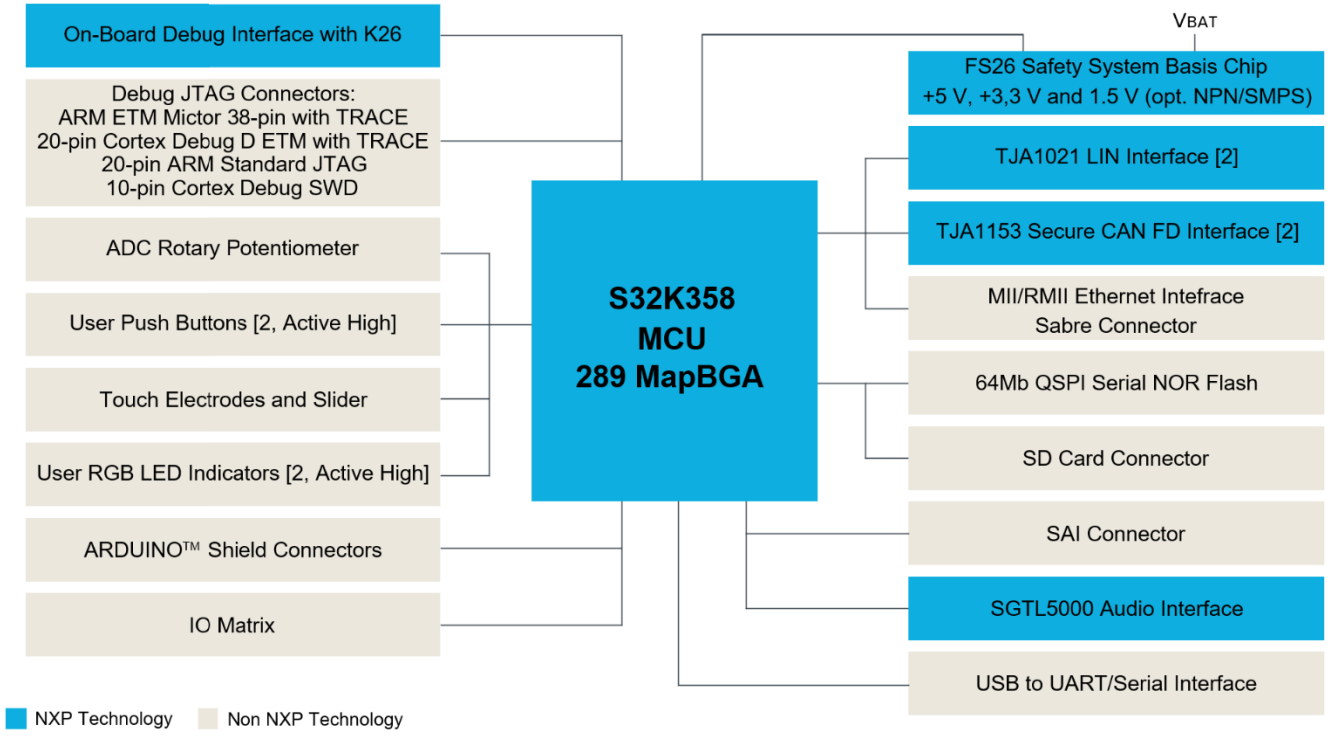


Figure 1. S32K3X8EVB-Q289 – Block diagram

4 S32K3X8EVB-Q289 - Features

IMPORTANT
• Verify and download the last version of this document in http://www.nxp.com • Before the S32K358 Evaluation board is used or power is applied, please fully read this user manual. An incorrect configuration in the board may cause a irreparable damage on the component, MCU or EVB. Power must be removed from the EVB prior to: - Removing or placing some component or measurement - Re-configuring the board jumpers

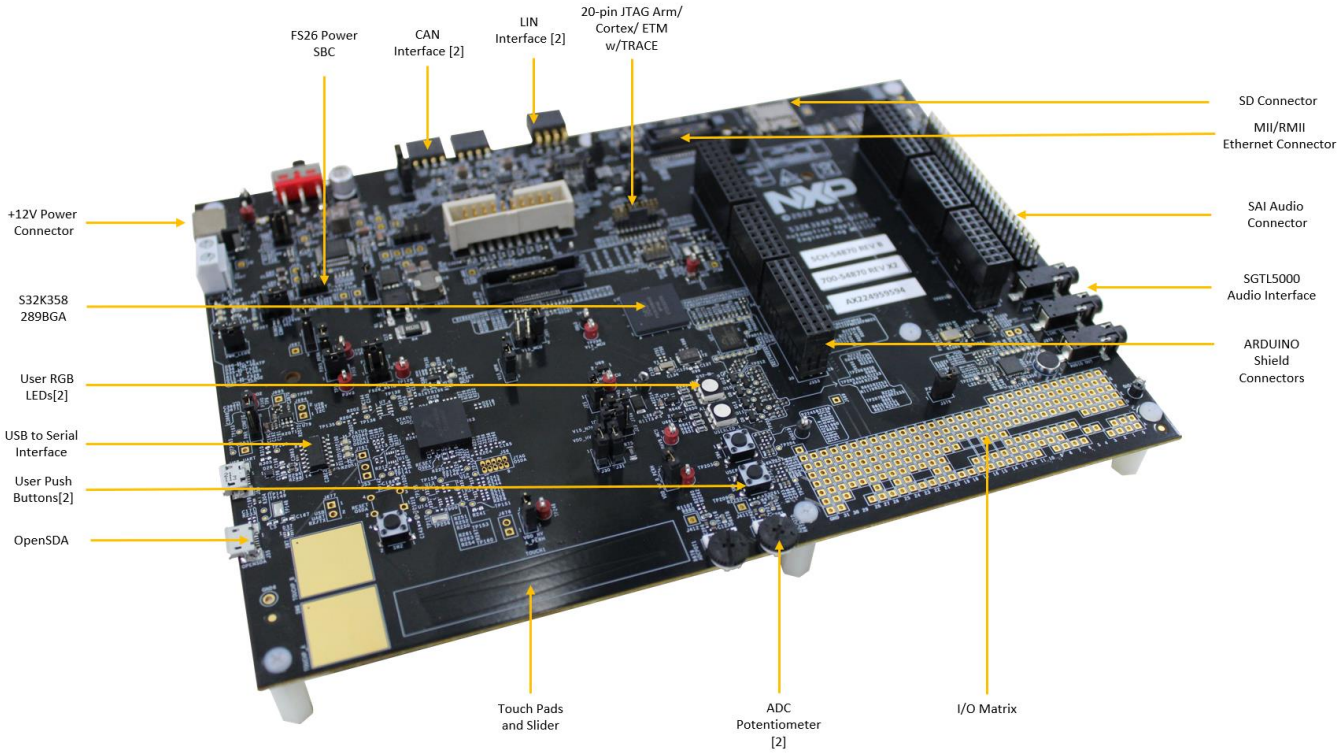


Figure 2. S32K3X8EVB-Q289 – Features

5 S32K3X8EVB-Q289 - Default Configuration

Table 1. S32K3X8EVB-Q289 - Default Configuration

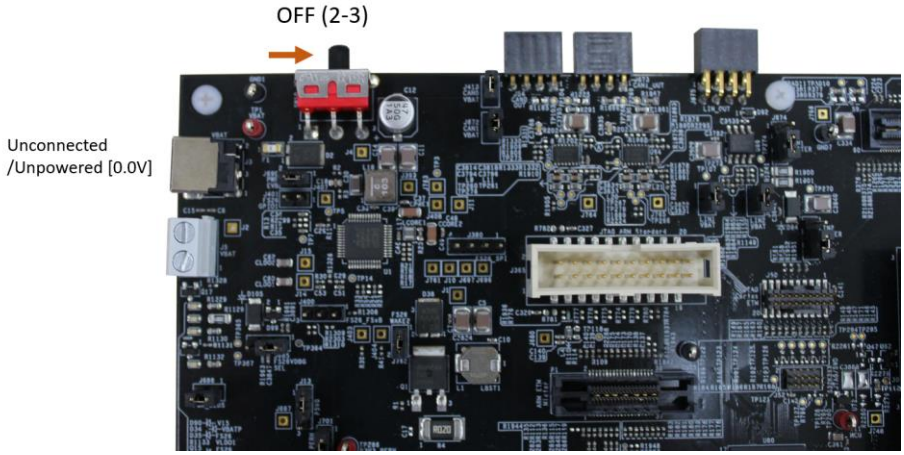
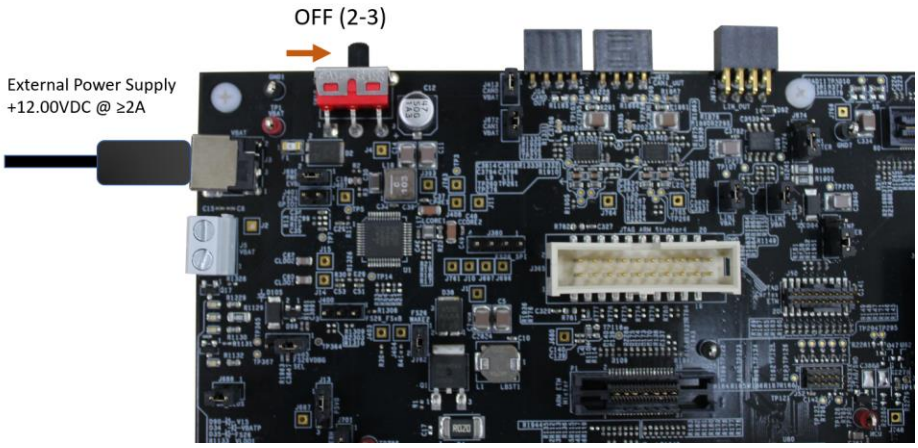
Interface	S32K3X8EVB -Q289	Reference / Signal	Default Configuration	Description/Comment
S32K358 V1.01 MCU	●	U80	V1.01	P32K358GGT0VJBST
MCU Power Supply	●	VDD_HV_A_MCU	+5.0V	The VDDA_HV_A domain is connected to +5.0V– Switching Power Supply
	●	VDD_HV_B_MCU	+3.3V	The VDDA_HV_B domain is connected to +3.3V– Switching Power Supply
	●	VDD_REFH_MCU	[VDD_HV_A]	The VDD_REFH domain is connected to VDD_HV_A_MCU
	●	V15_MCU	External NPN Transistor	The V15_MCU domain is routed to the external NPN Ballast Transistor
Ethernet	●	J63	MII/RMII Enabled	Ethernet MII signals are routed to ENET SABRE connector.

Interface	S32K3X8EVB-Q289	Reference / Signal		Default Configuration	Description/Comment
QSPI-A Memory	●	U27		Enabled	The MCU signals to the QSPI-A Memory Interface are enabled
Open SDA	●			PTA15	PTA15/LPUART6_RX is routed to OpenSDA for serial interface
				PTA16	PTA16/LPUART6_TX is routed to OpenSDA for serial interface
TRACE	●	J50		Disabled	The TRACE Signals are disabled as DEFAULT in the 20pin Cortex Debug D ETM Connector
CAN Interface	●	TJA115	/CAN0	PTA6	PTA6 is routed to the CAN0_RX
				PTA7	PTA7 is routed to the CAN0_TX
				PTC23	PTC23 is routed to the CAN0_ERRN
				PTC21	PTC21 is routed to the CAN0_EN
				PTC20	PTC20 is routed to the CAN0_STB
			/CAN1	PTE14	PTE14 is routed to the CAN1_RX
				PTE3	PTE3 is routed to the CAN1_TX
				PTE8	PTE8 is routed to the CAN1_ERRN
				PTB20	PTB20 is routed to the CAN1_EN
				PTD13	PTD13 is routed to the CAN1_STB
LIN Interface	●	LIN1		PTB9	LPUART9_RX is routed to LIN PHY1
				PTB10	LPUART9_TX is routed to LIN Phy1
		LIN2		PTE5	LPUART5_RX is routed to LIN Phy2
				PTE4	LPUART5_TX is routed to LIN Phy2
User Push Buttons	●	SW0		PTH1	Active High,
		SW1		PTH3	Active High,
User LEDs	●	D32		PTG29	Red
				PTG30	Green
				PTG31	Blue
	●	D33		PTF21	Red
				PTF22	Green
				PTF23	Blue
ADC Potentiometers	●	ADC_POT0		PTA11	ADCPOT0 [R672] is routed to PTA11 - ADC1_S10
	●	ADC_POT1		PTA17	ADCPOT1 [R679] is routed to PTA17 – ADC2_S19
SD Card	●	J700		PTA31	uSDHC_D0 is routed to PTA31 as default
				PTB18	uSDHC_D1 is routed to PTB18 as default
				PTB19	uSDHC_D2 is routed to PTB19 as default
				PTA29	uSDHC_D3 is routed to PTA29 as default
				PTB26	uSDHC_CMD is routed to PTB26 as default
				PTA30	uSDHC_CLK is routed to PTA30 as default
ARDUINO	●	-		-	

6 S32K3X8EVB-Q289 - Startup

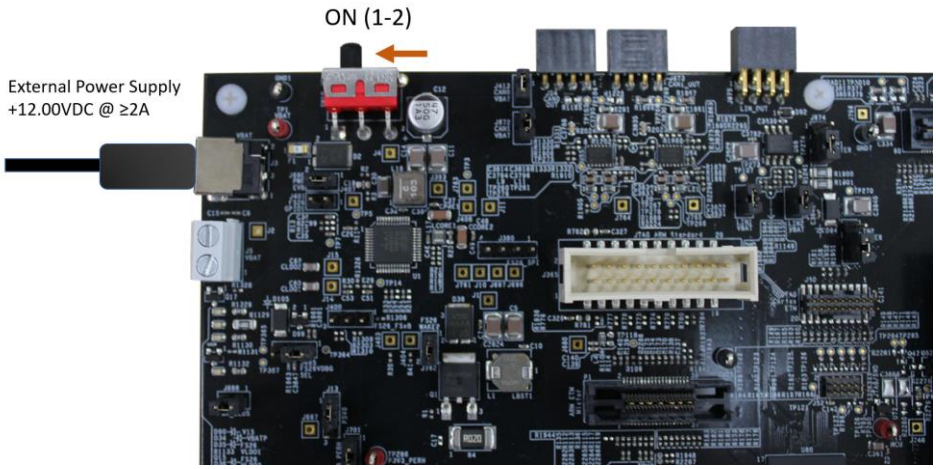
Follow these steps to connect and power on the board

1. Carefully unpack the S32K3X8EVB-Q289 and observe ESD preventive measures while handling the K3 development board.
2. Connect necessary cables between host PC and EVB board prior to applying power to the EVB.
3. The power-ON sequence for the EVB must be as follows:

a)	The power switch -SW10 must be in OFF-position before to the EVB be connected to an external power supply. 
b)	Once the power switch SW10 is in OFF-position, then the EVB can be connected to an external power supply. 

c)

Now the power switch SW10 can be changed to ON-position.



4. When power is applied to the EVB, three orange LEDs adjacent to the voltage regulators show the presence of the supply voltages as follows:
   - LED D34 Indicates that the +12.0V is connected to the EVB correctly.
   - LED D35 Indicates that the +5.0V linear regulator is enabled and working correctly.
   - LED D36 Indicates that the +3.3V linear regulator is enabled and working correctly.

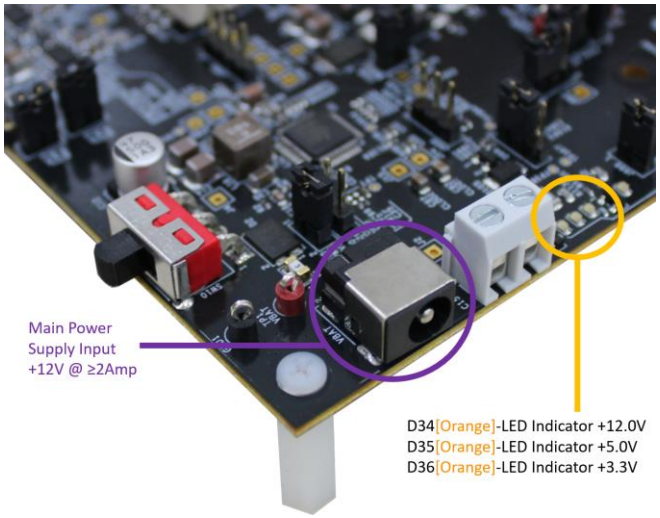


Figure 3. S32K3X8EVB-Q289 – Power supply Input and LED power indicators

If no LED are illuminated when power is applied to the EVB and the regulators are correctly enabled using the appropriate jumpers, it is possible that either power supply is not connected properly, or the voltage level is lower that the specified [+12.0V to ≥2Amps].

Notice that the fuse will not protect against one of the EVB regulators being shorted. If this happens, damage Will likely occur to the EVB and / or components.

5. The board is ready to use now.

7 S32K3X8EVB-Q289 - Power supply

The EVB requires an external power supply voltage of between to +12V/≥2A. This allows the EVB to be easily used in a vehicle if required. The 12V input on the EVB is used to supply an S26/SBC (U1). The power management IC controller provides +5.0V, +3.3V and +1.5V, for the different power configurations of VDD_HV_A, VDD_HV_B, V15 and other interfaces.

7.1 S32K3X8EVB-Q289 - Main Power Supply

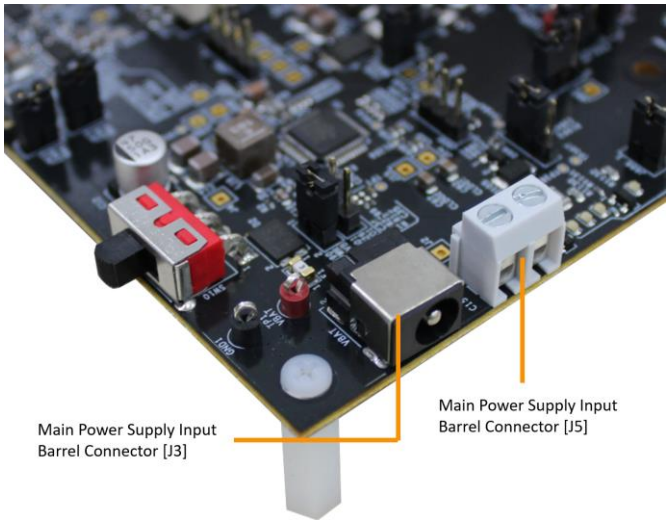
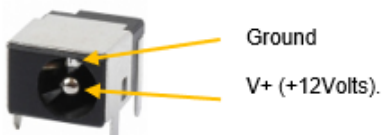
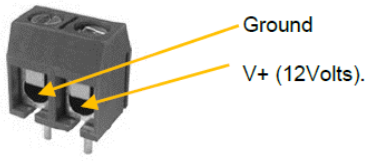


Figure 4. S32K3X8EVB-Q289 – Main power supply input

Table 2. Main power supply connector

Connector	Description
	**2.1mm Barrel Connector – J3** This connector should be used to connect the supplied wall-plug main adapter. Note if a replacement or alternative adapter is used, care must be taken to ensure the 2.1mm plug uses the correct polarization as shown
	**2-Way Screw Type Connector – J5** This can be used to connect a bare wire lead to the EVB, typically from a laboratory power supply. The polarization of the connectors is clearly marked on the EVB. Care must be taken to ensure correct connection.

S32K3X8EVB-Q289 – FS26/Modes Operation

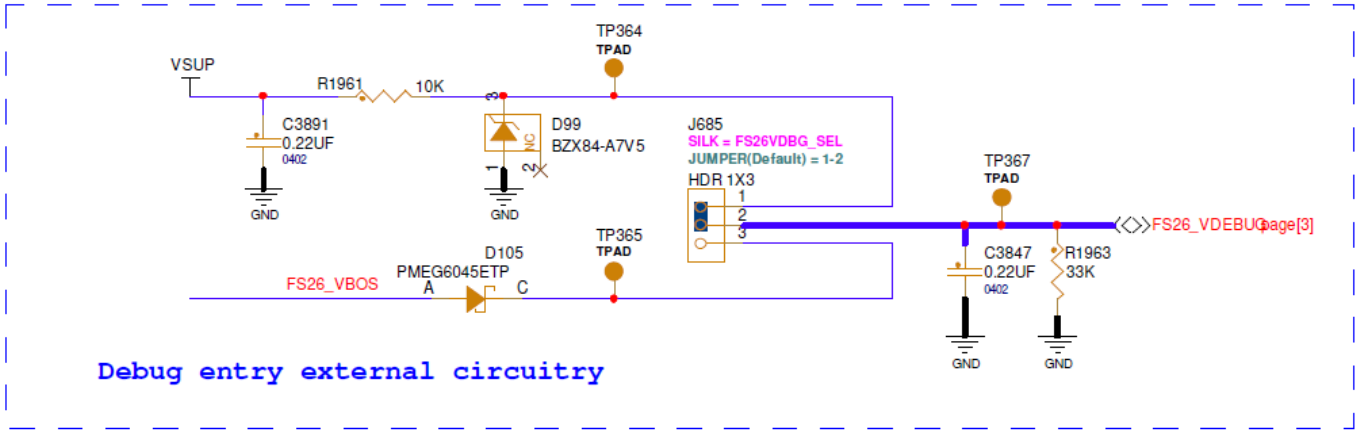


Figure 5. S32K3X8EVB-Q289 – FS26/Modes Operation

Table 3. S32K3X8EVB-Q289 – FS26/Modes Operation

Reference	Jumper Position			Description	Comments
J685	Normal Mode	1-2		The R1963 is selected for the divider voltage, +8.0V is applied on VDEBUG pin to set the FS26/SBC on MCU Flash Mode. In this mode device power up sequence starts with debug mode enabled and can be used during customer production process to flash MCU without need of WD refresh. After ~80ms ,once the SW10 is in ON-position, the VDEBUG pin will be switching to a low voltage (GND) due to the RC delay circuitry and Q18	Default 1-2
	Debug Mode	2-3		+5.0V is applied on VDEBUG pin to set the FS26/SBC on Debug Mode, voltage must be removed from debug pin in order to start power up sequence. In this mode Watchdog refresh is not needed. After ~80ms once the SW10 is in ON-position the VDEBUG pin will be switching to a low voltage (GND) due to the RC delay circuitry and Q18.	
	Disconnected	OPEN		The FS26 will be entering reset every 1 second (approximately),	
All change of jumpers must be done once the EVB is unpowered from J3 and J5 as MANDATORY					

7.2 S32K3X8EVB-Q289 – +5.0 Volts Power Supply

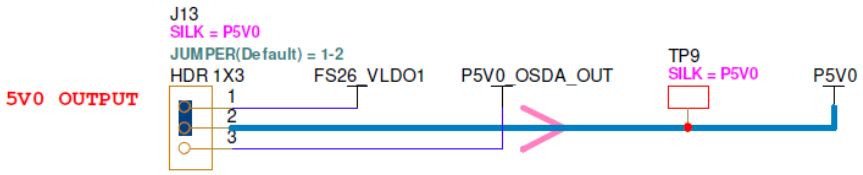
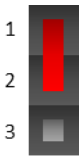
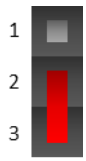
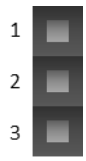


Figure 6. S32K3X8EVB-Q289 – General jumper for the P5V0 (+5.0V) reference

Table 4. S32K3X8EVB-Q289 – +5.0 Volts Power Supply

Reference	Jumper Position		Description	Comments
J13	1-2		The +5.0V output of the FS26/SBC [FS26_VLDO1] is routed to the main P5V0 domain.	Default closed
	2-3		The +5.0V output from the OpenSDA current limiting switch [P5V0_OSDA_OUT] is routed to the main P5V0 domain.	
	OPEN		Power domain is isolated/disconnected from the source.	

7.3 S32K3X8EVB-Q289 – +3.3 Volts Power Supply

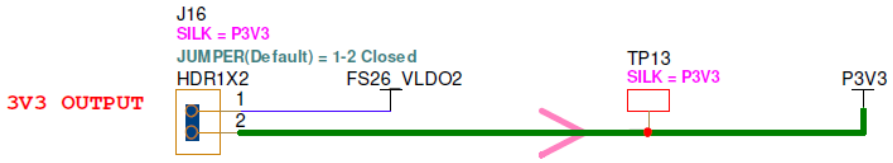
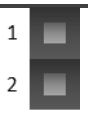


Figure 7. S32K3X8EVB-Q289 – General jumper for the P3V3 (+3.3V) reference

Table 5. S32K3X8EVB-Q289 – +.3.3 Volts Power Supply

Reference	Jumper Position		Description	Comments
J16		1-2	The +3.3V Switching power supply is routed to the main P3V3 domain (+3.3V for all board).	Default closed
		OPEN	The +3.3V output of the FS26/SBC is isolated to the main P3V3 domain (+3.3V for all board).	

7.4 S32K3X8EVB-Q289 – +3.3 Volts Power Supply (Peripherals)

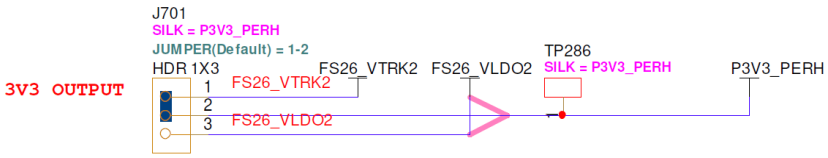
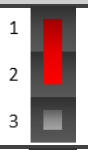
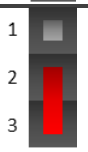


Figure 8. S32K3X8EVB-Q289 – Peripherals jumper for the P3V3 (+3.3V)

Table 6. S32K3X8EVB-Q289 – +.3.3 Volts Power Supply (Peripherals)

Reference	Jumper Position		Description	Comments
J701		1-2	The +3.3V Switching power supply is routed to an extra FS26 3V3 output (+3.3V for additional peripherals).	Default 1-2
		2-3	The +3.3V Switching power supply is routed to the main P3V3 domain (+3.3V for all board and peripherals).	

7.5 S32K3X8EVB-Q289 – VDD_HV_A

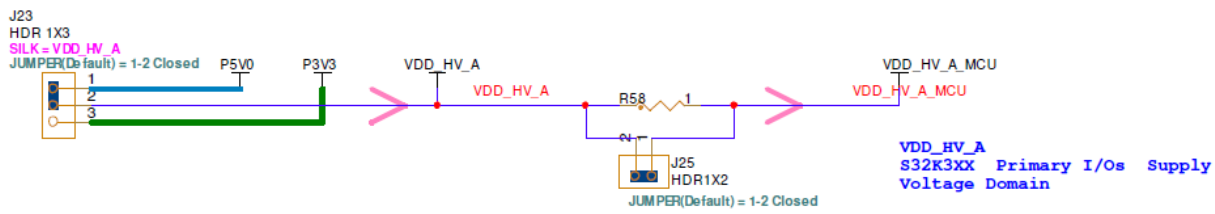
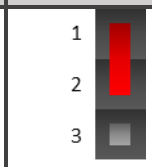
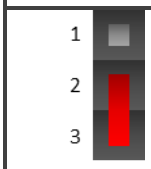
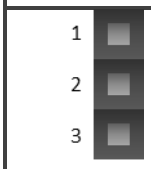
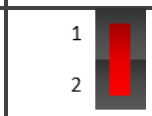
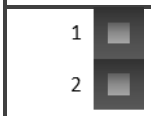


Figure 9. S32K3X8EVB-Q289 – VDD_HV_A power supply

Table 7. S32K3X8EVB-Q289 – VDD_HV_A

Reference	Jumper Position		Description	Comments
J23		1-2	P5V0 (+5.0V from the FS26/SBC) is selected for the VDD_HV_A_MCU reference	Default 1-2
		2-3	P3V3 (+3.3V from the FS26/SBC) is selected for the VDD_HV_A_MCU reference	
		OPEN	VDD_HV_A domain is isolated and unpowered	
J25		1-2	VDD_HV_A is routed to VDD_HV_A_MCU reference. This jumper can be used to measure current in the VDD_HV_A domain	Default closed
		OPEN	VDD_HV_A is routed to VDD_HV_A_MCU reference. This jumper can be used to measure current in the VDD_HV_A domain (Remove R58 to fully disconnect VDD_HV_A domain)	

7.5.1 S32K3X8EVB-Q289 – VDD_HV_B

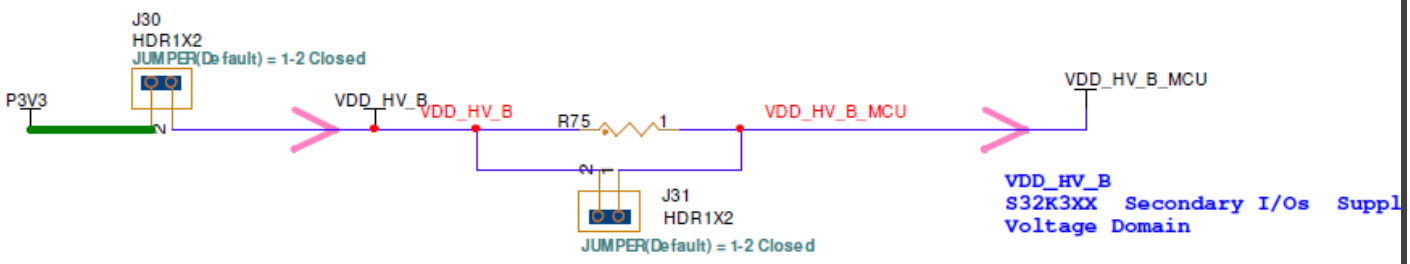
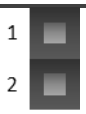


Figure 10. S32K3X8EVB-Q289 – Main power supply

Table 8. S32K3X8EVB-Q289 – VDD_HV_B

Reference	Jumper Position		Description	Comments
J30		1-2	P3V3 (+3.3V from the FS26/SBC) is selected for the VDD_HV_B_MCU reference	Default closed
		OPEN	VDD_HV_B_MCU domain is isolated and unpowered	
J31		1-2	VDD_HV_B is routed to VDD_HV_B_MCU reference. This jumper can be used to measure current in the VDD_HV_B domain	Default closed
		OPEN	VDD_HV_B is routed to VDD_HV_B_MCU reference. This jumper can be used to measure current in the VDD_HV_B domain (Remove R75 to fully disconnect VDD_HV_B domain)	

7.5.2 S32K3X8EVB-Q289 – VREFH

The VREFH reference of the S32K358 MCU is directly routed to the VDD_HV_A_MCU domain.

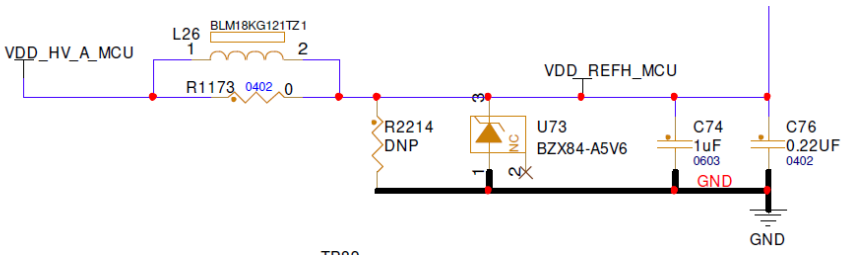


Figure 11. S32K3X8EVB-Q289 – VREFH power supply

7.5.3 S32K3X8EVB-Q289 – V15 Supply Voltage

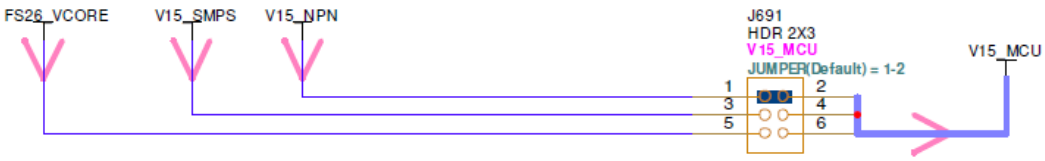
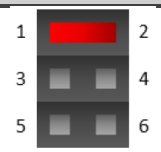
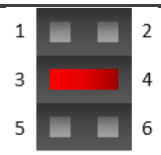
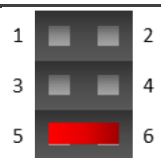
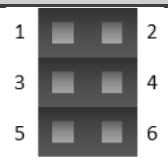


Figure 12. S32K3X8EVB-Q289 – V15 Supply Voltage Selection

Table 9. S32K3X8EVB-Q289 – V15 Domain

Reference	Jumper Position		Description	Comments
J691		1-2	The V15 supply [+1.5V] is taken from de external NPN Ballast Transistor	Default Closed
		3-4	The V15 supply [+1.5V] is taken from the DC/DC Converter (SMPS)	
		5-6	The FS26_VCORE domain [+1.5V] is directly routed to the V15_MCU domain.	

Reference	Jumper Position		Description	Comments
		OPEN	The V15_MCU domain is disconnected and isolated from the local external supplies.	
	CAUTION - 2 or more connections/jumpers in this header selector is **NOT ALLOWED**			

7.5.4 S32K3X8EVB-Q289 – V15 NPN Ballast Transistor

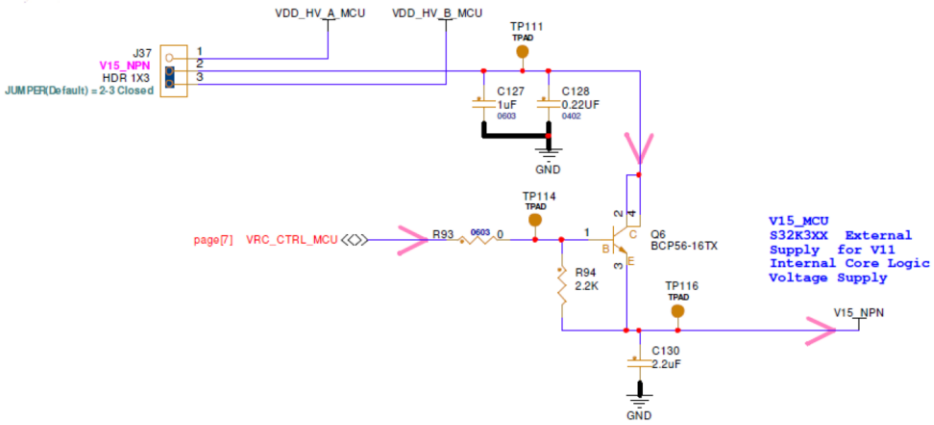


Figure 13. S32K3X8EVB-Q289 – V15 NPN Ballast power supply

Table 10. S32K3X8EVB-Q289 – V15 Ballast Domain

Reference	Jumper Position		Description	Comments
J37		1-2	The VDD_HV_A domain is routed to the collector terminal in order to supply the NPN external Ballast transistor for the V15_NPN domain.	
		2-3	The VDD_HV_B domain is routed to the collector terminal in order to supply the NPN external Ballast transistor for the V15_NPN domain.	Default 2-3
		OPEN	The VDD_HV_A and VDD_HV_B domains are isolated to supply the NPN external Ballast transistor for V15	

7.5.5 S32K3X8EVB-Q289 – V15 DC/DC Converter (SMPS)

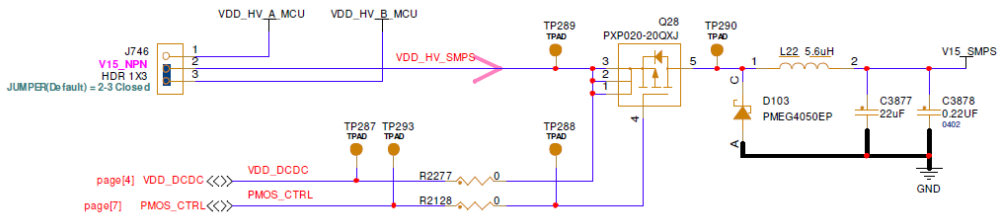


Figure 14. S32K3X8EVB-Q289 – V15 DC/DC Converter power supply

Table 11. S32K3X8EVB-Q289 – DC/DC Domain

Reference	Jumper Position		Description	Comments
J746		1-2	The VDD_HV_A domain is routed to the source terminal in order to supply the DC/DC Converter for the V15_SMPS domain.	
		2-3	The VDD_HV_B domain is routed to the source terminal in order to supply the DC/DC Converter for the V15_SMPS domain.	Default 2-3
		OPEN	The VDD_HV_A and VDD_HV_B domains are isolated to supply the DC/DC Converter for V15	

7.6 S32K3X8EVB-Q289 – V11

V11 is the core/logic supply of the MCU. In the default case of the board the S32K358 it is driven by a fully integrated low-dropout linear voltage regulator but if the customer replace the MCU with the S32K388, V11 must be supplied externally, nevertheless the S32K3X8EVB-Q289 integrates a great versatility that includes the two ways to support both MCUs.

7.6.1 V11 – S32K358 MCU

As default the S32K3X8EVB-Q289 includes a S32K358 MCU which only need the corresponded decoupling and bulk capacitors to work as expected due this MCU integrates a full low-dropout linear voltage regulator that reduce the voltage from +1.5V in V15 to +1.1V.

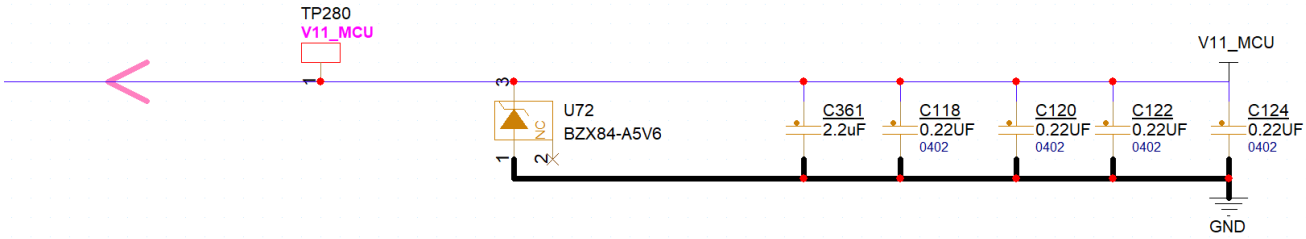


Figure 15. S32K3X8EVB-Q289 – V11 using S32K388

7.6.2 V11 – S32K388 MCU

In order to have a high versatility among our MCUs, the EVB can be used with both the MCU S32K358 and the S32K388 due to pinout compatibility. However, the S32K388 has an important feature that makes this MCU different from the others in the family, how to supply V11 for the CORE. The EVB is ready to support both MCUs, so if the user decides to replace the S32K358 with the S32K388, the user must fill the corresponding circuit as shown in the figure below.

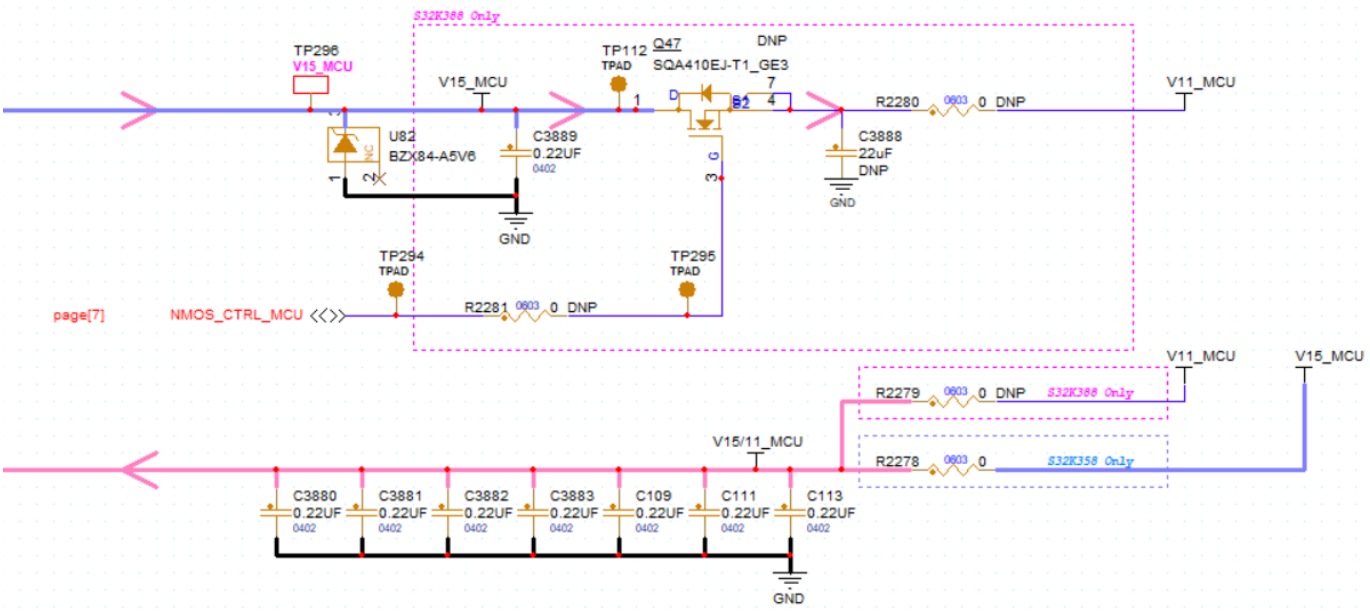


Figure 16. S32K3X8EVB-Q289 – V11 using S32K388

The Figure 16 shows the circuitry that regulates the voltage from V15 (+1.5 V) to V11 (+1.1 V) using a N-Channel MOSFET, which is controlled by NMOS_CTRL pin of the MCU.

Note: The MOSFET shown in the figure works for the application, nevertheless at high temperatures the MOSFET could fail due this component was selected to validate the functionality so this part number shouldn't have applied in real applications due the junction temperature of the NMOS channel.

The following table shows the components that should be placed in case of replace the S32K358 with the S32K388.

Table 12. S32K3X8EVB-Q289 – V11 populated components

Components	Value	S32K358	S32K388
R2279	0 Ω	DNP	POPULATED
R2278	0 Ω	POPULATED	DNP
R2281	0 Ω	DNP	POPULATED
R2280	0 Ω	DNP	POPULATED
C3888	22uF	DNP	POPULATED
Q47	SQA410EJ-T1_GE3	DNP	POPULATED

8 S32K3X8EVB-Q289 - Programming and Debug Interface

8.1 RESET Switch and LED indicator

The RESET switch [SW2] provides an input signal for manual application RESET. The S32K3 MCU will drive the RESET signal to reset the EVB board peripherals. The RESET LED indicator [D22] will be ON for the duration of the RESET signal. This operation indicates the S32K358 MCU is in the RESET state.

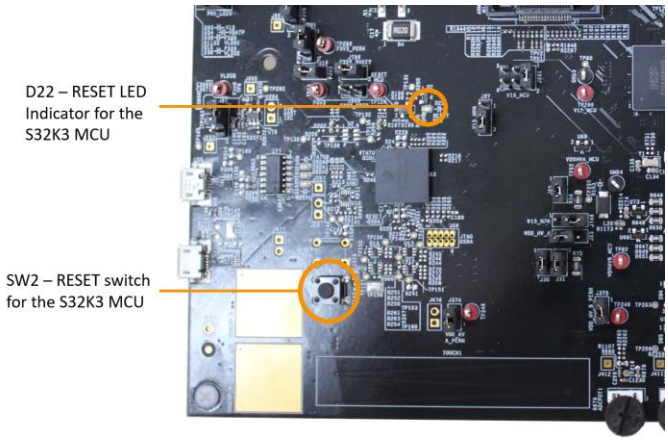


Figure 17. S32K3X8EVB-Q289 – RESET Switch

8.2 On-board S32K3 Debugger

The S32K3X8EVB-Q289 incorporates an On-Board Debugger as well as embedded JTAG connectors. It bridges serial and debug communications between an USB host and an embedded target processor.

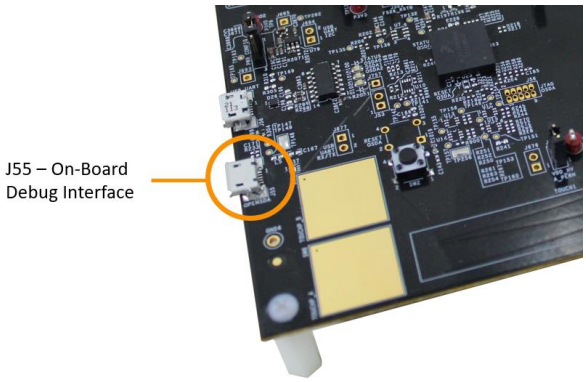


Figure 18. S32K3X8EVB-Q289 – On-board S32K3 Debugger

Table 13. Programming and Debug Connectors

<table>
<tr><th colspan="2">Connector</th><th>Reference/ Component</th><th>Description</th></tr>
<tr><td>20-Pin Cortex Debug + ETM Connector</td><td>  </td><td>J50</td><td>This small 20-pin (0.05") connector provides access to SWD, SWV, JTAG, and ETM (4-bit) signals available on a Cortex-M3/M4/M7 device.
A 20-pin header (Samtec FTSH-110-01) is specified with dimensions:
0.50" x 0.188" (12.70 mm x 4.78 mm).

NOTE - JTAG – TRACE Signals
Due to the MCU ports used on the trace signals also are shared with other interfaces, it is important to isolate these signals/interfaces for the J4-Cortex Debug D ETM connector.
<table>
<tr><th>SIGNAL Name</th><th>MCU Port Name</th><th>Signal Resistor</th><th>COMMENT</th></tr>
<tr><td>TRACE_CLK</td><td>PTG6</td><td>R160</td><td></td></tr>
<tr><td>TRACE_D0</td><td>PTG7</td><td>R163</td><td></td></tr>
<tr><td>TRACE_D1</td><td>PTG15</td><td>R165</td><td></td></tr>
<tr><td>TRACE_D2</td><td>PTG16</td><td>R167</td><td></td></tr>
<tr><td>TRACE_D3</td><td>PTF31</td><td>R169</td><td></td></tr>
</table></td></tr>
<tr><td>10-Pin Cortex Debug Connector</td><td>  </td><td>J52</td><td>The Cortex Debug Connector provides support for Serial Wire and JTAG interface modes in a very small, low cost 10-pin (0.05") connector. This new style connector provides access to all SWD, SWV, and JTAG signals available on a Cortex-Mx device.
A 10-pin header (Samtec FTSH-105-01) is specified with these dimensions:
0.25" x 0.188" (6.35 mm x 4.78 mm).</td></tr>
</table>

38-Pin ARM ETM Mictor Connector		**P1**	The Mictor (Matched Impedance Connector) has been the standard way to connect a trace probe to an ARM target. It supports up to 32-bit ETM trace and is really intended for use with very high-speed ARM processors such as Cortex-R4 and Cortex-A9. Cortex-M7 supports 16-bit data trace using the Mictor connector. This is only available with DS-5 using a DSTREAM debug and trace unit.
20-Pin ARM Standard JTAG Connector		**J635**	The ARM standard JTAG connector has been used for many years in systems with ARM processors. It supports the JTAG interface for accessing ARM7 and ARM9 based devices. For Cortex-Mx devices, it supports Serial Wire and JTAG interfaces for accessing all SWD, SWV, and JTAG signals available on a Cortex-Mx device. The header (e.g. a Samtec: TST-110-01-L-D) is a 20-Pin, 0.10" (2.54 mm) pitch connector with these dimensions: 1.3" x 0.365" (33 mm x 9.27mm).
All TRACE signals are DISABLED as default configuration. In order to enable the TRACE interface, the MCU signals routed to the **QSPIA**(R451,R189,R447,R512) and **Ethernet interface**(R2274, R2283,R2284,R2285,R2286) must be disabled and isolated, but the **TRACE** resistors (R192,RR452,R190,R435,R511)must be populated.			

9 S32K3X8EVB-Q289 - USB to I2C/UART Interface

The EVB incorporates an interface providing a serial connectivity via a direct USB connection between the PC and the EVB. The circuit contains a Microchip MCP2221A USB to I2C/UART interface which should automatically install the drivers on your PC. For more information on the USB drivers and general fault finding, consult Microchip's MCP2221A website.

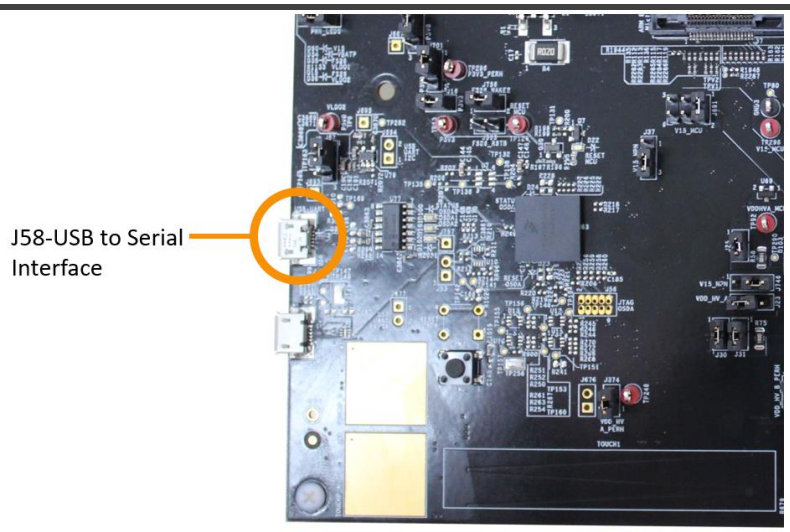


Figure 19. S32K3X8EVB-Q289 – USB to I2C/UART Interface

The PTC27 MCU port (LPUART13_RX) and PTC26 MCU port (LPUART13_TX) signals are routed to the MCP2221A transceiver via zero ohms resistors allowing the transceiver to be isolated from the MCU pin if desired. The default configuration is with the zero ohms resistors, routing the TX and RX signals from the MCU to the MCP2221A transceiver.
The PTC6 MCU port (LPI2C1_SDA) and PTC7 MCU port (LPI2C1_SCL) signals are routed to the MCP2221A transceiver via zero ohms resistors allowing the transceiver to be isolated from the MCU pin if desired. The default configuration is with the zero ohms resistors, routing the TX and RX signals from the MCU to the MCP2221A transceiver.

Table 13. USB to serial interface – Control Jumpers

Signal /Module		MCU Port	Reference	Description	Comment
1	LPUART13_RX	PTC27	R303	LPUART13_RX signal is routed to MCP2221A interface	Default Configuration
	LPUART13_TX	PTC26	R309	LPUART13_TX signal is routed to MCP2221A interface	Default Configuration
2	LPUART6_TX	PTA16	R308	LPUART6_RX signal is routed to MCP2221A interface	
	LPUART6_RX	PTA15	R302	LPUART6_TX signal is routed to MCP2221A interface	

1. If the user wants to use or change to LPUART6 RX/TX, then:
   - R303 and R309 must be removed
   - R308-0402-0ohms and R302-0402-0ohms must be populated
2. If the user wants to use other LPUARTx RX/TX module of the MCU, the user can have access to the USB to serial interface by the J677 header. For this use case R303, R309, R308 and R302 must be removed.

Signal /Module	MCU Port	Reference	Description	Comment
LPI2C1_SDA	PTC6	R2060	LPI2C1_SDA signal is routed to MCP2221A interface	Default Configuration
LPI2C1_SCL	PTC7	R2061	LPI2C1_SCL signal is routed to MCP2221A interface	Default Configuration

1. If the user wants to use other LPI2Cx SDA/SCL module of the MCU, the user can have access to the USB to serial interface by the J694 header. For this use case R2060 and R2061 must be removed.
   - For a LPI2Cx SDA/SCL module under the domain voltage VDD_HV_A, the R2067 must be populated R2066 must be removed.
   - For a LPI2Cx SDA/SCL module under the domain voltage VDD_HV_B, the R2066 must be populated R2067 must be removed.

The USB to serial device in the EVB has two options to configure.

- USB Bus powered Configuration.
- USB Self powered Configuration.

USB Bus Powered Configuration.

The USB Bus Powered device gets its power from the USB bus. Basic rules for USB Bus power devices are as follows:

- On plug-in, the device must draw no more than 100mA
- On USB Suspend the device must draw no more than 500µA.
- A High-Power USB Bus Powered Device (one that draws more than 100mA).
- A device that consumes more than 100mA cannot be plugged into a USB Bus Powered Hub.
- No device can draw more than 500mA from the USB Bus.

USB Self Powered Configuration (Default Configuration).

A USB Self Powered configuration gets its power from its own POWER SUPPLY and does not draw current from the USB bus. The basic rules for USB Self power devices are as follows.

- A Self-Powered device should not force current down the USB bus when the USB Host or Hub Controller is powered down.

- A Self Powered Device can take as much current as it likes during normal operation and USB suspend as it has its own POWER SUPPLY.
- A Self Powered Device can be used with any USB Host and both Bus and Self Powered USB Hubs.

10 S32K3X8EVB-Q289 - LIN Interface

The EVB incorporates two LIN interfaces connected to the S32K358 MCU. Using an NXP LIN transceiver the TJA1021T/20/C, supporting both master and slave mode (jumper selectable). The output from the LIN transceiver is connected to J675.

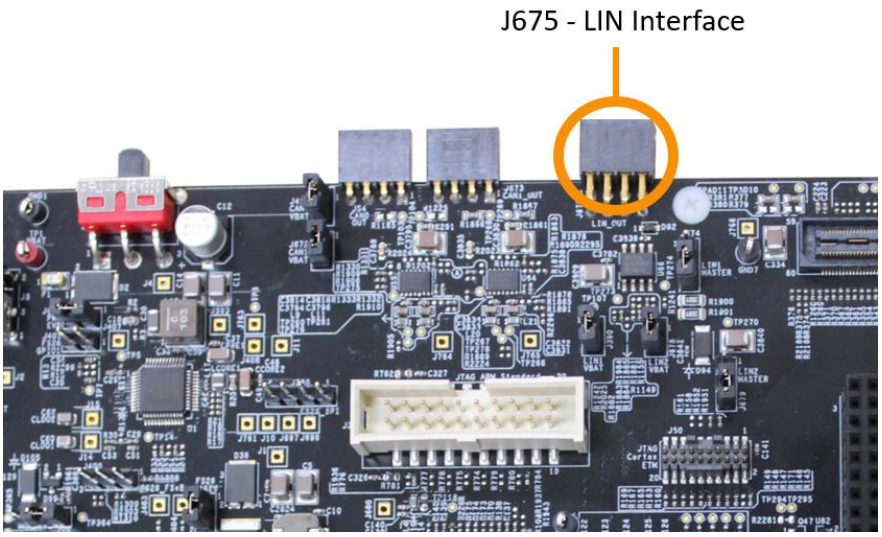
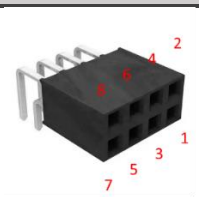


Figure 20. S32K3X8EVB-Q289 – LIN Interface

Table 14. LIN Connector

Connector	Reference	Pin Number	Signal/Connection
	J23	1	GND
		2	GND
		3	NC
		4	NC
		5	VBAT
		6	VBAT
		7	LIN2_OUT
		8	LIN1_OUT

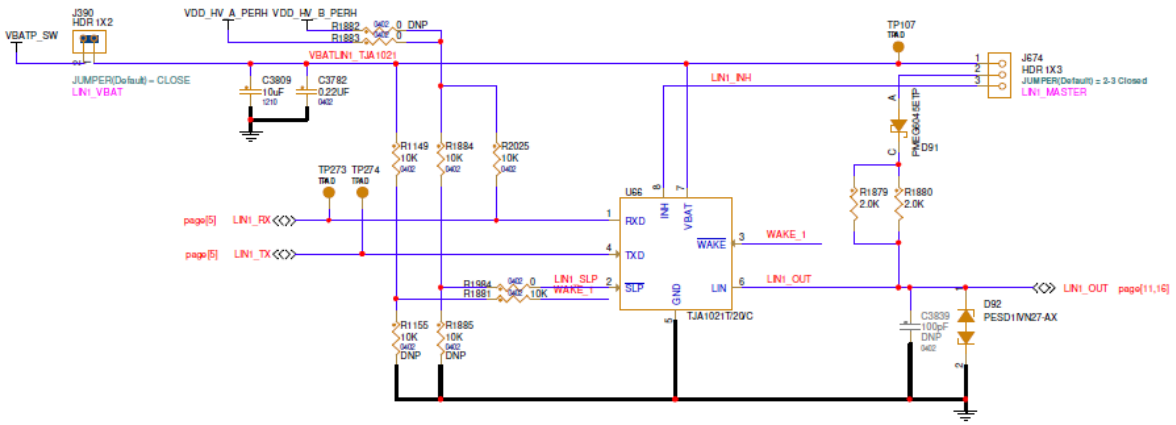


Figure 21. S32K3X8EVB-Q289 – LIN Physical Layer1 TJA1021HG: Quad LIN 2.2A/SAE J2602 transceiver

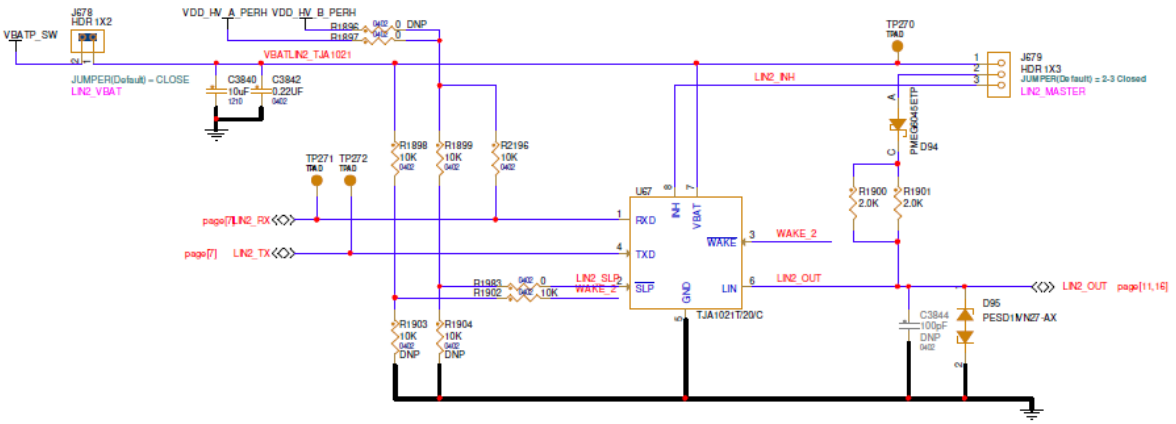


Figure 22. S32K3X8EVB-Q289 – LIN Physical Layer2 TJA1021HG: Quad LIN 2.2A/SAE J2602 transceiver

Table 15. LIN Interface – MCU Connections

LIN Interface	Signal Name	MCU Port	Comment/Description
TJA1021 /LIN1	LIN1_RX	PTB9	LPUART9_RX is routed to LIN PHY1
	LIN1_TX	PTB10	LPUART9_TX is routed to LIN PHY1
TJA1021 /LIN2	LIN2_RX	PTE5	LPUART12_RX is routed to LIN PHY2
	LIN2_TX	PTE4	LPUART12_TX is routed to LIN PHY2

11 S32K3X8EVB-Q289 - CAN Interface

The EVB incorporates a CAN interface connected to the S32K358 MCU. Using an NXP CAN transceiver the TJA1153. The output from the CAN transceiver is connected to J54.

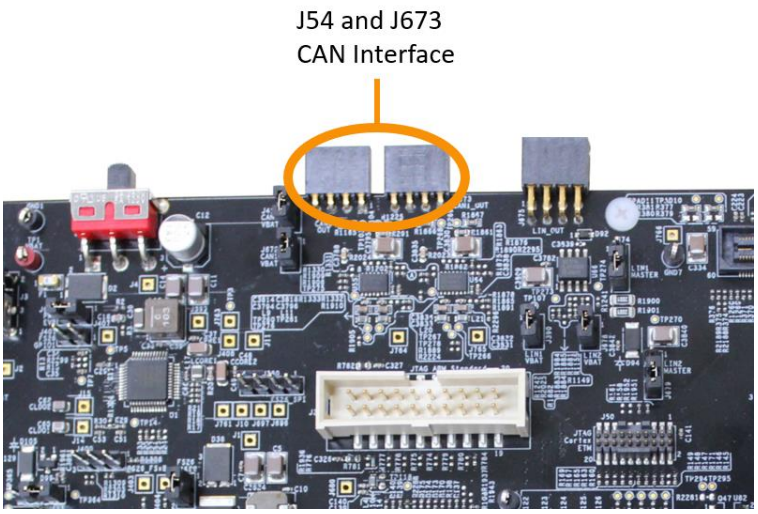


Figure 23. S32K3X8EVB-Q289 – CAN Interface

Table 16. CAN Interface - Connectors

Connector	Reference	Circuit/ Interface	Pin Number	Signal/Connection
	J54	CAN0	1	CANH0
			2	CANL0
			3	GND
			4	NC
	J673	CAN1	1	CANH1
			2	CANL1
			3	GND
			4	NC

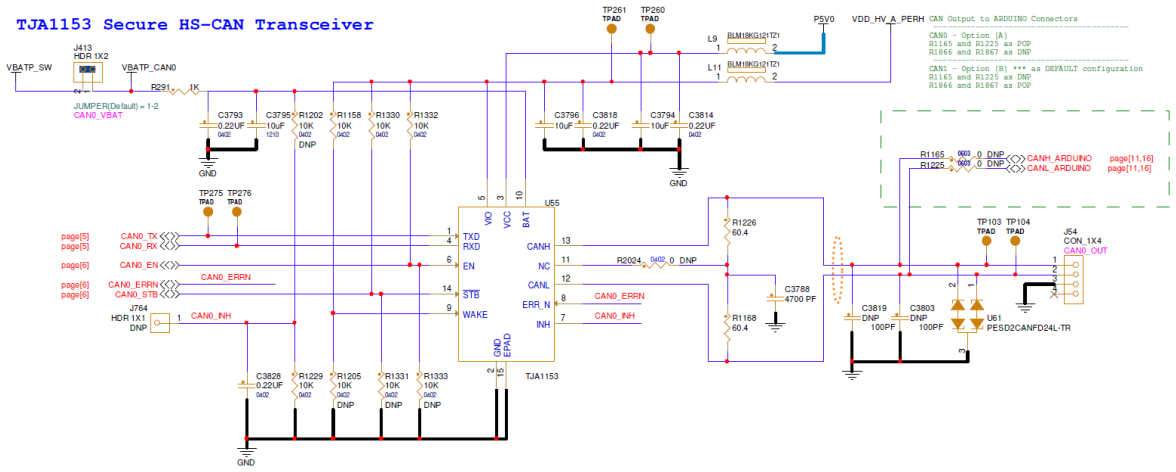


Figure 24. S32K3X8EVB-Q289 – CAN Physical Layer0 - TJA1153 Secure HS-CAN Transceiver

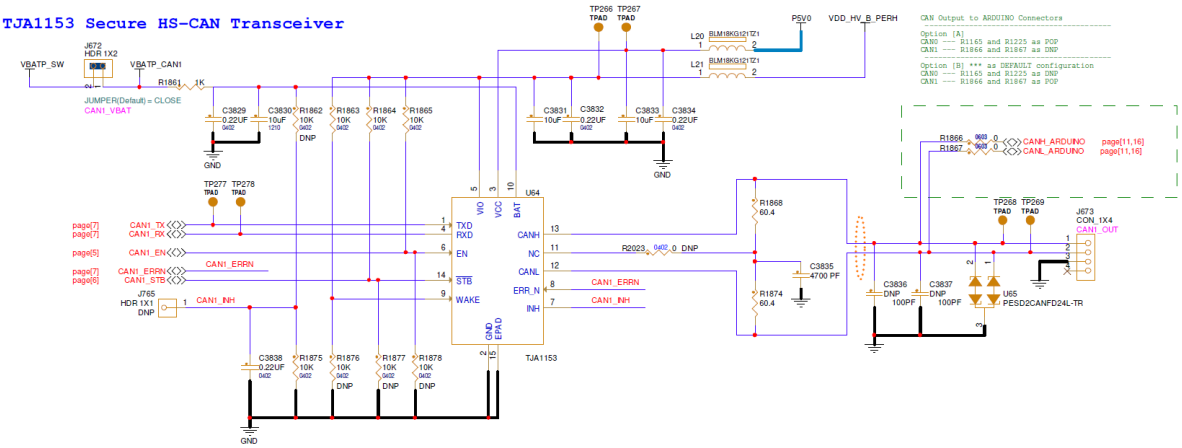


Figure 25. S32K3X8EVB-Q289 – CAN Physical Layer1 - TJA1153 Secure HS-CAN Transceiver

Table 17. CAN Interface – MCU Connections

CAN Interface	Signal Name	MCU Port	Comment/Description
TJA1153 /CAN0	CAN0_RX	PTA6	[CAN0_RX Module] is routed to CAN PHY0
	CAN0_TX	PTA7	[CAN0_TX Module] is routed to CAN PHY0
	CAN0_ERRN	PTC23	PTC23 is routed to CAN PHY 0 as CAN0_ERRN
	CAN0_EN	PTC21	PTC21 is routed to CAN PHY 0 as CAN0_EN
	CAN0_STB	PTC20	PTC20 is routed to CAN PHY 0 as CAN0_STB
TJA1153 /CAN1	CAN1_RX	PTE14	[CAN4_RX Module] is routed to CAN PHY1
	CAN1_TX	PTE3	[CAN4_TX Module] is routed to CAN PHY1
	CAN1_ERRN	PTE8	PTE8 is routed to CAN PHY 1 as CAN1_ERRN
	CAN1_EN	PTB20	PTB20 is routed to CAN PHY 1 as CAN1_EN
	CAN1_STB	PTD13	PTD13 is routed to CAN PHY 1 as CAN1_STB

12 S32K3X8EVB-Q289 – Serial Audio Interface

The S32K3x8EVB-Q289 incorporates a Serial Audio Interface (SAI) connected to a SGTL5000. This low power stereo codec with headphone amp has tree audio jack connectors connected to J370, J371, J372, a microphone (P4) and an audio connector (P3).

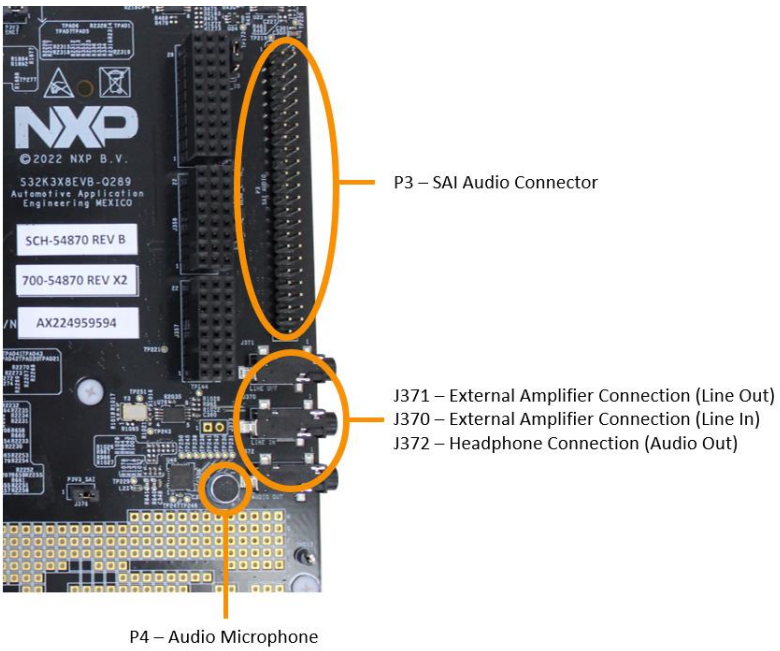


Figure 26. S32K3X8EVB-Q289 – Serial Audio Interface (SAI)

Table 18. Serial Audio Interface - Connectors

Connector	Reference	Circuit/ Interface	Pin Number	Signal/Connection
	J371	LINE OUT	1	GND
			2	LINEOUT_L
			3	LINEOUT_R
			4	NC
	J370	LINE IN	1	GND
			2	LINEIN_L
			3	LINEIN_R
			4	NC
	J372	AUDIO OUT	1	HP_VGND
			2	HP_L
			3	HP_R
			4	NC
	P3	SAIAUDIO	1	P3V3
			3	PTD5 – SAI0_DATA3

			5	PTD6 – SAI0_DATA2
			7	PTB4 – SAI0_DATA1
			9	PTB2 – SAI0_DATA0
			11	PTC12 – SAI0_BCLK
			13	PTC13 – SAI0_SYNC
			15	PTE9 – SAI0_MCLK
			17	PTA26
			19	PTB20 – I2C_SCL0
			21	PTB21 – I2C_SDA0
			23	PTD13 – SAI1_DATA0
			25	PTE8 – SAI1_BCLK
			27	PTA28
			29	PTD15 – SAI1_SYNC
			31	PTD14 – SAI1_MCLK
			33	PTE3 – I2C_SCL1
			35	PTE14 – I2C_SDA1
			37	PTE12
			39	PTB5
			41	PTB19
			43	PTA27
			45	PTB27
			47	PTA31 – GPIO Control
			49	P5V0

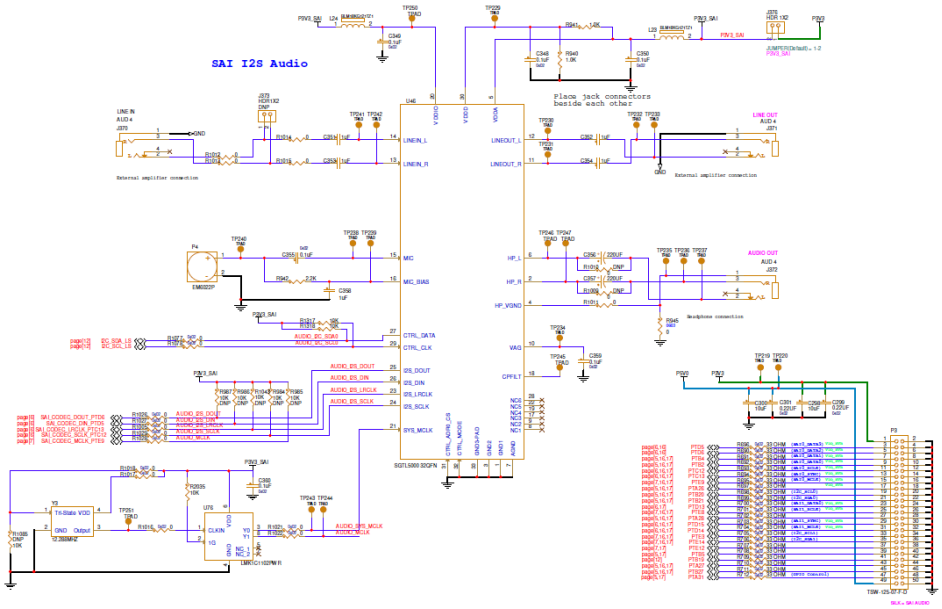


Figure 27. S32K3X8EVB-Q289 – SGTL5000 Low Power Codec

Table 19. SAI Interface – MCU Connections

MODULE /FUNCTION	Signal Name	MCU Port	Comment/Description
SGTL5000 SAI	SAI_CODEC_DOUT_PTD6	PTD6	Audio I2S data out
	SAI_CODEC_DIN_PTD5	PTD5	Audio I2S data in
	SAI_CODEC_LRCLK_PTC13	PTC13	Audio I2S frame clock
	SAI_CODEC_SCLK_PTC12	PTC12	Audio I2S bit clock
	SAI_CODEC_MCLK_PTE9	PTE9	Audio master clock
SGTL5000 I2C	I2C_SDA_LS	PTC6	I2C serial Data
	I2C_SCL_LS	PTC7	I2C Serial Clock

13 S32K3X8EVB-Q289 - Ethernet Interface

The S32K3x8EVB-Q289 incorporates a complete Ethernet interface providing MII, RMII or RGMII connectivity trough a SABRE connector. The default configuration is RGMII, nevertheless this configuration can be modified through populate or do not populate the resistors explained in the **chapter Rework for RMII**

Ethernet Connector – The EVB includes a high-speed connector which is compatible with the boards described below, with which the EVB becomes a complete interface fully ready to communicate and adapt to the different cards developed for communication over ethernet

- ADTJA1101-RMII
- TJA1103SDB
- SJA1105Q-EVB
- SJA1110-EVM

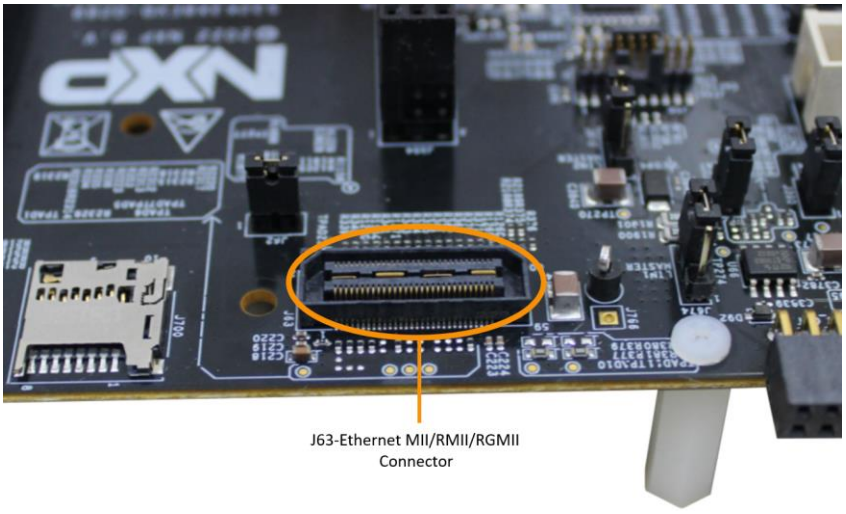


Figure 28. S32K3X8EVB-Q289 – 10/100 T-Base Ethernet Connector

13.1 Ethernet MII/RMII/RGMII Connector – Pinout

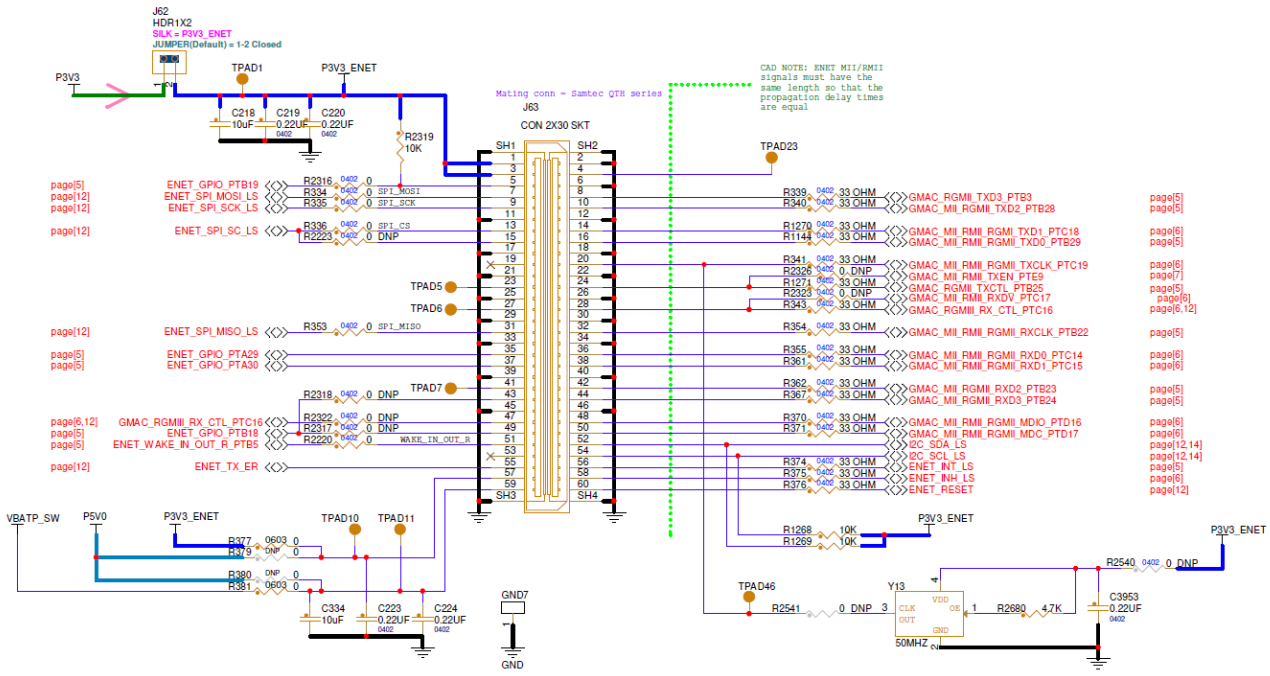


Figure 29. S32K3X8EVB-Q289 – Ethernet MII/RMII/RGMII Connector

Table 20. Ethernet Interface – MCU Connections

MODULE /FUNCTION	SIGNAL	MCU PORT	Comment/Description
MII/RMII/RGMII	GMAC_MII_RMII_RGMII_RXD0_PTC14	PTC14	
	GMAC_MII_RMII_RGMII_RXD1_PTC15	PTC15	
	GMAC_MII_RGMII_RXD2_PTB23	PTB23	
	GMAC_MII_RGMII_RXD3_PTB24	PTB24	
	GMAC_MII_RMII_RGMII_RXCLK_PTB22	PTB22	
	GMAC_RGMII_RX_CTL_PTC16	PTC16	
	GMAC_MII_RMII_RXDV_PTC17	PTC17	
	GMAC_MII_RMII_RGMII_TXD0_PTB29	PTB29	
	GMAC_MII_RMII_RGMI_TXD1_PTC18	PTC18	
	GMAC_MII_RGMII_TXD2_PTB28	PTB28	
	GMAC_RGMII_TXD3_PTB3	PTB3	
	GMAC_MII_RMII_RGMII_TXCLK_PTC19	PTC19	
	GMAC_MII_RMII_TXEN_PTE9	PTE9	
	GMAC_RGMII_TXCTL_PTB25	PTB25	
	GMAC_MII_RMII_RGMII_MDIO_PTD16	PTD16	
	GMAC_MII_RMII_RGMII_MDC_PTD17	PTD17	

GPIOs	ENET_INT_LS	PTB27	
	ENET_INH_LS	PTD14	
	ENET_RESET	PTE21	
LPSPIx	ENET_SPI_MISO_LS	PTC9	
	ENET_SPI_MOSI_LS	PTB1	
	ENET_SPI_SCK_LS	PTC8	
	ENET_SPI_SC_LS	PTB8	
I2C	I2C_SDA_LS	PTC6	
	I2C_SCL_LS	PTC7	
PWR	VBATP_SW	+12V	P5V0 [+5.0V] can be routed to the Ethernet connector as optional power supply reference instead the VBATP_SW reference. For this option, R380/0-Ohms must be placed and R381 must be removed.
	P3V3_ENET	+3.3V	P5V0 [+5.0V] can be routed to the Ethernet connector as optional power supply reference instead the P3V3_ENET reference. For this option, R380/0-Ohms must be placed and R381 must be removed.

For more information about the different versions of the SABRE connector please check the Errata's chapter.

13.2 Rework for RMII

In order to provide greater versatility to the board and take full advantage of the capabilities of the S32K358 the ethernet configuration using the SABRE connector can be changed by modifying the resistors as shown in the Table 21.

Table 21. Rework for RMII

Signal	Resistor	Value	Package	RGMII (Default)	RMII	MCU Port
TX_EN	R2326	33 Ω	0402	DNP	Populate	PTE9
	R2327	0 Ω		DNP	Populate	PTE9
	R1271	33 Ω		Populate	DNP	PTB25
RX_DV	R2323	33 Ω		DNP	Populate	PTC17
	R2324	0 Ω		DNP	Populate	PTC17
	R343	33 Ω		Populate	DNP	PTC16
RX_ER	R2322	33 Ω		DNP	Populate	PTC16
QSPI	R2325	0 Ω		Populate	DNP	PTC17
SAI	R2212	0 Ω		Populate	DNP	PTE9
	R2213	0 Ω		Populate	DNP	PTE9

In order to identify the resistors in the board consult the S32K3X8EVB-Q289_HWPack_C_Layout.pdf document in the S32K3X8EVB-Q289HWPack_C2

14 S32K3X8EVB-Q289 - QSPI-A Interface

The S32K3x8EVB-Q289 EVB incorporates a 26KL512SDABHV030 64MB Serial NOR Flash memory, which is connected to the QSPI-A Module of the S32K358 MCU.

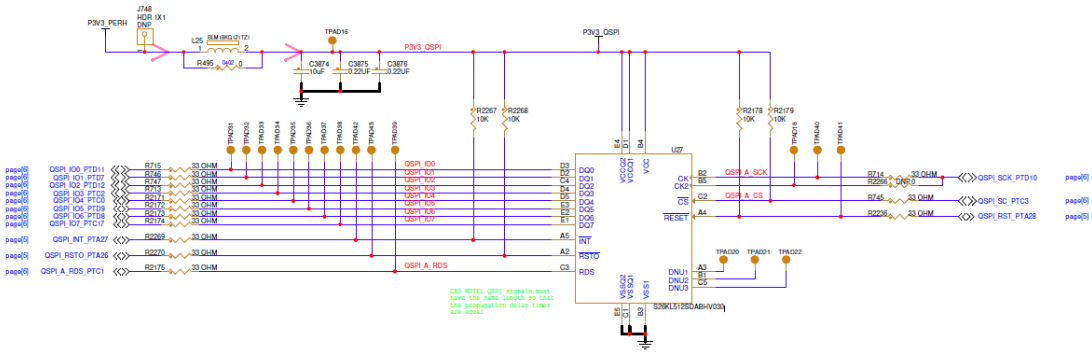


Figure 30. S32K3X8EVB-Q289 – QSPI-A Memory Interface

Table 22. QSPI-A – Signals configuration

Module /Function	Signal	MCU PORT	DESCRIPTION /COMMENT
QSPIA	QSPI_IO0_PTD11	PTD11	Enabled as default.
	QSPI_IO1_PTD7	PTD7	
	QSPI_IO2_PTD12	PTD12	
	QSPI_IO3_PTC2	PTC2	
	QSPI_IO4_PTC0	PTC0	
	QSPI_IO5_PTD9	PTD9	
	QSPI_IO6_PTD8	PTD8	
	QSPI_IO7_PTD17	PTD17	
	QSPI_INT_PTA27	PTA27	
	QSPI_RSTO_PTA26	PTA26	
	QSPI_A_RDS_PTC1	PTC1	
	QSPI_SCK_PTD10	PTD10	
	QSPI_SC_PTC3	PTC3	
	QSPI_RST_PTA28	PTA28	

15 S32K3X8EVB-Q289 – SD Interface

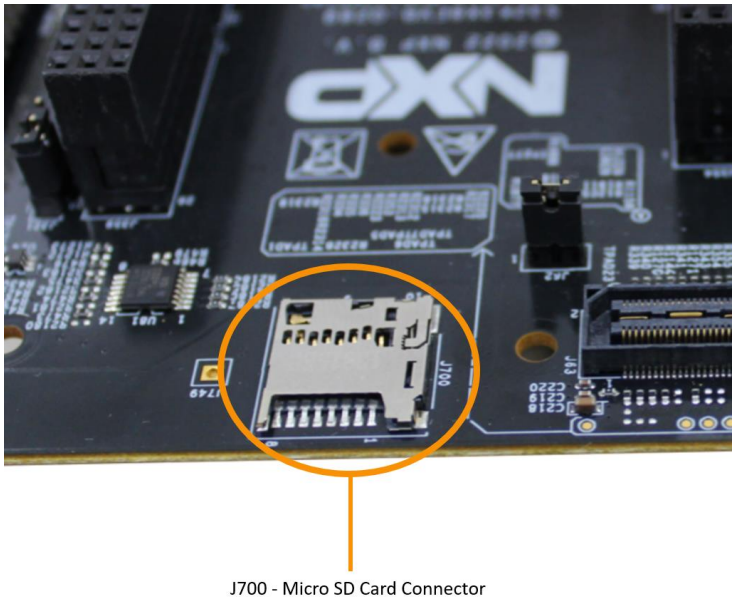


Figure 31. S32K3X8EVB-Q289 – µSD Card Connector

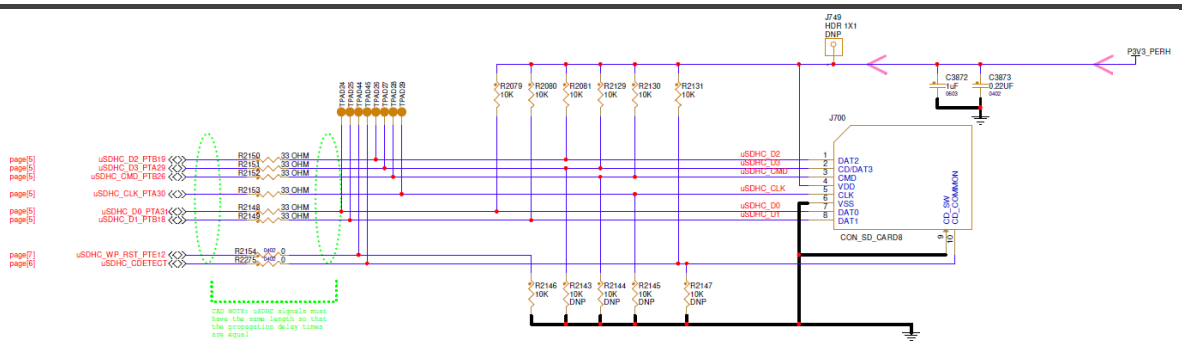


Figure 32. S32K3X8EVB-Q289 – µSD Card Interface

Table 23. uSDHC – Signals configuration

Module /Function	Signal	MCU PORT	DESCRIPTION /COMMENT
uSDHC	uSDHC_D0	PTA31	Enabled as default.
	uSDHC_D1	PTB18	
	uSDHC_D2	PTB19	
	uSDHC_D3	PTA29	
	uSDHC_CMD	PTB26	
	uSDHC_CLK	PTA30	
	uSDHC_WP_RST	PTE12	

16 S32K3X8EVB-Q289 - User Peripherals

16.1 GPIO Matrix

A subset of available GPIO pins (available pins being those not already routed to the Ethernet connector and the QSPIA-Memory Interface) are available at the GPIO matrix as detailed below. The matrix provides an easy to follow, intuitive, space-saving grid of 0.1" header through-hole pads. Users can solder wires, fit headers, or simply insert a scope probe into the respective pad.

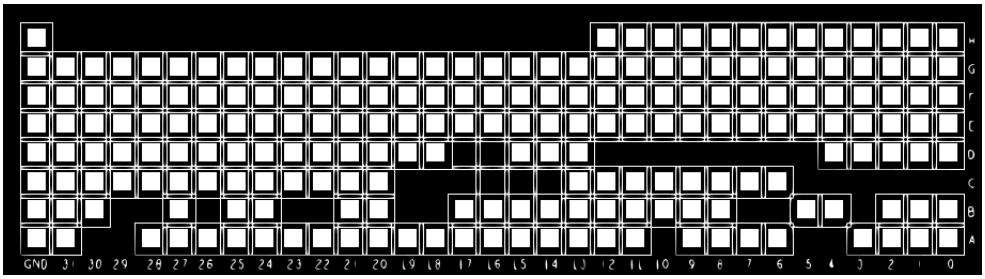


Figure 31. S32K3X8EVB-Q289 – GPIO Matrix

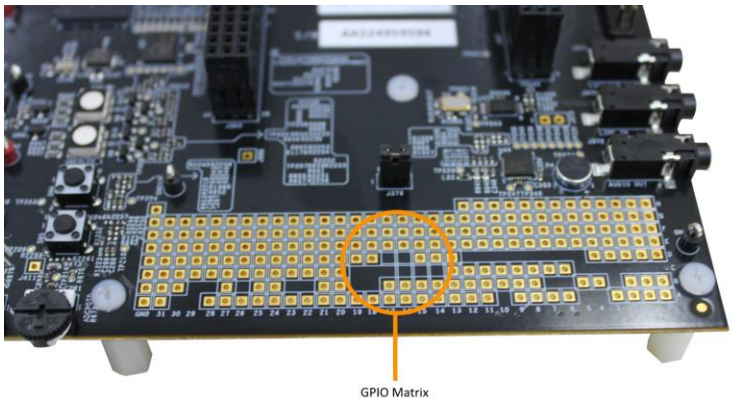


Figure 33. S32K3X8EVB-Q289 – GPIO Matrix

16.2 User RGB LED Indicators

There are 2 active high user RGB LED's, connected through NPN transistors to the MCU ports. The USER LED is connected as follows:

Table 24. User LED Indicators

Reference	Signal Name	MCU Port Default	Color	Comment
D32	RGBLED0_RED	PTG29	Red	Active High
	RGBLED0_GREEN	PTG30	Green	Active High
	RGBLED0_BLUE	PTG31	Blue	Active High
D33	RGBLED1_RED	PTF21	Red	Active High
	RGBLED1_GREEN	PTF22	Green	Active High
	RGBLED1_BLUE	PTF23	Blue	Active High

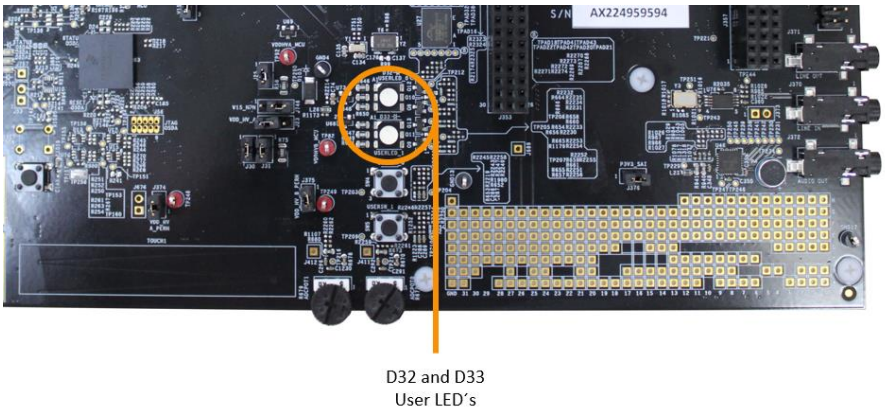


Figure 34. S32K3X8EVB-Q289 – User RGB LED Indicators

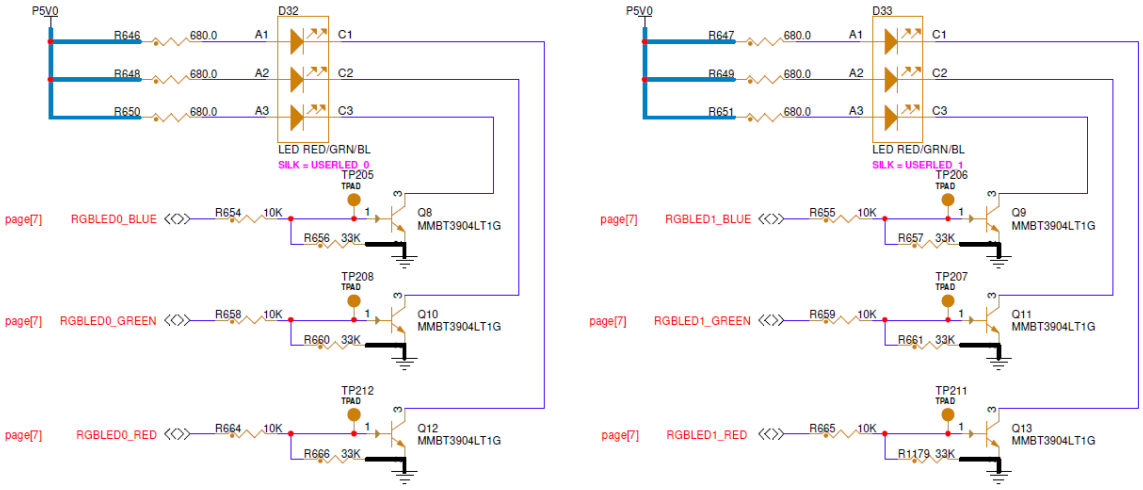


Figure 35. S32K3X8EVB-Q289 – User LED indicators

16.3 User Push Buttons

There are 2 push-buttons active high (pulled low, driven to VDD_HV_B_PERH), the push button switches (SW4 and SW5) connected to MCU ports. The switches are connected as follows:

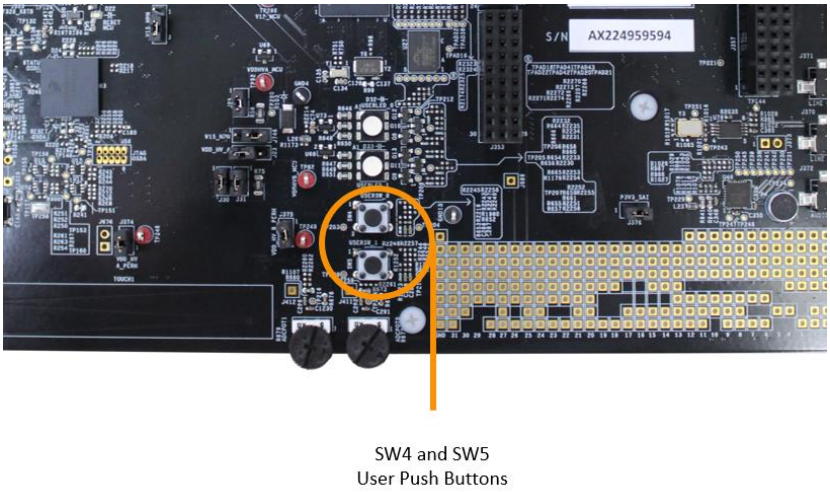


Figure 36. S32K3X8EVB-Q289 – User Push buttons

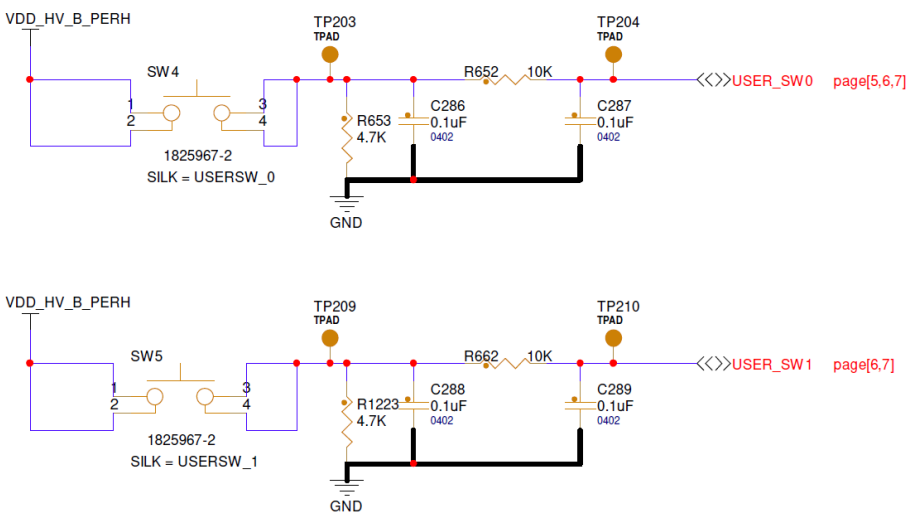


Figure 37. S32K3X8EVB-Q289 – User Push buttons

Table 25. User Pushbuttons

Reference	Function	MCU Port	Comments
SW4	USER_SW0	PTH1	Enabled as DEFAULT
		PTB21	Disabled
		PTD23	Disabled
		PTD31	Disabled
SW5	USER_SW1	PTH3	Enabled as DEFAULT
		PTD27	Disabled
		PTD29	Disabled
		PTF31	Disabled

1. There are zero-ohm resistors on the direct connections between each **USER_SWx** and the MCU pins. These can be removed if required to isolate or change the User Switch from the default MCU pin.

16.4 ADC Rotary Potentiometers

The EVB incorporates a couple of ADC Rotary Potentiometer (which routes a voltage between 0v to VDD_HV_A) directly connected to ADC Precise Input Chanel of the S32K358 Microcontroller.

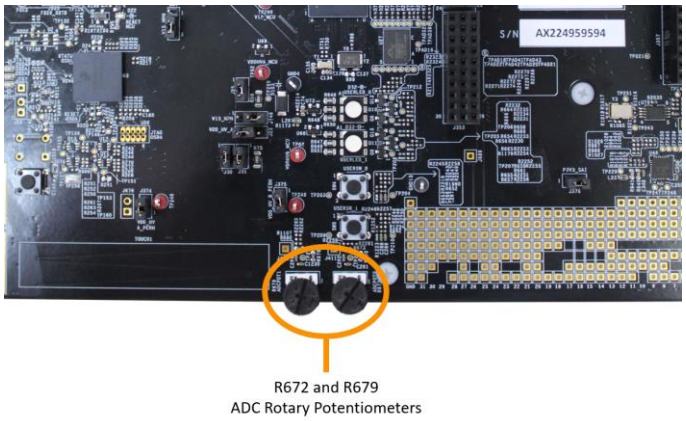


Figure 38. S32K3X8EVB-Q289 – ADC Rotary Potentiometers

Table 26. ADC Potentiometers

Reference	Function	MCU Port	Comments
R672	ADC_POT0	PTA11	Enabled as DEFAULT
		PTA9	Disabled
		PTC24	Disabled
R679	ADC_POT1	PTA17	Enabled as DEFAULT
		PTC31	Disabled

1. There are zero-ohm resistors on the direct connections between each **ADC_POTx** and the MCU pins. These can be removed if required to isolate or change the User Switch from the default MCU pin.

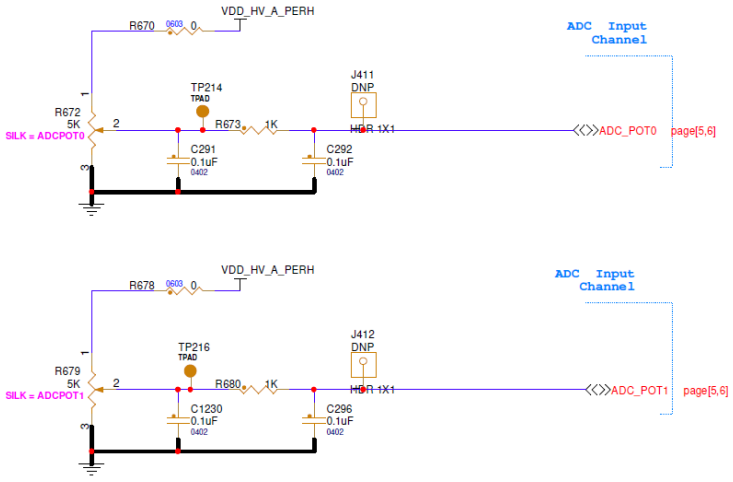


Figure 39. S32K3X8EVB-Q289 – ADC Rotary Potentiometers

17 S32K3X8EVB-Q289 - Default Jumpers

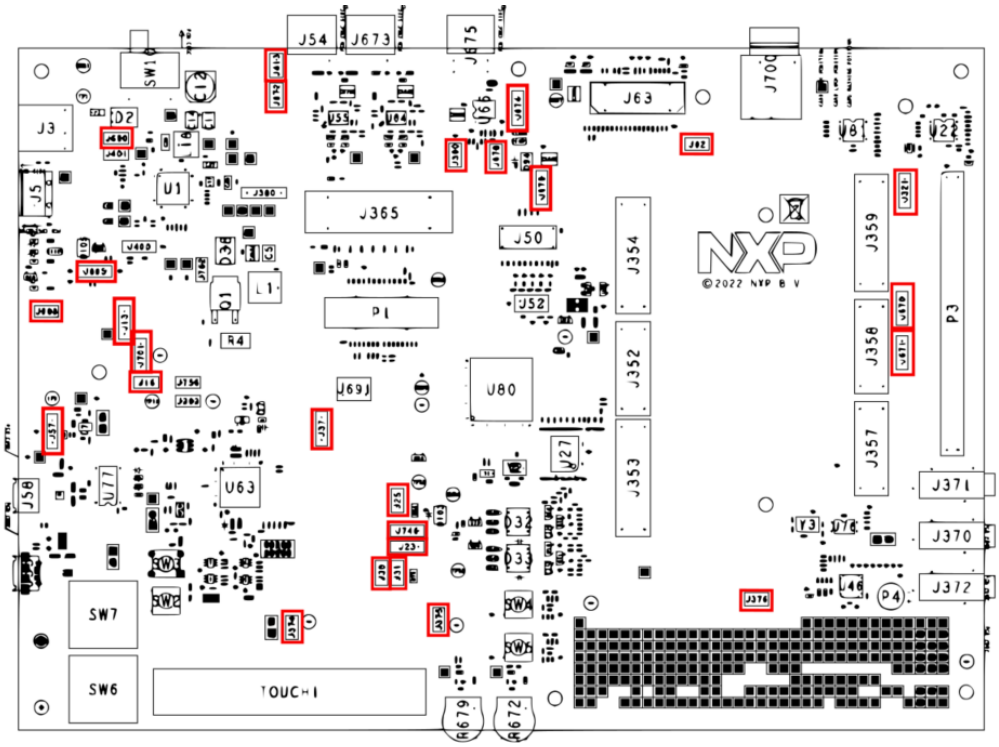


Figure 40. S32K3X8EVB-Q289 – Default jumpers configuration

Table 27. Default Jumper Configuration

Interface	Reference	Position	Description / Comments
FS26/SBC SBC Power Supply	**J13**	1-2	FS26_VLDO1 [+5.0V] is routed to P5V0 domain
	J16	1-2	FS26_VLDO2 [+3.3V] is routed to P3V3 domain
	J701	1-2	FS26_VTRK2 [+3.3V] is routed to P3V3_PERH domain
	J685	1-2	Select the debug mode of the FS26
	J688	1-2	Power LED Indicators enabled
S32K358 MCU Power Supply	**J23**	1-2	P5V0 (+5.0V from the FS26) is selected for the VDD_HV_A_MCU reference.
	J25	1-2	VDD_HV_A is routed to VDD_HV_A_MCU reference. Remove R58 to enable J25 functionality.
	J30	1-2	P3V3 (+3.3V from the FS26) is selected for the VDD_HV_B_MCU reference.
	J31	1-2	VDD_HV_B is routed to VDD_HV_B_MCU reference. Remove R75 to enable J31 functionality.
	J375	1-2	VDD_HV_B is routed to VDD_HV_B_PERH
	J374	1-2	VDD_HV_A is routed to VDD_HV_A_PERH
	J691	1-2	V15_NPN [+1.5V] is routed to V15_MCU domain

	J37	2-3	VDD_HV_B_MCU is routed to the collector pin of the V15 ballast transistor.
	J746	2-3	VDD_HV_B_MCU is routed to the source pin of the V15 DC/DC converter
USB to UART/I2C Interface	**J57**	1-2	USB is in self-powered configuration.
Ethernet Interface	**J62**	1-2	P3V3 domain is routed to P3V3_ENET
User Peripherals	**J670**	1-2	PTE0 is routed to the ARDUINO shield connectors
	J671	1-2	PTE1 is routed to the ARDUINO shield connectors
	J321	1-2	VDD_HV_A_PERH is routed to VDD_IO
LIN Interface	**J390**	1-2	LIN1 physical layer is enabled
	J678	1-2	LIN2 physical layer is enabled
CAN Interface	**J413**	1-2	CAN1 physical layer is enabled
	J672	1-2	CAN2 physical layer is enabled

18 S32K3X8EVB-Q289 – Errata

18.1 S32K3X8EVB-Q289 – V15 SMPS

The EVB must have only one type of power connected for V15. For example, when the NPN transistor and the SMPS are left connected but inactive, they can create an unwanted RESET when the SMPS is deactivated by software (LMSMPSEN = 0b), this phenomenon occurs only when there are multiple sources connected. A workaround is to only connect a single source either FS26_Core, NPN or SMPS.

18.2 S32K3X8EVB-Q289 – TXCLK Crystal

In order to have a proper RGMII ethernet communication an oscillator of 50 MHz was added to the “TXCLK” pin of the SABRE Connector in order to follow the communication standard.

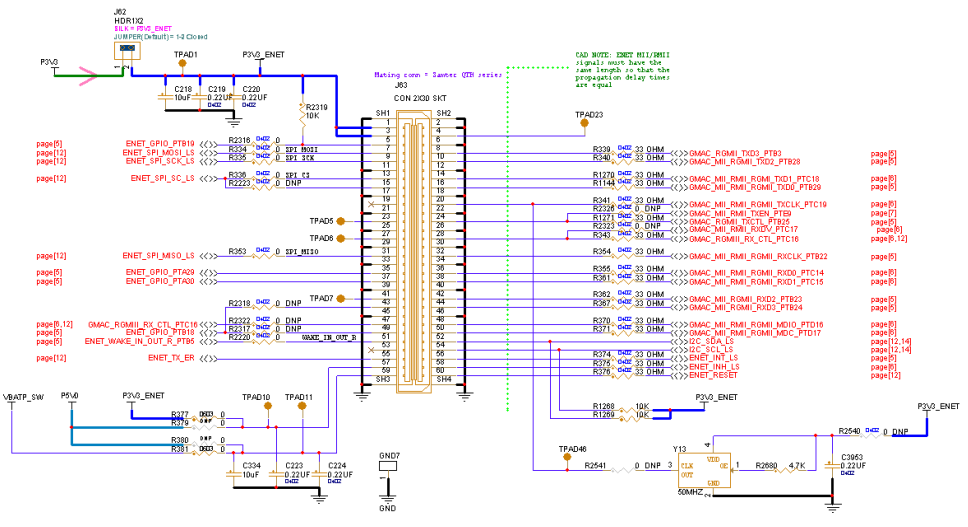


Figure 41. TXCLK errata

18.3 QSPI

Earlier versions of the schematic have an outdated component with pin B1 and B5 swapped, specifically versions prior to C have this bug. The image below is show the swap in these pins. This doesn't affect the functionality of the board as long as R714 is populated and R2266 is depopulated.

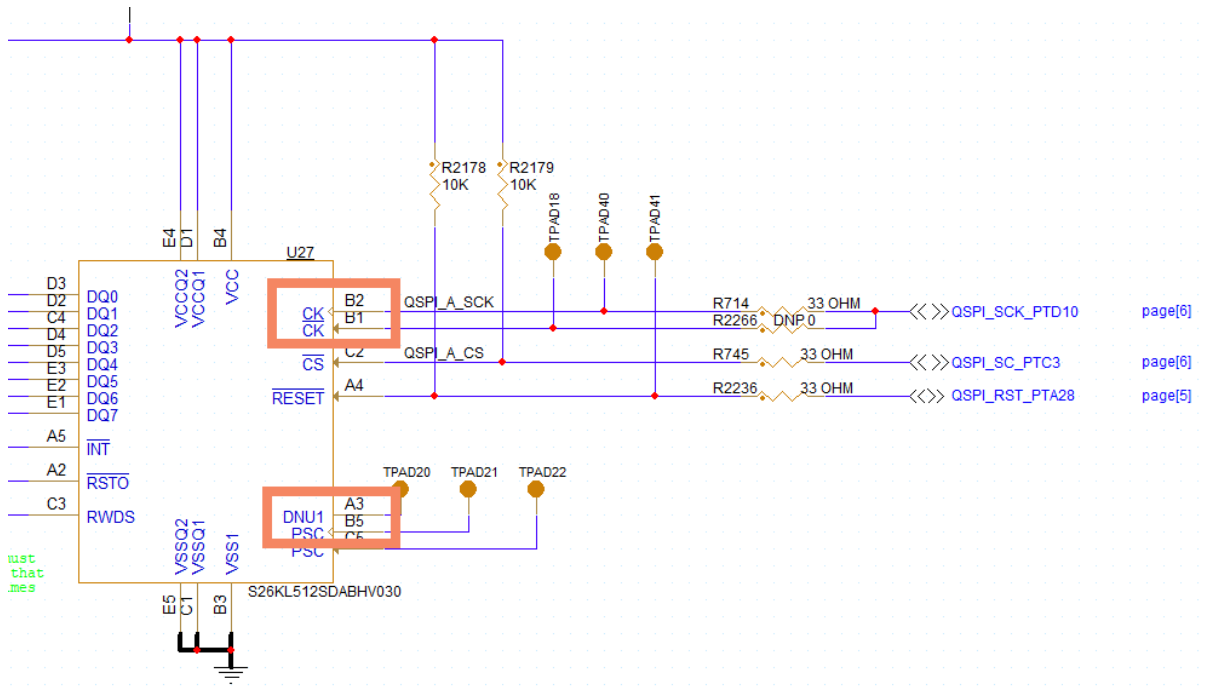


Figure 42. QSPI errata

19 S32K3X8EVB-Q289 – Board versions

Due to the great versatility and a lot of features that this board includes there are 3 different versions, which are described in the following table.

Table 28. S32K3X8EVB-Q289 - Board versions description

Main functionality	Version	Description	Involved components
Prototype	A	Initial release.	NA
Current limiting Power distribution switch U7. Multiple changes in FS26 related to use case.	B	R202 is not populated. This resistor is connected to the pull-up enable signal of the MIC2005-0.8YM6. Low band added to AMUX signal of FS26. Connection in the WAKE pins were modified related to a more general use case. PGOOD circuitry added to the GPIO2 in FS26	R202, U1 (FS26)
Ethernet for RGMII, replacement of obsolete components	C	The main modification between the B2 version and the C version is the addition of a 50 MHz crystal and their circuitry used for RGMII in the SABRE connector. The other changes between version B2 and C is the replacement for obsolete components as the NTS0102GD to NTS0102TLH, SGTL5000AA to SGTL5000BA, etc. Additionally, the DNP Last mile Regulator was replaced from SQ2310ES to SQA410EJ-T1_GE3.	R2540, C3953,R2680, Y13, R2541, U10, U16, U75, U78, U46, Q47

20 S32K3X8EVB-Q289 - Revision history

Table 29. Revision history

Document Revision	Date	Board Name	Schematic/ Board Number	Schematic/ Board Revision	Changes	Author
A	12/2022	S32K3X8EVB-Q289	54870	A	Prototype	Yvan Ramirez
B	02/2023	S32K3X8EVB-Q289	54870	B	Update to pilot version	Yvan Ramirez
C	08/2023	S32K3X8EVB-Q289	54870	C	• Chapter **S32K3X8EVB-Q289 – V11 included** • Subchapter included for Ethernet considerations **Rework for RMII** • Errata chapter included: **S32K3X8EVB-Q289 – Errata** • **Board versions chapter included.**	Yvan Ramirez/Luis Rico

21 Legal Information

21.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

21.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third-party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third-party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third-party customer(s). NXP does not accept any liability in this respect.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — While NXP Semiconductors has implemented advanced security features, all products may be subject to unidentified vulnerabilities. Customers are responsible for the design and operation of their applications and products to reduce the effect of these vulnerabilities on customer's applications and products, and NXP Semiconductors accepts no liability for any vulnerability that is discovered. Customers should implement appropriate design and operating safeguards to minimize the risks associated with their applications and products.

21.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.