Giuseppe Maganuco

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Summary

Passionate Computer Engineering student with a strong interest in system embedded, fpga, electronics and OS. Always eager to learn and take on new challenges.

Projects

For a better overwiev of the projects done: giuko.github.io

DLX processor
Full implementation of a pipelined DLX processor architecture in VHDL, a RISC processor with 5 stage (IF, ID, EX, ME, WB). Following the development from the design, simulation, synthesis and physical design.

UVM testbench
Development of a UVM testbench in SystemVerilog, written for QuestaSim. Analyzed different possible scenerio, covering: Constrained random test generation, Constrained precise generation, Assertion-based verification, Functional coverage collection and analysis.

QEMU Modding
This project involved modifying the QEMU emulator to support the NXP S32K3x8 development board, enabling full system emulation. The work included implementing peripheral emulation, particularly for UART communication, and integrating FreeRTOS support for real-time operating system testing.

Optimizer for Gate-Level Netlist
Developed a custom power optimization tool written in TCL that analyzes gate-level netlists and optimizes power consumption by intelligently adjusting voltage thresholds of individual cells. The optimizer respects timing and design constraints while maximizing power savings.

Education

2024 - present	Master's Degree in Computer Engineering Embedded System - Second year	
2021 - 2024	Bachelor's Degree in Computer Engineering, Università di Catania	(110 cum laude)

Skills

Language Spoken	Italian (native), English Fluent (C1 in CEFR)
Hardware Description Language	VHDL, SystemVerilog
Verification	UVM
Scripting	Bash, TCL
Tools	QEMU, QuestaSIM, Innovus
Programming Language	C, python
Miscellaneous	FreeRTOS, GIT, Linux, Javascript

Last updated: October 16, 2025

Giuseppe Francesco Vincenzo MAGANUCO

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https://giuko.github.io/

EDUCATION

10/14/2024 - up to present *

Master's Degree in Computer Engineering

Politecnico di Torino

average mark 28.9 - Credits 45 %

07/20/2021 - 10/04/2024

Bachelor's Degree in Ingegneria Informatica

Università di Catania

Thesis: ANALISI DEI MODELLI DI MOLTIPLICATORI APPROSSIMATI PER APPLICAZIONI RESILIENTI ALL'ERRORE

Verificare il funzionamento di diversi modelli di moltiplicatori approssimati, da essere utilizzati in diversi ambiti, quali AI o processamento di immagini

Final grade 110/110 cum laude

2021

high school diploma AMM. FINANZA E MARKETING SISTEMI INF. AZIENDALI

Final grade 100/100

LANGUAGE SKILLS

Mother tongue: Italian

Other languages

	UNDERSTANDING		SPEAKING		WRITING
	Listening	Reading	Spoken interaction	Spoken production	
English	C1	C1	C1	C1	C1

Levels: A1/2: Basic user - B1/2: Independent user - C1/2 Proficient user

Common European Framework of Reference for Languages

COMPUTER SKILLS

OPERATING SYSTEM: advanced level

PROGRAMMING LANGUAGE/CODE: advanced level

PROGRAMS/SOFTWARE: advanced level

DATABASES: good level

SPREADSHEET

good level

EXAMS *

Master's Degree in Computer Engineering

conference date	Exam	Credits	Final grade
01/23/2025	Electronics for embedded systems	10	28
02/12/2025	Computer architectures	10	29
02/17/2025	Specification and simulation of digital systems	6	30 cum laude
06/23/2025	Software engineering	8	27
07/07/2025	Synthesis and optimization of digital systems	6	30 cum laude
07/15/2025	Cybersecurity for Embedded Systems	6	29
09/10/2025	Operating systems for embedded systems	8	30

* *Fields marked with an * are certified by Politecnico di Torino, while the potential thesis description is added by the candidate.*