

Proiect Circuite Integrate Digitale

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Grupa: 2125

Temă proiect:

1. Automatul de tranziții: 22
2. Tabel de adevăr pentru bistabil: H.
3. Implementare: III. MUX 4:1 și porți logice
4. Instrucțiuni implementare MUX: iv. Instrucțiunea secvențială CASE

1. Rezolvarea proiectului pe hârtie

Proiect CIB
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Automate de tranziții

22.

Tabel de adevăr pentru bistabil

n	clk	Action
1	x	Reset
0	↓	$Q^+ = JK$
otherwise		Wait

H. - Bistabil JK

Implementare

III. MUX 4:1 și porți logice

Instrucțiuni implementare MUX

iv. instrucțiunea secvențială CASE

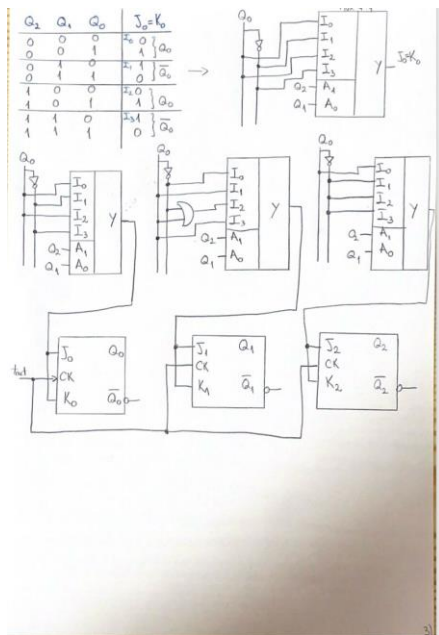
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	$J_2=K_2$	$J_1=K_1$	$J_0=K_0$
0	0	0	x	x	x	x	x	x
0	0	1	1	0	0	1	x	x
0	1	0	1	1	1	1	x	x
0	1	1	0	0	1	0	x	x
1	0	0	0	1	0	x	1	x
1	0	1	1	1	0	x	1	x
1	1	0	0	1	1	x	1	x
1	1	1	1	0	1	x	1	x

Q_2^+ este x0 sau 0x $\Rightarrow JK$ este 0
 Q_2^+ este x1 sau 1x $\Rightarrow JK$ este 1

Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	$J_2=K_2$	$J_1=K_1$	$J_0=K_0$
0	0	0	x	x	x	x (0)	x (1)	x (0)
0	0	1	1	0	0	1	0	1
0	1	0	1	1	1	1	0	1
0	1	1	0	0	1	0	1	0
1	0	0	0	1	0	1	1	0
1	0	1	1	1	0	0	1	1
1	1	0	0	1	1	1	0	1
1	1	1	1	0	1	0	1	0

1)

2)



2. Rezolvarea proiectului în Vivado

2.1. Surse de design

- MUX 4:1

```

mux4.vhd
D:/CID/proiect_CID/proiect_CID/srcs/sources_t1/mux4.vhd

20
21
22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24 -- Uncomment the following library declaration if using
25 -- arithmetic functions with Signed or Unsigned values
26 --use IEEE.NUMERIC_STD.ALL;
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx leaf cells in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31 entity mux4 is
32     Port ( i0 : in STD_LOGIC;
33           i1 : in STD_LOGIC;
34           i2 : in STD_LOGIC;
35           i3 : in STD_LOGIC;
36           a1 : in STD_LOGIC;
37           a0 : in STD_LOGIC;
38           y : out STD_LOGIC);
39 end mux4;
40 architecture Behavioral of mux4 is
41
42     signal a : std_logic_vector (1 downto 0);
43     begin
44         a <= a0;
45         process(a, i0, i1, i2, i3)
46         begin
47             case a is
48                 when "00" =>
49                     y <= i0;
50                 when "01" =>
51                     y <= i1;
52                 when "10" =>
53                     y <= i2;
54                 when others =>
55                     y <= i3;
56             end case;
57         end process;
58     end Behavioral;
59

```

- Poarta inversoare (not)

```
inversor.vhd
D:/CID/proiect_CID/proiect_CID/srcs/sources_1/new/inversor.vhd

7  -- Module Name: inversor - Behavioral
8  -- Project Name:
9  -- Target Devices:
10 -- Tool Versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 -----
20
21
22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 -- Uncomment the following library declaration if using
26 -- arithmetic functions with Signed or Unsigned values
27 --use IEEE.NUMERIC_STD.ALL;
28
29 -- Uncomment the following library declaration if instantiating
30 -- any Xilinx leaf cells in this code.
31 --library UNISIM;
32 --use UNISIM.VComponents.all;
33
34 entity inversor is
35     Port ( a : in STD_LOGIC;
36           f : out STD_LOGIC);
37 end inversor;
38
39 architecture Behavioral of inversor is
40
41 begin
42
43     f <= not a;
44
45 end Behavioral;
46
```

- Poarta OR

```
or2.vhd
D:/CID/proiect_CID/proiect_CID/srcs/sources_1/new/or2.vhd

7  -- Module Name: or2 - Behavioral
8  -- Project Name:
9  -- Target Devices:
10 -- Tool Versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 -----
20
21
22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 -- Uncomment the following library declaration if using
26 -- arithmetic functions with Signed or Unsigned values
27 --use IEEE.NUMERIC_STD.ALL;
28
29 -- Uncomment the following library declaration if instantiating
30 -- any Xilinx leaf cells in this code.
31 --library UNISIM;
32 --use UNISIM.VComponents.all;
33
34 entity or2 is
35     Port ( a : in STD_LOGIC;
36           b : in STD_LOGIC;
37           f : out STD_LOGIC);
38 end or2;
39
40 architecture Behavioral of or2 is
41
42 begin
43
44     f <= a or b;
45
46 end Behavioral;
47
```

- Bistabilul JK

```

bistabil_JK.vhd
D:\CD\proiect_CD\proiect_CD\srcs\sources_tnew\bistabil_JK.vhd

20
21
22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 -- Document the following library declaration if using
26 -- arithmetic functions with Signed or Unsigned values
27 --use IEEE.NUMERIC_STD.ALL;
28
29 -- Document the following library declaration if instantiating
30 -- any Xilinx leaf cells in this code.
31 --library UNISIM;
32 --use UNISIM.VComponents.all;
33
34 entity bistabil_JK is
35     Port ( jk : in STD_LOGIC;
36           clk : in STD_LOGIC;
37           r : in STD_LOGIC;
38           q : out STD_LOGIC;
39           qn : out STD_LOGIC);
40 end bistabil_JK;
41
42 architecture Behavioral of bistabil_JK is
43     signal qint : std_logic;
44 begin
45     flipflop: process(r, clk)
46     begin
47         if r = '1' then
48             qint <= '0';
49         elsif falling_edge (clk) then
50             qint <= jk;
51         else
52             qint <= qint;
53         end if;
54     end process;
55
56     q<=qint;
57     qn<=not qint;
58 end Behavioral;

```

- Automatul

```

automat.vhd
D:\CD\proiect_CD\proiect_CD\srcs\sources_tnew\automat.vhd

22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 -- Document the following library declaration if using
26 -- arithmetic functions with Signed or Unsigned values
27 --use IEEE.NUMERIC_STD.ALL;
28
29 -- Document the following library declaration if instantiating
30 -- any Xilinx leaf cells in this code.
31 --library UNISIM;
32 --use UNISIM.VComponents.all;
33
34 entity automat is
35     Port ( clk : in STD_LOGIC;
36           r : in STD_LOGIC;
37           q : out STD_LOGIC_VECTOR (2 downto 0));
38 end automat;
39
40 architecture Behavioral of automat is
41
42     component bistabil_JK is
43         Port ( jk : in STD_LOGIC;
44               clk : in STD_LOGIC;
45               r : in STD_LOGIC;
46               q : out STD_LOGIC;
47               qn : out STD_LOGIC);
48     end component bistabil_JK;
49
50     component mux4 is
51         Port ( i0 : in STD_LOGIC;
52               i1 : in STD_LOGIC;
53               i2 : in STD_LOGIC;
54               i3 : in STD_LOGIC;
55               a1 : in STD_LOGIC;
56               a0 : in STD_LOGIC;
57               y : out STD_LOGIC);
58     end component mux4;
59
60     component inverter is
61         Port ( a : in STD_LOGIC;
62               f : out STD_LOGIC);
63     end component inverter;

```

```

automatvhdl
D:\CID\project_CID\project_CID srcs\srcs\the\automatvhdl

41      f : out STD_LOGIC;
42    end component inverter;
43  component or2 is
44    Port ( a : in STD_LOGIC;
45          b : in STD_LOGIC;
46          f : out STD_LOGIC);
47  end component or2;
48
49  signal q1:std_logic_vector(2 downto 0);
50  signal y1, y2, y3, y4, y5: std_logic;
51
52  begin
53
54    q <= q1;
55
56    U0: mux4 port map (i0 => q1(0),
57                      i1 => y4,
58                      i2 => q1(0),
59                      i3 => y4,
60                      a1 => q1(2),
61                      a0 => q1(1),
62                      y=>y1);
63    U1: inverter port map ( a=> q1(0),
64                          f => y4);
65
66    U3: mux4 port map ( i0 => q1(0),
67                      i1 => y4,
68                      i2 => y4,
69                      i3 => y4,
70                      a1 => q1(2),
71                      a0 => q1(1),
72                      y=>y3);
73    U5: or2 port map ( a => q1(0),
74                     b => y4,
75                     f=> y3);
76    U4: mux4 port map ( i0 => y4,
77                      i1 => q1(0),
78                      i2 => y5,
79                      i3 => q1(0),
80

```

```

automatvhdl
D:\CID\project_CID\project_CID srcs\srcs\the\automatvhdl

83      y=>y1);
84    U1: inverter port map ( a=> q1(0),
85                          f => y4);
86
87    U3: mux4 port map ( i0 => q1(0),
88                      i1 => y4,
89                      i2 => y4,
90                      i3 => y4,
91                      a1 => q1(2),
92                      a0 => q1(1),
93                      y=>y3);
94    U5: or2 port map ( a => q1(0),
95                     b => y4,
96                     f=> y3);
97    U4: mux4 port map ( i0 => y4,
98                      i1 => q1(0),
99                      i2 => y5,
100                     i3 => q1(0),
101                     a1 => q1(2),
102                     a0 => q1(1),
103                     y=>y2);
104    U6: bistabil_NK port map (y1 => y1,
105                             clk => clk,
106                             z => z,
107                             q => q1(0));
108
109    U7: bistabil_NK port map (y2 => y2,
110                             clk => clk,
111                             z => z,
112                             q => q1(1));
113
114    U8: bistabil_NK port map (y3 => y3,
115                             clk => clk,
116                             z => z,
117                             q => q1(2));
118
119
120  end Behavioral;
121

```

2.2. Surse de simulare

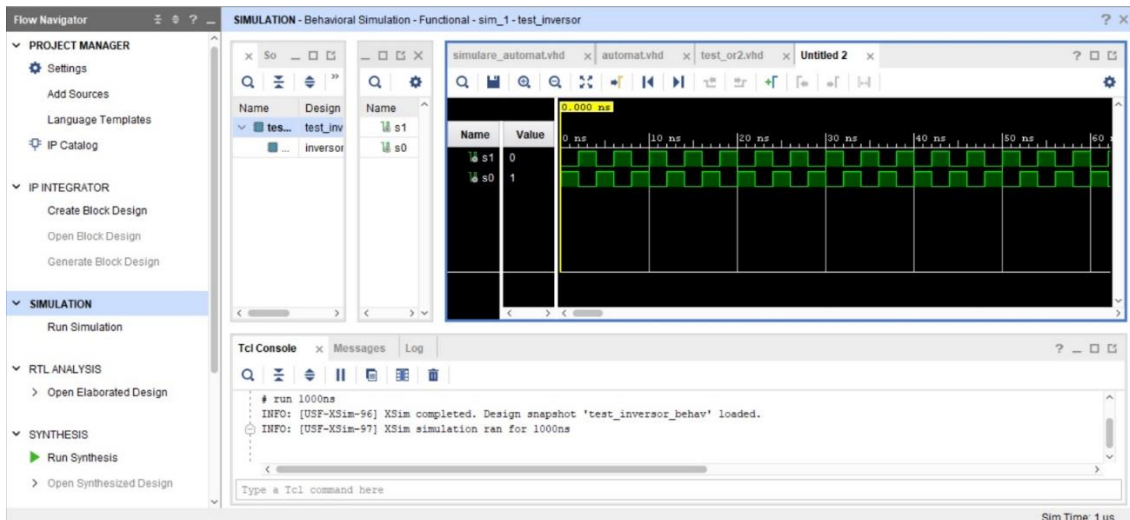
- Simulare poarta inversoare

```

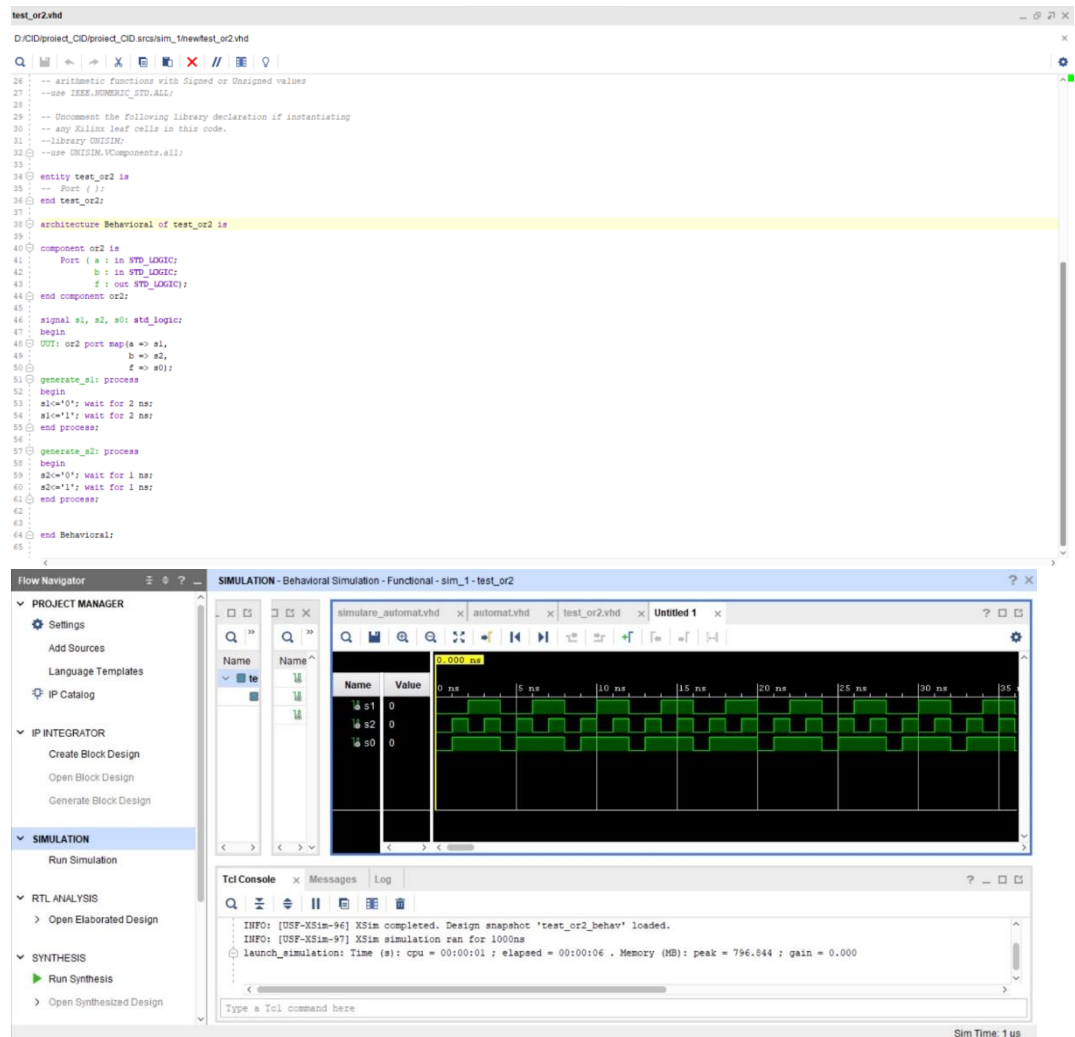
test_inversor.vhd
D:\CID\project_CID\project_CID srcs\sim\the\test_inversor.vhd

17  -- Additional Comments:
18  --
19  -----
20
21
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity test_inversor is
35    Port ( );
36  end test_inversor;
37
38  architecture Behavioral of test_inversor is
39    component inverter is
40      Port ( a : in STD_LOGIC;
41            f : out STD_LOGIC);
42    end component inverter;
43    signal a1, s:std_logic;
44
45  begin
46    UUT: inverter port map(a => a1,
47                          f => s);
48
49    generate_a1: process
50    begin
51      a1<='0'; wait for 2 ns;
52      a1<='1'; wait for 2 ns;
53    end process;
54
55  end Behavioral;
56

```



- Simulare poarta OR



- Simulare automat

