# Proiect Circuite Integrate Digitale

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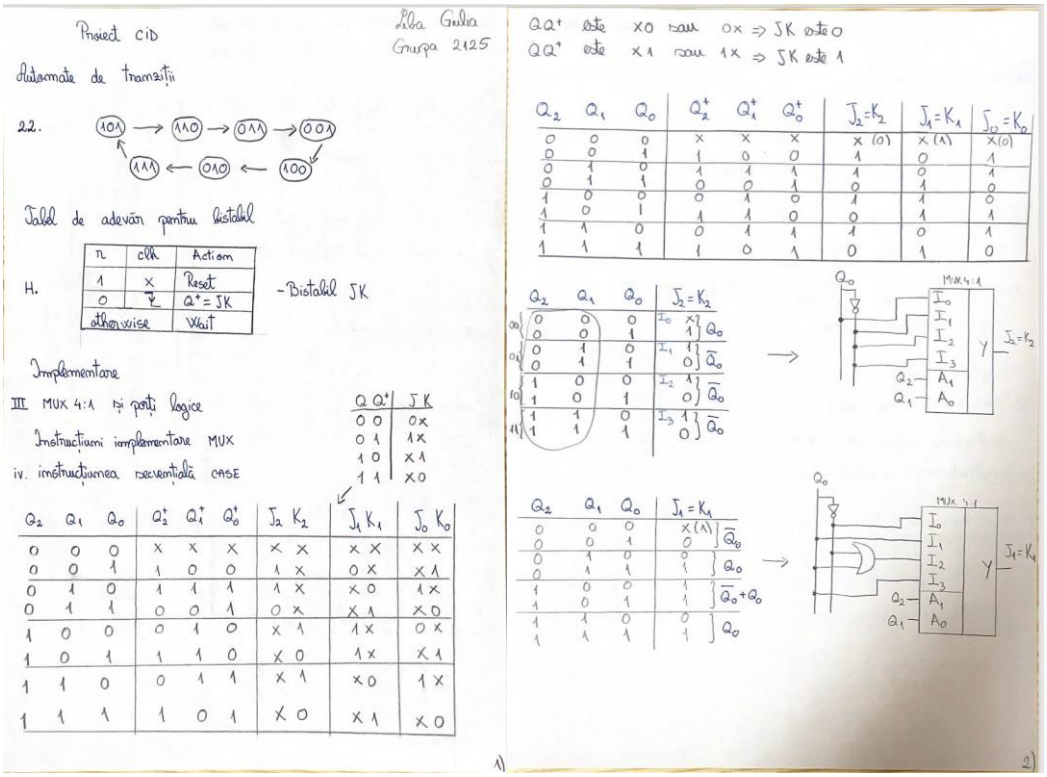
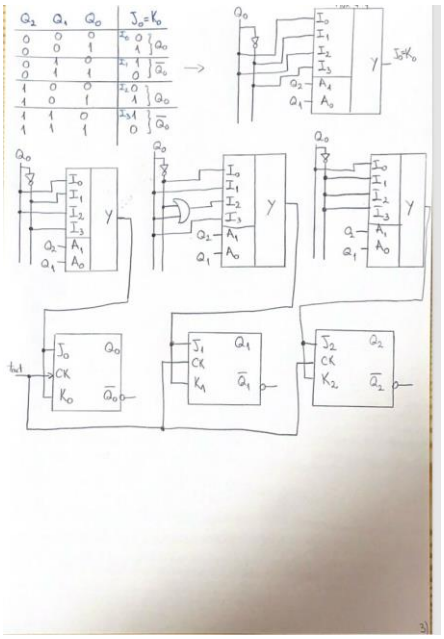
Grupa: 2125

Temă proiect:

1. Automatul de tranziții: 22
2. Tabel de adevăr pentru bistabil: H.
3. Implementare: III. MUX 4:1 și porți logice
4. Instrucțiuni implementare MUX: iv. Instrucțiunea secvențială CASE

## 1. Rezolvarea proiectului pe hârtie





## 2. Rezolvarea proiectului în Vivado

### 2.1. Surse de design

- MUX 4:1

mux4.vhd

D:/CID/proiect_CID/proiect_CID.srcs/sources_1/new/mux4.vhd

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity mux4 is
    Port ( i0 : in STD_LOGIC;
           i1 : in STD_LOGIC;
           i2 : in STD_LOGIC;
           i3 : in STD_LOGIC;
           a1 : in STD_LOGIC;
           a0 : in STD_LOGIC;
           y : out STD_LOGIC);
end mux4;
architecture Behavioral of mux4 is

signal a: std_logic_vector (1 downto 0);
begin
a<=a1 & a0;
process(a, i0, i1, i2, i3)
    begin
        case a is
            when "00" =>
                y <= i0;
            when "01" =>
                y <= i1;
            when "10" =>
                y <= i2;
            when others =>
                y <= i3;
        end case;
    end process;
end Behavioral;
```

- Poarta inversoare (not)

inversor.vhd

D:/CID/proiect_CID/proiect_CID.srcs/sources_1/new/inversor.vhd

```
-- Module Name: inversor - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity inversor is
    Port ( a : in STD_LOGIC;
           f : out STD_LOGIC);
end inversor;

architecture Behavioral of inversor is

begin

f <= not a;

end Behavioral;
```

- Poarta OR

or2.vhd

D:/CID/proiect_CID/proiect_CID.srcs/sources_1/new/or2.vhd

```
-- Module Name: or2 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity or2 is
    Port ( a : in STD_LOGIC;
           b : in STD_LOGIC;
           f : out STD_LOGIC);
end or2;

architecture Behavioral of or2 is

begin

f <= a or b;
end Behavioral;
```

- Bistabilul JK

bistabil_JK.vhd

D:/CID/proiect_CID/proiect_CID.srcs/sources_1/new/bistabil_JK.vhd

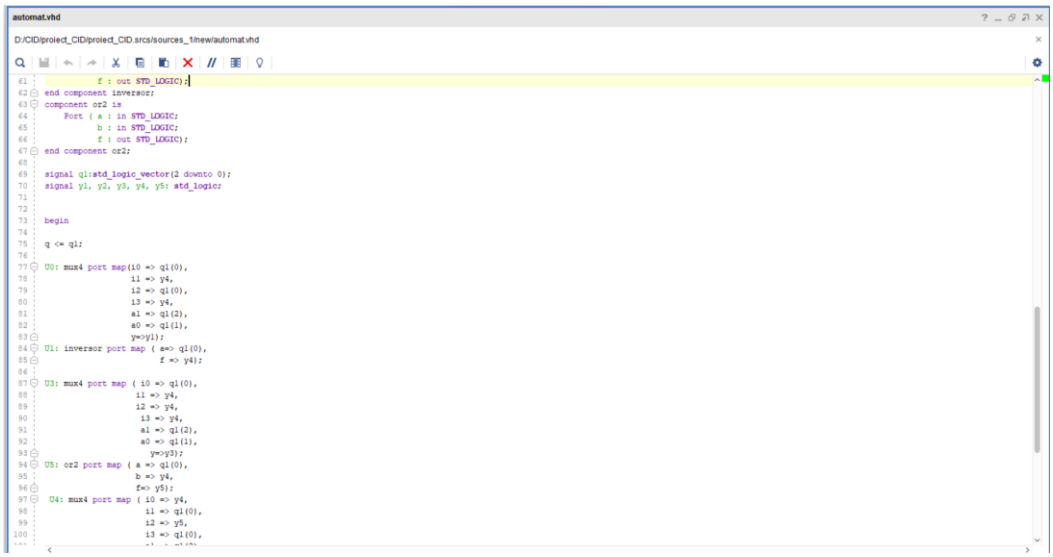
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity bistabil_JK is
    Port ( jk : in STD_LOGIC;
           clk : in STD_LOGIC;
           r : in STD_LOGIC;
           q : out STD_LOGIC;
           qn : out STD_LOGIC);
end bistabil_JK;

architecture Behavioral of bistabil_JK is
signal qint: std_logic;
begin
flipflop: process(r, clk)
begin
  if r = '1' then
     qint <= '0';
  elsif falling_edge (clk) then
     qint <= jk;
  else
     qint <= qint;
  end if;

  end process;

  q<=qint;
  qn<=not qint;
end Behavioral;
```

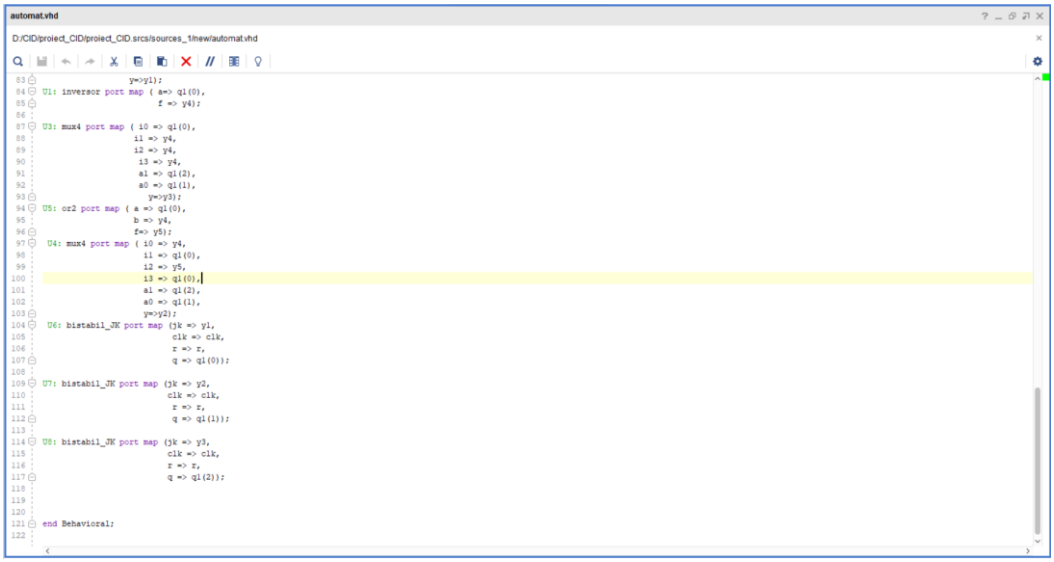
- Automatul

automat.vhd

D:/CID/proiect_CID/proiect_CID.srcs/sources_1/new/automat.vhd

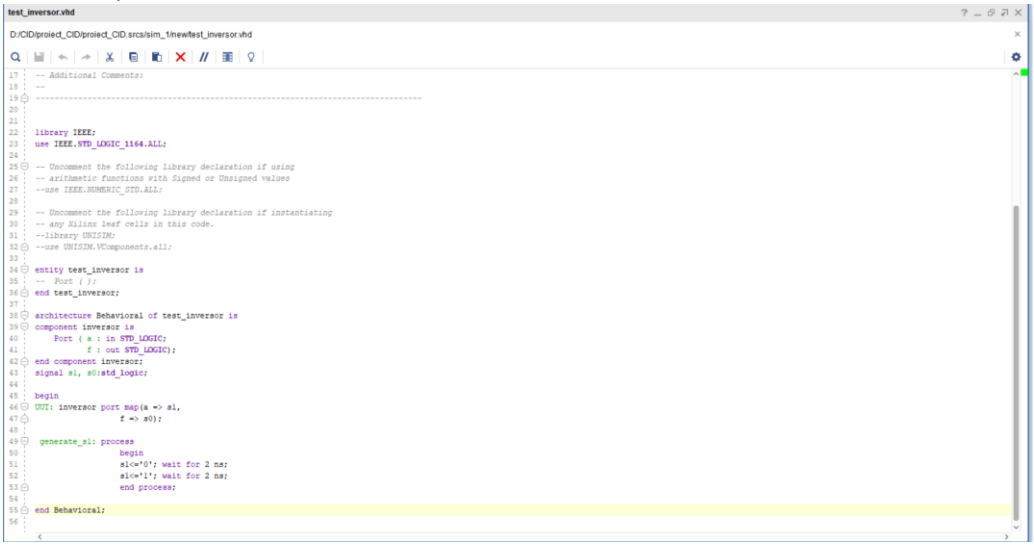
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity automat is
    Port ( clk : in STD_LOGIC;
           r : in STD_LOGIC;
           q : out STD_LOGIC_VECTOR (2 downto 0));
end automat;

architecture Behavioral of automat is

component bistabil_JK is
    Port ( jk : in STD_LOGIC;
           clk : in STD_LOGIC;
           r : in STD_LOGIC;
           q : out STD_LOGIC;
           qn : out STD_LOGIC);
end component bistabil_JK;

component mux4 is
    Port ( i0 : in STD_LOGIC;
           i1 : in STD_LOGIC;
           i2 : in STD_LOGIC;
           i3 : in STD_LOGIC;
           a1 : in STD_LOGIC;
           a0 : in STD_LOGIC;
           y : out STD_LOGIC);
end component mux4;
component inversor is
    Port ( a : in STD_LOGIC;
           f : out STD_LOGIC);
```

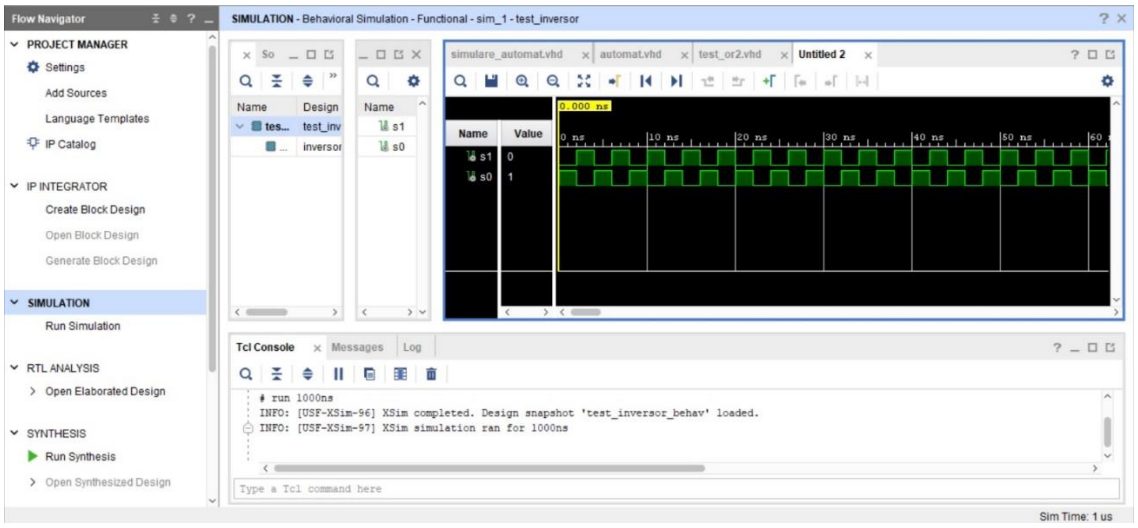


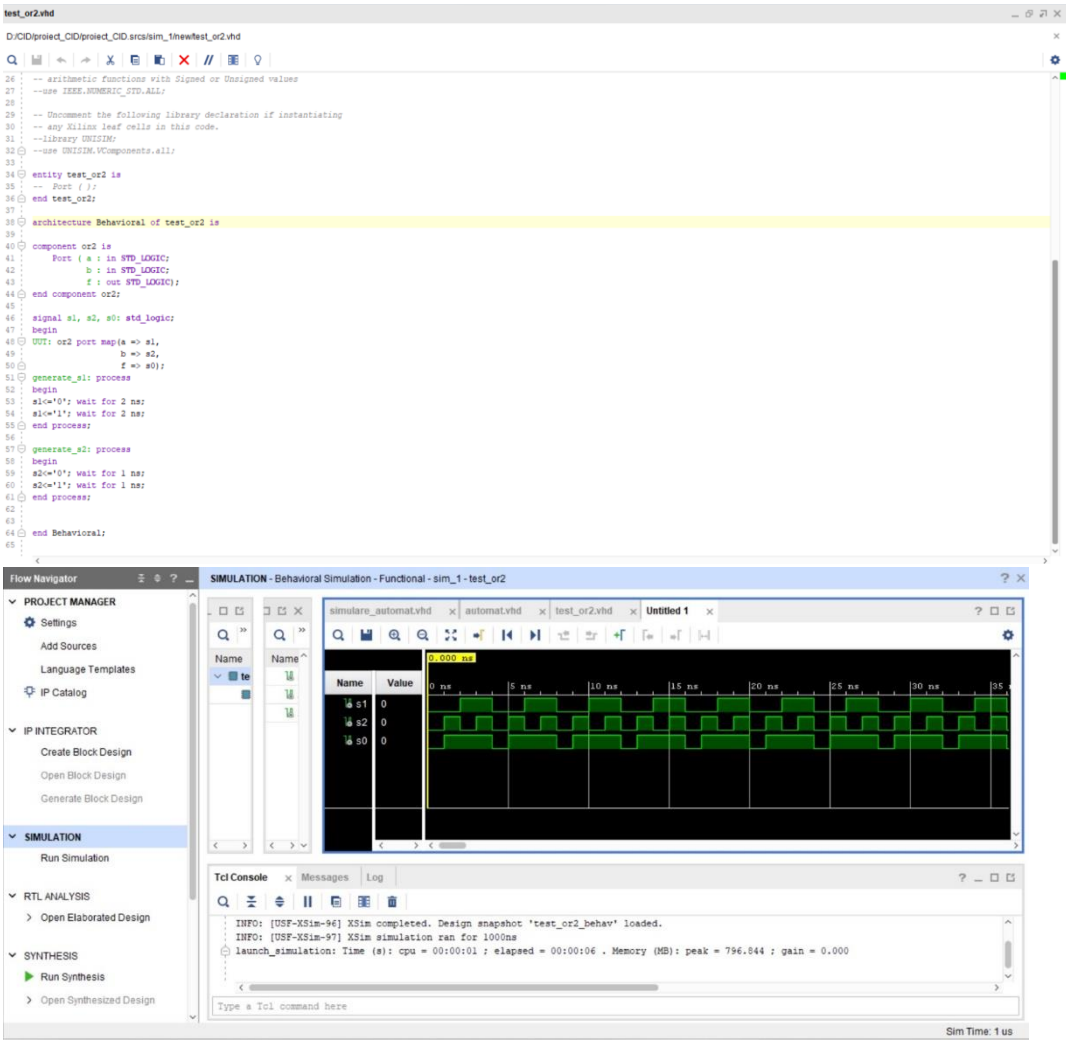

## 2.2. Surse de simulare

- Simulare poarta inversoare

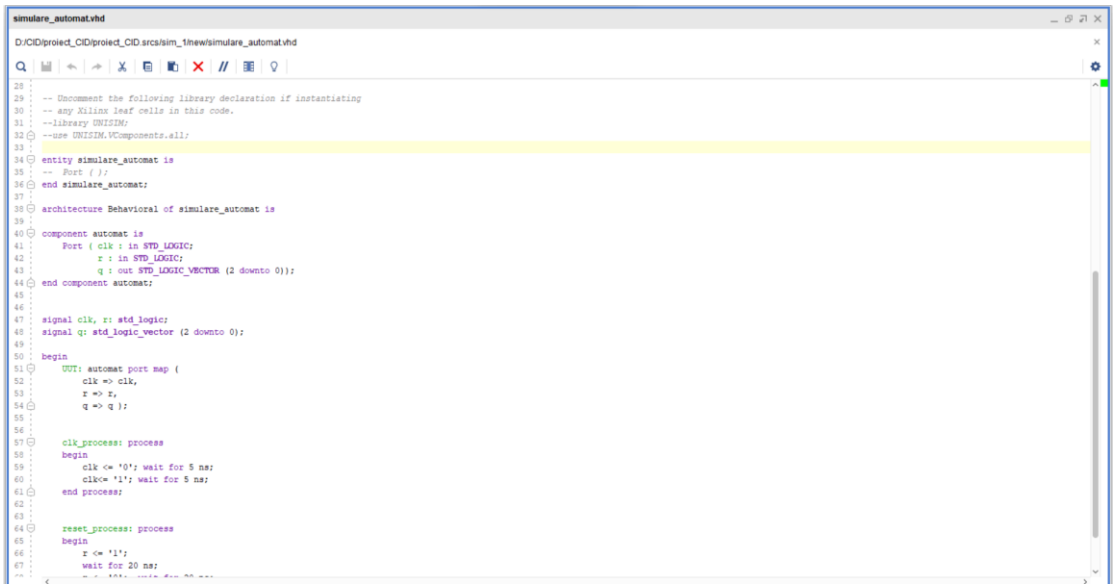


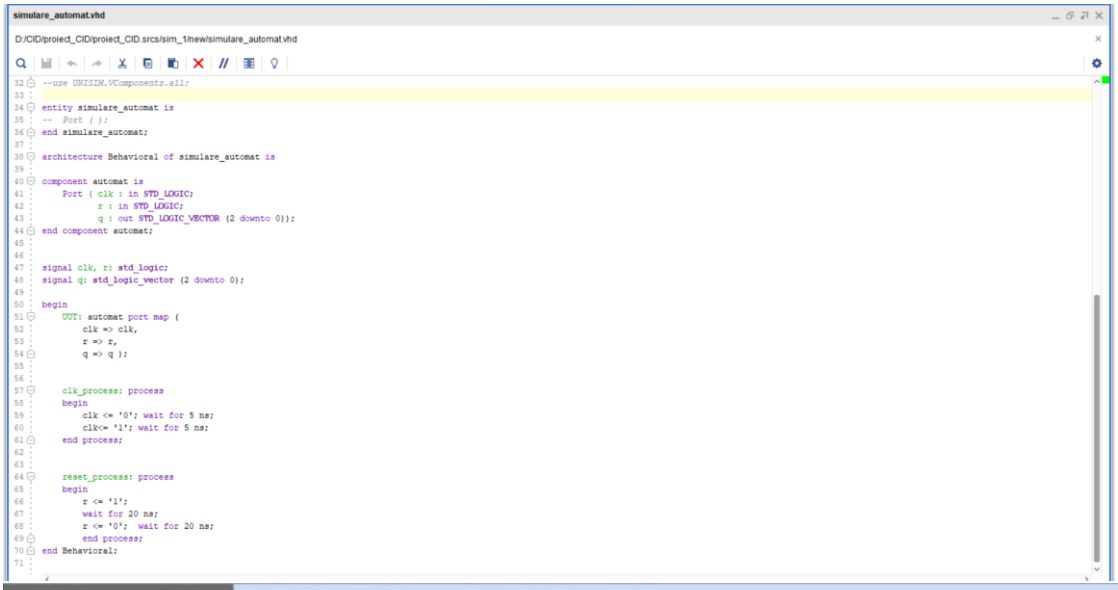


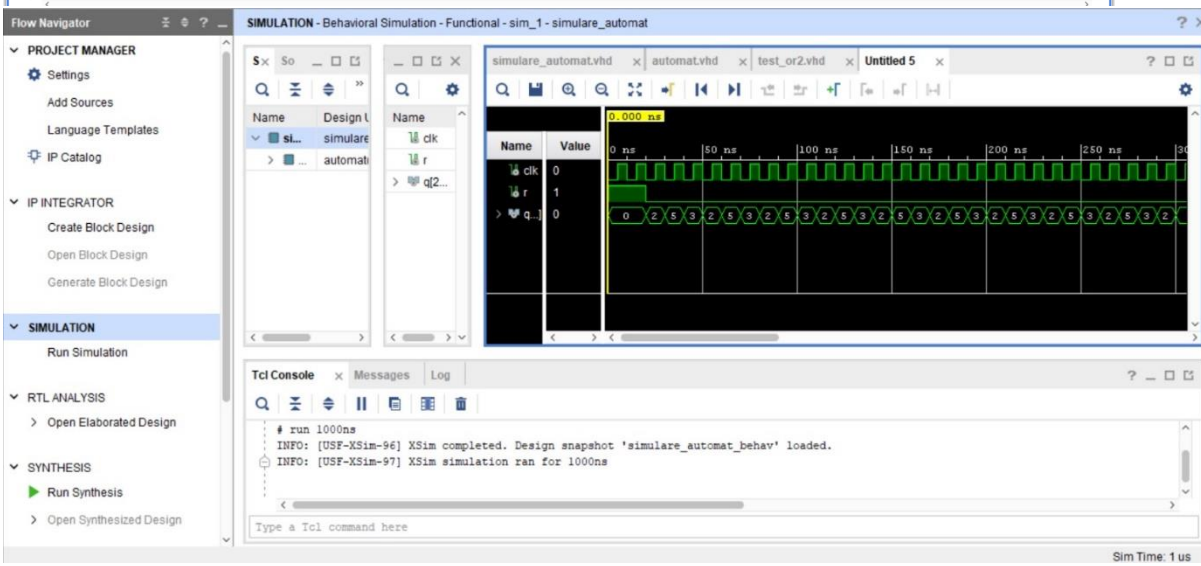

- Simulare poarta OR




- Simulare automat


simulare_automat.vhd
D:/CID/proiect_CID/proiect_CID.srcs/sim_1/new/simulare_automat.vhd
-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity simulare_automat is
--  Port ( );
end simulare_automat;
architecture Behavioral of simulare_automat is
component automat is
Port ( clk : in STD_LOGIC;
r : in STD_LOGIC;
q : out STD_LOGIC_VECTOR (2 downto 0));
end component automat;
signal clk, r: std_logic;
signal q: std_logic_vector (2 downto 0);
begin
UUT: automat port map (
clk => clk,
r => r,
q => q );
clk_process: process
begin
clk <= '0'; wait for 5 ns;
clk<= '1'; wait for 5 ns;
end process;
reset_process: process
begin
r <= '1';
wait for 20 ns;


simulare_automat.vhd
D:/CID/proiect_CID/proiect_CID.srcs/sim_1/new/simulare_automat.vhd
--use UNISIM.VComponents.all;
entity simulare_automat is
--  Port ( );
end simulare_automat;
architecture Behavioral of simulare_automat is
component automat is
Port ( clk : in STD_LOGIC;
r : in STD_LOGIC;
q : out STD_LOGIC_VECTOR (2 downto 0));
end component automat;
signal clk, r: std_logic;
signal q: std_logic_vector (2 downto 0);
begin
UUT: automat port map (
clk => clk,
r => r,
q => q );
clk_process: process
begin
clk <= '0'; wait for 5 ns;
clk<= '1'; wait for 5 ns;
end process;
reset_process: process
begin
r <= '1';
wait for 20 ns;
r <= '0';  wait for 20 ns;
end process;
end Behavioral;


Flow Navigator
PROJECT MANAGER
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Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
SIMULATION - Behavioral Simulation - Functional - sim_1 - simulare_automat
simulare_automat.vhd
automat.vhd
test_or2.vhd
Untitled 5
Name
Value
clk
r
0.000 ns
0 ns
50 ns
100 ns
150 ns
200 ns
250 ns
Tcl Console
Messages
Log
# run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'simulare_automat_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
Type a Tcl command here
Sim Time: 1 us