GIULIANO SISTO [in] [github] [iD] [◈] [g]

@ giuliano.sisto1@gmail.com 📞 +32 470 13 63 06 📞 +39 340 41 09 479 📍 Emile van Arenberghstraat 23, 3000, Leuven, Belgium

ABOUT ME

I am an enthusiastic SoC Researcher, with Physical Design expertise and a keen eye for design methodologies. I thrive in contexts where "what?" is always followed by "how?". Currently, I am looking for a chance to boost my knowledge on Computer Architectures while leveraging my expertise in SoC design. My ambition is to steer the semiconductor industry towards the path of Architecture-Design Co-Optimization, as I strongly believe that it will be a key enabler for next generation digital ICs.

EDUCATION

Doctor of Philosophy (PhD), Electrical Engineering
Ecole polytechnique de Bruxelles – Université Libre de Bruxelles

📅 Oct 2018 – Oct 2021(expected)   📍 Leuven, BE

– Thesis:"Design Enablement of integrated circuts using sub-5nm technology process and 3D integration"
– Guest lecturer - ETH Zurich, Politecnico di Bari

Exchange Student, Electronic Systems
Department of Electrical Engineering – Technology University of Eindhoven

📅 Feb 2017 – July 2017   📍 Eindhoven, NL

– Projects: RISC microprocessor design ● interconnection network modelling for a multicore processor ● embedded controller design for automotive (Xilinx FPGA) ● low power RF mixer design

MSc, Electrical Engineering, Micro Electronics Systems
Dipartimento di Ingegneria Elettrica e dell'informazione – Politecnico di Bari

📅 Jan 2016 – Jul 2018   📍 Bari, IT

EXPERIENCE

PhD Candidate
Cadence Design Systems - IMEC

📅 Oct 2018 – Present   📍 Leuven, BE

– Proposal and implementation of new methods to enable advanced technologies for front-end and back-end digital IC design
– Advanced CMOS technology nodes (sub-$5nm$): FinFET ● GAAFET ● CFET
– 3D-IC: Face-to-Face Hybrid Bonding stacking
– Industrial design benchmarking: ARM ● RISC-V ● NVDLA
– European project technical lead for 2nm technology node research

Engineering Internship
Huawei Technologies

📅 Feb 2018 – Jul 2018   📍 Sophia-Antipolis, FR

– Architecture design and physical implementation of digital filters for All Digital PLLs

Event organizing team
Devlounge

📅 Sep 2016 – Nov 2016   📍 Bari, IT

– Technical support to comics convention: Hardware management ● Ordering service

TECHNICAL SKILLS

TCL	●●●●○
Bash	●●●●○
Linux	●●●●○
Verilog, VHDL	●●●○○
Python	●●●○○
Git	●●●○○
Matlab	●●○○○

SOFT SKILLS

Resilience   Problem solving
Project management   Empathy
Affinity to learn   Team player
Public Speaking/Presenting

LANGUAGES

Italian	●●●●●
English	●●●●●
French	●●●○○
Dutch	●○○○○

AWARDS

⚷ ERASMUS+ for Traineeship Scholarship
TUCEP

📅 2018   📍 Bari,IT

⚷ ERASMUS+ Scholarship
Politecnico di Bari

📅 2017   📍 Bari,IT

INTERESTS

Videogames   Board/Card games
eSports   Football   Cinema
Travel   Music

LIST OF PUBLICATIONS

– G.Sisto, P. Debacker, R. Chen, G. Van der Plas, R. Chou, E. Beyne, D. Milojevic, "Design enablement of fine pitch face-to-face 3D system integration using die-by-die place & route", 3DIC 2019, Sendai, Japan
– G.Sisto et al., "IR-Drop Analysis of Hybrid Bonded 3D-ICs with Backside Power Delivery and μ- & n- TSVs", IITC 2021, Kyoto, Japan