GIULIANO SISTO

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ABOUT ME

I am an enthusiastic SoC Researcher, with Physical Design expertise and a keen eye for design methodologies. I thrive in contexts where "what?" is always followed by "how?". Currently, I am looking for a chance to boost my knowledge on Computer Architectures while leveraging my expertise in SoC design. My ambition is to steer the semiconductor industry towards the path of Architecture-Design Co-Optimization, as I strongly believe that it will be a key enabler for next generation digital ICs.

EDUCATION

Doctor of Philosophy (PhD), Electrical Engineering

Ecole polytechnique de Bruxelles – Université Libre de Bruxelles - IMEC

Oct 2018 – June 2022 Leuven, BE

- Thesis:"Design Enablement of integrated circuts using sub-5nm technology process and 3D integration"
- Guest lecturer - ETH Zurich, Politecnico di Bari

MSc, Electrical Engineering, Micro Electronics Systems

Dipartimento di Ingegneria Elettrica e dell'informazione – Politecnico di Bari

Jan 2016 – Jul 2018 Bari, IT

- Feb-July 2017 - Exchange semester at Technology University of Eindhoven (TUe) in the Electronic Systems group (ES)

EXPERIENCE

Chiplet Solution Architect

IMEC

Sep 2023 – Present Leuven, BE

- Drive system architecture development with 2.5D and 3D technologies
- Next generation HPC systems for AI

Researcher

IMEC

Nov 2021 – August 2023 Leuven, BE

- Backside PDN and functional Backside pathfinding
- HW-SW co-design methodologies for STCO

PhD Candidate

Cadence Design Systems - IMEC

Oct 2018 – 2021 Leuven, BE

- Proposal and implementation of new methods to enable DTCO and 3D IC design
- European project technical lead for 2nm technology node research

Engineering Internship

Huawei Technologies

Feb 2018 – Jul 2018 Sophia-Antipolis, FR

- Architecture design and physical implementation of digital filters for All Digital PLLs

TECHNICAL SKILLS

TCL
Bash
Linux
Verilog, VHDL
Python
Git
Matlab

SOFT SKILLS

Resilience | Problem solving | Project management | People management | Mentoring | Empathy | Affinity to learn | Team player | Public Speaking/Presenting

LANGUAGES

Italian
English
French
Dutch

AWARDS

ERASMUS+ for Traineeship Scholarship

TUCEP

2018 Bari,IT

ERASMUS+ Scholarship

Politecnico di Bari

2017 Bari,IT

INTERESTS

Videogames | Board/Card games | eSports | Soccer | Cinema | Travel | Music | Photography

LIST OF PUBLICATIONS

- **G.Sisto**, et al., “Block-level Evaluation and Optimization of Backside PDN for High-Performance Computing at the A14 node”, 2023 IEEE Symposium on VLSI Technology and Circuits, Kyoto, Japan
- **G.Sisto**, et al., “System-level evaluation of 3D power delivery network at 2nm node”, 2023 SPIE Advanced Lithography + Patterning, DTCO and Computational Patterning, San Jose, USA
- **G.Sisto**, et al., “Physical design level PPA evaluation of buried power rail at 2nm node”, 2023 SPIE Advanced Lithography + Patterning, DTCO and Computational Patterning, San Jose, USA
- **G.Sisto**, et al., “Evaluation of Nanosheet and Forksheet Width Modulation for Digital IC Design in the Sub-3nm Era”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 30, no. 10, pp. 1497-1506, Oct. 2022
- R.Chen, **G.Sisto***, et al., “Design and Optimization of SRAM Macro and Logic Using Backside Interconnects at 2nm Node”, IEDM 2021, San Francisco, USA (*authors contributed equally to the work)
- **G.Sisto** et al., “Design And Sign-off Methodologies For Wafer-To-Wafer Bonded 3D-ICs At Advanced Nodes (invited)”, SLIP 2021 (co-hosted with ICCAD 2021), Virtual Event
- **G.Sisto** et al., “IR-Drop Analysis of Hybrid Bonded 3D-ICs with Backside Power Delivery and μ- & n- TSVs”, IITC 2021, Virtual Event
- **G.Sisto** et al., “Design enablement of fine pitch face-to-face 3D system integration using die-by-die place & route”, 3DIC 2019, Sendai, Japan