

ABOUT ME

I am an enthusiastic SoC Researcher, with Physical Design expertise and a keen eye for design methodologies. I thrive in contexts where "what?" is always followed by "how?". Currently, I am looking for a chance to boost my knowledge on Computer Architectures while leveraging my expertise in SoC design. My ambition is to steer the semiconductor industry towards the path of Architecture-Design Co-Optimization, as I strongly believe that it will be a key enabler for next generation digital ICs.

EDUCATION

Doctor of Philosophy (PhD), Electrical Engineering

Ecole polytechnique de Bruxelles – Université Libre de Bruxelles

Oct 2018 – 2022(expected)

Leuven, BE

- Thesis: "Design Enablement of integrated circuits using sub-5nm technology process and 3D integration"
- Guest lecturer - ETH Zurich, Politecnico di Bari

Exchange Student, Electronic Systems

Department of Electrical Engineering – Technology University of Eindhoven

Feb 2017 – July 2017

Eindhoven, NL

MSc, Electrical Engineering, Micro Electronics Systems

Dipartimento di Ingegneria Elettrica e dell'informazione – Politecnico di Bari

Jan 2016 – Jul 2018

Bari, IT

EXPERIENCE

Researcher

IMEC

Nov 2021 – Present

Leuven, BE

PhD Candidate

Cadence Design Systems - IMEC

Oct 2018 – 2021

Leuven, BE

- Proposal and implementation of new methods to enable advanced technologies for front-end and back-end digital IC design
- Advanced CMOS technology nodes (sub-5nm FinFET • GAAFET • CFET) and 3D-IC
- Industrial design benchmarking: ARM • RISC-V • NVDLA
- European project technical lead for 2nm technology node research

Engineering Internship

Huawei Technologies

Feb 2018 – Jul 2018

Sophia-Antipolis, FR

- Architecture design and physical implementation of digital filters for All Digital PLLs

LIST OF PUBLICATIONS

- G.Sisto*, et al., "Evaluation of Nanosheet and Forksheet Width Modulation for Digital IC Design in the Sub-3nm Era", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 30, no. 10, pp. 1497-1506, Oct. 2022
- R.Chen, G.Sisto*, et al., "Design and Optimization of SRAM Macro and Logic Using Backside Interconnects at 2nm Node", IEDM 2021, San Francisco, USA (*authors contributed equally to the work)
- G.Sisto et al., "Design And Sign-off Methodologies For Wafer-To-Wafer Bonded 3D-ICs At Advanced Nodes (invited)", SLIP 2021 (co-hosted with ICCAD 2021), Virtual Event
- G.Sisto et al., "IR-Drop Analysis of Hybrid Bonded 3D-ICs with Backside Power Delivery and μ - & n - TSVs", IITC 2021, Kyoto, Japan
- G.Sisto et al., "Design enablement of fine pitch face-to-face 3D system integration using die-by-die place & route", 3DIC 2019, Sendai, Japan

TECHNICAL SKILLS

TCL
Bash
Linux
Verilog, VHDL
Python
Git
Matlab



SOFT SKILLS

Resilience Problem solving
Project management Empathy
Affinity to learn Team player
Public Speaking/Presenting

LANGUAGES

Italian
English
French
Dutch



AWARDS

ERASMUS+ for Traineeship
Scholarship

TUCEP

2018

Bari, IT

INTERESTS

Videogames Board/Card games
eSports Soccer Cinema
Travel Music