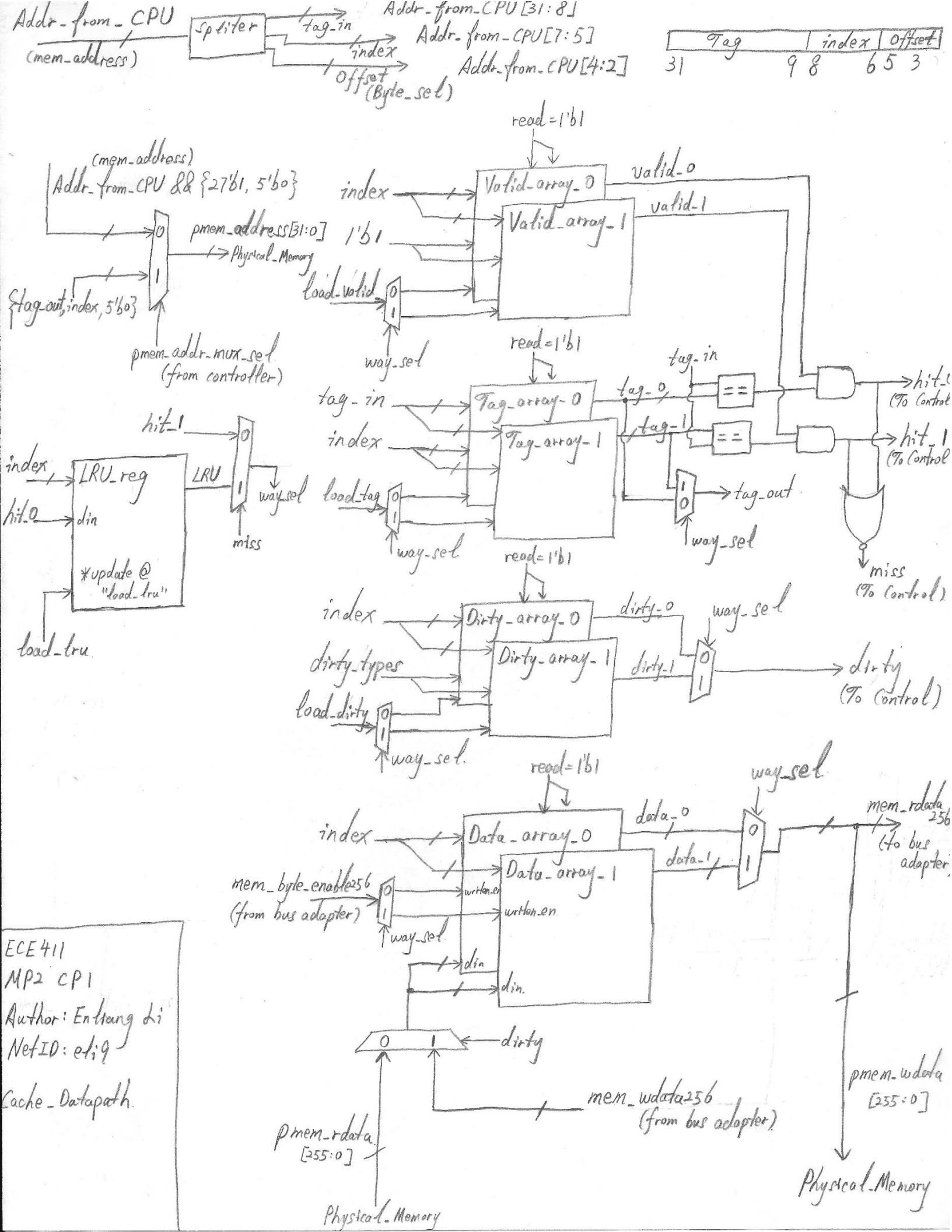

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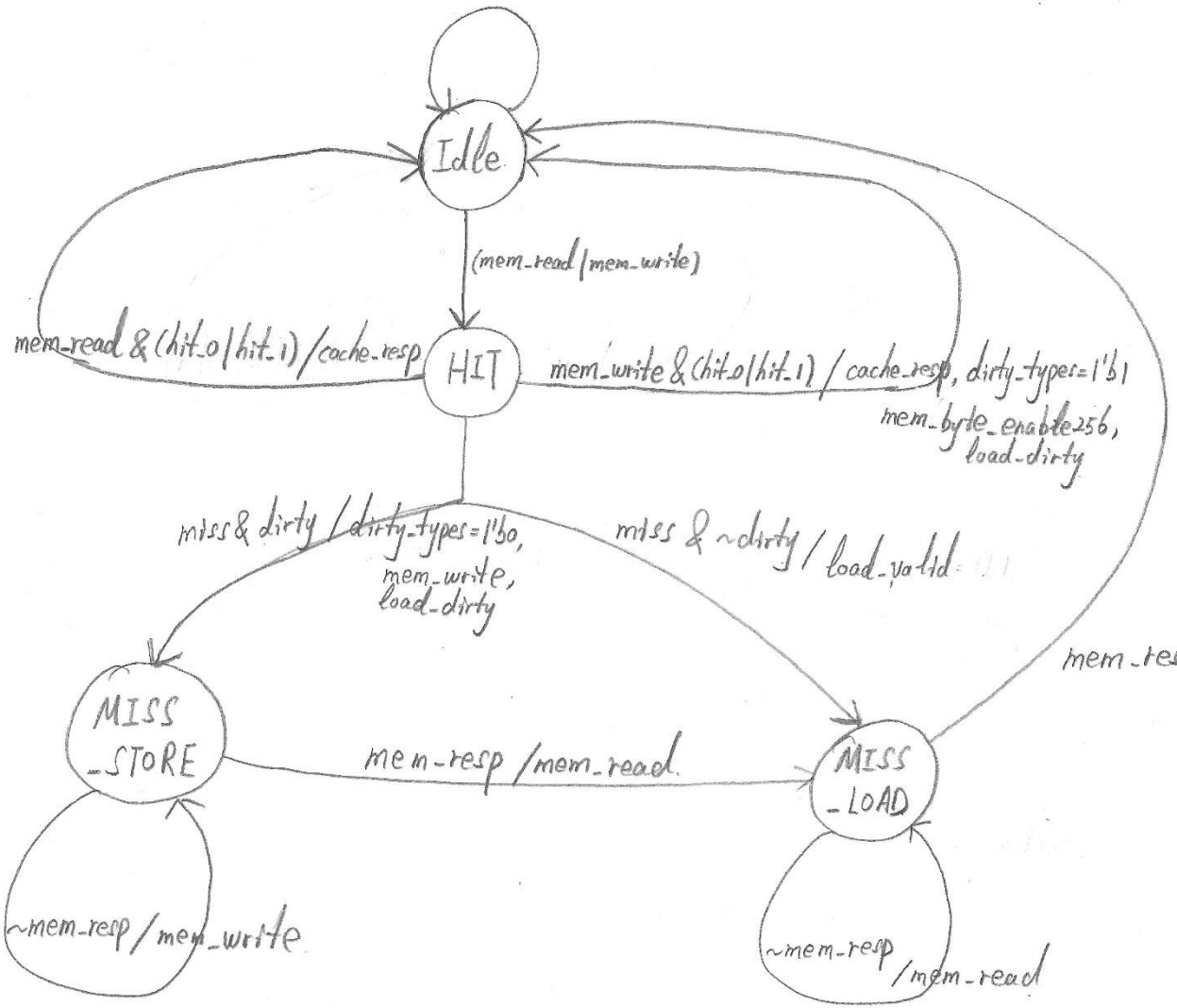
Cache_Datapath

Legend:
Input / Output



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Cache_State_Machine

Answers to testing methodology:

1. MP1 Testing.
    a. No, I didn't use any randomized testing, every test I wrote was functional coverage.
    b. Yes.
    c. Yes, autograding runs tells me where I should look into, usually within one or two states in control state machine or a few wires in datapath.
    d. No. We were not informed on the presence of unaligned-word read nor write by any kind before the final deadline, thus no way for "impact on testing methodology".

2. Two edge cases related to cache design.
    a. Totally empty cold-start cache with consequent write-misses.

    b. A full dirty cache with write-miss followed by read-miss from previous evicted memory location (where just write-back).

3. Cache input stimuli for one of the identified corner cases.

    For the first edge case, "cold-start cache with consequent write-misses"

    (omit clock generation and ports connection)

```
Initial begin
        for (i = 0; i < 8'd256; i++) begin

            mem_address <= i;
            mem_wdata <= i + 8'd1;
            mem_write <= 1'b1;
            ##1

            @(cache_resp)
        end
end
```

4. Briefly describe how to test the cache as the DUT itself.

    If we don't connect ports on cache to our processors but instead to monitor ports in our testbenches, the cache should be considered as the DUT itself.

    By giving stimuli manually, we just simply take the position of our processor.