

[DL] A Survey of FPGA Based Neural Network Accelerator

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Recent researches on neural network have shown great advantage in computer vision over traditional algorithms based on handcrafted features and models. Neural network is now widely adopted in regions like image, speech and video recognition. But the great computation and storage complexity of neural network based algorithms poses great difficulty on its application. CPU platforms are hard to offer enough computation capacity. GPU platforms are the first choice for neural network process because of its high computation capacity and easy to use development frameworks.

On the other hand, FPGA based neural network accelerator is becoming a research topic. With specific designed hardware, FPGA is the next possible solution to surpass GPU in speed and energy efficiency. Various FPGA based accelerator designs have been proposed with software and hardware optimization techniques to achieve high speed and energy efficiency. In this paper, we give an overview of previous work on neural network accelerators based on FPGA and summarize the main techniques used. Investigation from software to hardware, from circuit level to system level is carried out to complete analysis of FPGA based neural network accelerator design and serves as a guide to future work.

CCS Concepts: • **General and reference** → **Surveys and overviews**; • **Computer systems organization** → *Parallel architectures*;

Additional Key Words and Phrases: FPGA architecture, Neural Network, Parallel Processing

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1 INTRODUCTION

Recent research on Neural Network (NN) is showing great improvement over traditional algorithms in computer vision. Various network models, like convolutional neural network (CNN), recurrent neural network (RNN), have been proposed for image, video, and speech process. CNN [22] improves the top-5 image classification accuracy on ImageNet [41] dataset from 73.8% to 84.7% and further helps improve object detection [7] with its outstanding ability in feature extraction. RNN [15] achieves state-of-the-art word error rate on speech recognition. In general, NN features a high fitting ability to a wide range of pattern recognition problems. This makes NN a promising candidate to many artificial intelligence applications.

But the computation and storage complexity of NN models are high. Current researches on NN are still increasing the size of NN models. Take CNN as an example. The largest CNN model for an 224×224 image classification requires upto 39 billion floating point operations (FLOP) and more than 500MB model parameters [47]. As the computation complexity is propotional to the input image size, processing images with higher resolutions may need more than 100 billion operations.

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Therefore, choosing a proper computation platform for neural network based applications is important. A common CPU can perform 10-100G FLOP per second, and the power efficiency is usually below 1GOP/J. So CPUs are hard to meet the high performance requirements in cloud applications nor the low power requirements in mobile applications. In contrast, GPUs offer up to 10TOP/s peak performance and are good choices for high performance neural network applications. Development frameworks like Caffe [20] and Tensorflow [1] also offer easy-to-use interfaces which makes GPU the first choice of neural network acceleration.

Besides CPUs and GPUs, FPGAs are becoming a platform candidate to achieve energy efficient neural network processing. With a neural network oriented hardware design, FPGAs are able to implement high parallelism and make use of the properties of neural network computation to remove unnecessary logic. Algorithm researches also show that a NN model is able to be simplified in a hardware friendly way while not hurting the accuracy of the model. Therefore FPGAs are possible to achieve higher energy efficiency compared with CPU and GPU.

FPGA based accelerator designs are faced with two challenges in performance and flexibility:

- Current FPGAs usually support working frequency at 100-300MHz, which is much less than CPU and GPU. The FPGA's logic overhead for reconfigurability also reduces the overall system performance. Straight forward design on FPGA is hard to achieve high performance and high energy efficiency.
- Implementation of neural networks on FPGAs is much harder than that on CPUs or GPUs. Development framework like Caffe and Tensorflow for CPU and GPU is needed for FPGA.

Many researches on the above two problems have been carried out to implement energy efficient and flexible FPGA based neural network accelerators. In this paper, we summarize the techniques proposed in these works from the following aspects:

- We first give a simple model on FPGA based neural network accelerator performance to analyze the methodology in energy efficient design.
- We investigate current techniques for high performance and energy efficient neural network accelerator designs. We introduce the techniques in both software and hardware level and estimate the effect of these techniques.
- We compare state-of-the-art neural network accelerator designs to evaluate the techniques introduced and estimate the achievable performance of FPGA based accelerator design, which is at least 40× better energy efficient than current GPUs.
- We investigate state-of-the-art automatic design methods of FPGA based neural network accelerators.

The rest part of this paper is organized as follows: Section 2 introduces the basic operations of neural networks and the background of FPGA based NN accelerator. In section 3, we analyze the design target of NN accelerators and corresponding methods. Section 4 and section 5 review the techniques on neural network accelerator in NN model and hardware respectively. Section 6 compares existing designs and evaluate the techniques. Section 7 introduces the methods for a flexible accelerator design. Section 8 concludes this paper.

2 PRELIMINARY

Before discussing the system design for neural network acceleration, we first introduce the basic concepts of neural networks and the basic components of an FPGA-based accelerator design.

2.1 Neural Network

In this section, we introduce the basic functions in a neural network. In this paper, we only focus on the inference of NN, which means using a trained model to predict or classify new data. The

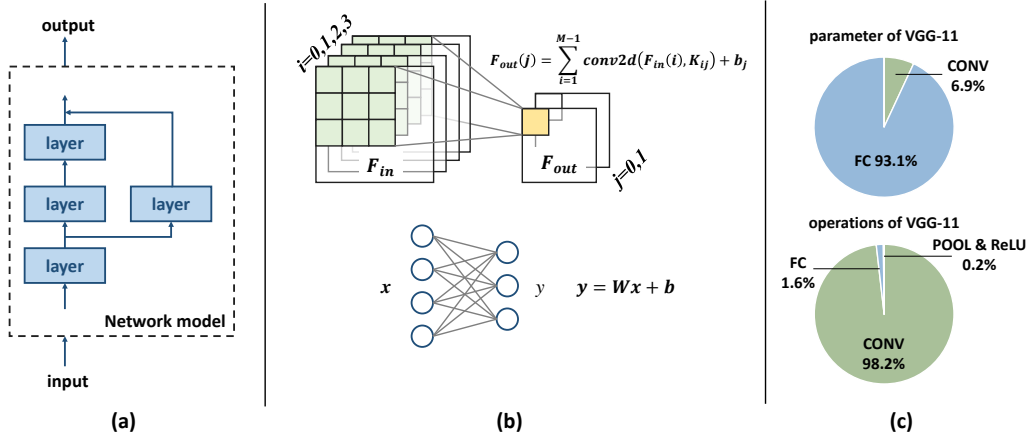


Fig. 1. (a) Computation graph of a neural network model. (b) CONV and FC layers in NN model. (c) CONV and FC layers dominates the computation and parameter of a NN model.

training process of NN is not discussed in this paper. A neural network model can be described as a directed graph shown in Figure 1(a). Each vertex of the graph denotes a layer which conducts operations on data from a previous layer or input and generates results to the next layer or output. We refer the parameter of each layer as weights and the input/output of each layer as activations through this paper.

Convolution (CONV) layers and fully connected (FC) layers are two common types of layers in NN models. The functions of these two layers are shown in Figure 1(b). CONV layers conduct 2D convolutions on a set of input feature maps F_{in} and add the results to get output feature maps F_{out} . FC layers receives a feature vector as input and conduct matrix-vector multiplications.

Besides CONV and FC layers, NN layers also have pooling, ReLU [22], concat [49], element-wise [16] and other types of layers. But these layers contributes little to the computation and storage requirement of a neural network model. Figure 1(c) shows the distribution of weights and operations in the VGG-11 model [47]. CONV and FC layers together contributes more than 99% of the network's weights and operations. So most of the neural network acceleration systems focus on these two types of layers.

2.2 FPGA-based Accelerator

In recent years, FPGA is becoming a promising solution for accelerating certain algorithms. Compared with CPU, GPU, and DSP platforms, for which the software and hardware are designed independently, FPGA enables the developers to implement only the necessary logic in hardware according to the target algorithm. By eliminating the redundancy in general hardware platforms, FPGAs are able to achieve higher efficiency. Application specific integrated circuits (ASICs) based solutions achieves even higher efficiency, but requires much longer development cycle and higher cost.

For FPGA-based neural network accelerator, a typical architecture of the system is shown in Figure 2(a). The system usually consists of a CPU host and an FPGA part. A pure FPGA chip usually works with a host PC/server through PCIe connections. SoC platforms (like the Xilinx Zynq Series) and Intel HARPv2 [12] platform integrates the host and the FPGA in the same chip or package. Both the host and the FPGA can work with their own external memory and access each others'

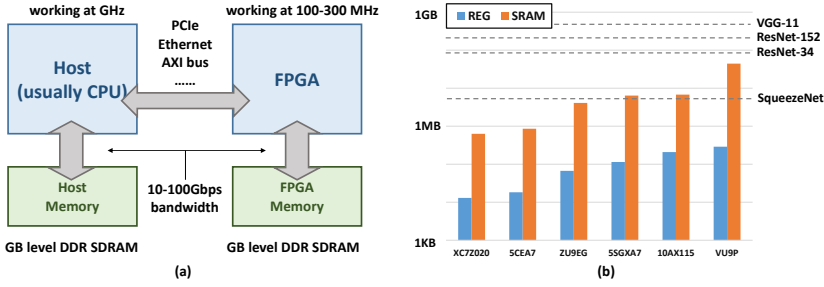


Fig. 2. (a) A typical structure of an FPGA based NN accelerator. (b) Comparison between NN model size and the storage on different FPGA chips.

memory through the connection. Most of the designs implements NN accelerator on the FPGA part and controls the accelerator with the software on the host.

Typical FPGA chips implement large on-chip storage units like registers and SRAMs, but still too small compared with NN models as shown in Figure 2(b). Common models implement 100-1000MB parameters while the largest available FPGA chip implements <50MB on-chip SRAM. This requires that external memory like DDR SDRAM is needed. The bandwidth and power consumption of DDR limits the system performance.

The computation capacity of FPGA is relatively higher. Common FPGAs implements hundreds to thousands of DSP units, each of which can compute 18×27 or 18×19 , achieving upto 10TFLOP/s (floating point operations per second) on the largest FPGAs. But for low-end FPGAs like Xilinx XC7Z020, this number is reduced to 20GFLOP/s, which is hard to support real-time video processing for applications on mobile platforms.

Even faced with the above challenges, researchers have proposed a series of optimization methods from algorithm to architecture to design high performance NN accelerators on FPGA, which will be discussed in the following sections of this paper.

3 DESIGN METHODOLOGY AND CRITERIA

Before going into the details of the techniques used for neural network accelerators, we first give an overview of the design methodology. In general, the design target of a neural network processing system includes the following two aspects: high speed (high throughput and lower latency), and high energy efficiency.

Speed. The throughput of an NN accelerator can be expressed by equation 1. **Peak performance**, measured in operations (multiplication or addition) per second, is achieved when all the computation units work every clock cycle. Utilization denotes the average ratio of working cycles of the computation units. The workload measures the number of operations in the target neural network. With a certain FPGA chip, the on-chip resource is limited. We can increase the peak performance by reducing the size of each computation unit and increasing the working frequency. Reducing the size of computation units can be achieved by simplifying the basic operations in neural network model, which may hurt the model accuracy and requires hardware-software co-design. Increasing working frequency, on the other hand is pure hardware design work. A high utilization ratio is kept by reasonable parallelism implementation and efficient memory system. Most of this part is affected by hardware design. But optimization on NN models can also reduce the storage requirement of a neural network model and benefits the memory system.

$$throughput = \frac{actual_performance}{workload} = \frac{peak_performance \times utilization}{workload} \quad (1)$$

Most of the FPGA based NN accelerators compute different inputs one at a time, which means the latency of the system is the reciprocal of throughput. The concurrent process of different inputs is usually realized with batch [28] or layer pipeline [24]. In these cases, the concurrency equals to the batch size or the number of pipeline stages. The latency of the accelerator can be described as equation 2.

$$latency = \frac{concurrency}{throughput} \quad (2)$$

So in this paper, we focus more on optimizing the throughput. As different accelerators may be evaluated on different NN models, a common criterion of speed is the *actual_performance*, which eliminates the effect of different workload to some extent.

Energy Efficiency. Energy efficiency is the actual performance within a certain power cost, i.e. the average number of operations can be executed within certain energy budget. This is usually measured in (OP/s/W) or (OP/J). Given a certain network model, the workload is fixed. Increasing the energy efficiency of a neural network accelerator means to reduce the total energy cost, E_{total} to process each input as shown in equation 3. This energy cost comes from 2 parts: computation and memory access, which is shown in equation 4.

$$energy_efficiency = \frac{E_{total}}{workload} \quad (3)$$

$$E_{total} \approx N_{op} \times E_{op} + N_{SRAM_access} \times E_{SRAM_access} + N_{DRAM_access} \times E_{DRAM_access} + E_{static} \quad (4)$$

The first item in equation 4 is the dynamic energy cost for computation. N_{op} denotes the number of operations processed. E_{op} denotes the average energy cost of each operation. Given a certain network and target FPGA platform, both N_{op} and E_{op} are fixed. For this part, researchers have been focusing on optimizing the NN models by quantization (narrowing the bit-width used for computation) to reduce E_{op} or sparsification (setting more weights to zeros) to skip the multiplications with these zeros to reduce N_{op} .

The second and third item in equation 4 is the dynamic energy cost for memory access. As shown in section 2.2, FPGA based NN accelerator usually works with external DRAM, we separate the memory access energy into DRAM part and SRAM part. N_{xx_access} denotes to total number of bytes to be accessed from memory. E_{xx_access} denotes the energy cost for accessing each byte. This part can also be reduced by quantization and sparsification, which helps reduce N_{xx_access} . Efficient on-chip memory system and scheduling method also helps to reduce N_{DRAM} . E_{xx_access} can hardly be reduced given a certain FPGA platform.

The fourth item E_{static} denotes the static energy cost of the system. This can hardly be improved given the FPGA chip and the scale of the design.

From the analysis of speed and energy, we see that neural network accelerator involves both optimization on NN models and hardware. In the following sections, we will introduce previous work in these two aspects respectively.

4 HARDWARE ORIENTED MODEL COMPRESSION

As introduced in section 3, the design of energy efficient and high speed neural network accelerator can benefit from the optimization of NN models. A larger NN model usually results in a higher

model accuracy. This means it is possible to tradeoff between the model accuracy and the hardware speed or energy cost. Neural network researchers are designing more efficient network models from AlexNet [22] to ResNet [16], SqueezeNet [19] and MobileNet [18]. The main differences between these networks are the size of and the connections between each layer. The basic operations are the same and hardly affect the hardware design. For this reason, we will not focus on these techniques in this paper. Other methods try to achieve the tradeoff by compressing existing NN models. They try to reduce the number of weights or reduce the number of bits used for each activation or weight, which help reduce the computation and storage complexity. Corresponding hardware designs can benefit from these NN model compression methods. In this section, we investigate these hardware oriented network model compression methods.

4.1 Data Quantization

One of the most commonly used method for model compression is the quantization on the weights and activations. The activations and weights of a neural network is usually represented by floating point data in common developing frameworks. Recent work try to replace this representation with low-bit fixed-point data or even a small set of trained values. On one hand, using less bits for each activation or weight helps reduce the bandwidth and storage requirement of the neural network processing system. On the other hand, using a simplified representation reduce the hardware cost for each operation. The benefit on hardware will be discussed in detail in section 5. Two kinds of quantization methods are discussed in this section: linear quantization and non-linear quantization.

4.1.1 Linear Quantization. Linear quantization finds the nearest fixed-point representation of each weight and activation. The problem of this method is that the dynamic range of floating point data greatly exceeds that for fixed point data. Most of the weights and activations will suffer from overflow or underflow. Qiu, et al. [40] finds that the dynamic range of the weights and activations in a single layer is much more limited and differs across different layers. Therefore they assign different fractional bit-widths to the weights and activations in different layers. To decide the fractional bit-width of a set of data, i.e. the activations or weights of a layer, the data distribution is first analyzed. A set of possible fractional bit-widths are chosen as candidate solutions. Then the solution with the best model performance on training data set is chosen. In [40], the optimized solution of a network is chosen layer by layer to avoid an exponential design space exploration. Guo, et al. [11] further improves this method by fine tuning the model after the fraction bit-width of all the layers are fixed.

The method of choosing certain fractional bit-width equals to scale the data with a scaling factor of 2^k . Li, et al. [23] scales the weights with trained parameter W^l for each layer and quantize the weights with 2-bit data, representing W^l , 0 and $-W^l$. The activations in this work is not quantized. So the the network still implements 32-bit floating point operations. Zhou, et al. [65] further quantize the weights of a layer with only 1 bit to $\pm s$, where $s = E(|w^l|)$ is the expectation of the absolute value of the weights of this layer. Linear quantization is also applied to the activations in this work.

4.1.2 Non-linear Quantization. Compared with linear quantization, non-linear quantization independently assigns values to different binary codes. The translation from a non-linear quantized code to its corresponding value is thus a look-up table. This kind of methods helps further reduce the bit-width used for each activation or weight. Chen, et al. [4] assign each of the weight to an item in the look-up table by a pre-defined hash function and train the values in look-up table. Han et al. [14] assigns the values in look-up table to the weights by clustering the weights of a trained model. Each look-up table value is set as the cluster center and further fine-tuned with training data set. This method is able to compress the weights of state-of-the-art CNN models to

4-bit without accuracy loss. Zhu, et al. [66] propose the ternary quantized network where all the weights of a layer are quantized to three values: W^n , 0, and W^p . Both the quantized value and the correspondance between weights and look-up table are trained. This method sacrifices less than 2% accuracy loss on ImageNet data set on state-of-the-art network models. The weight bit-width is reduced from 32-bit to 2-bit, which means about $16\times$ model size compression.

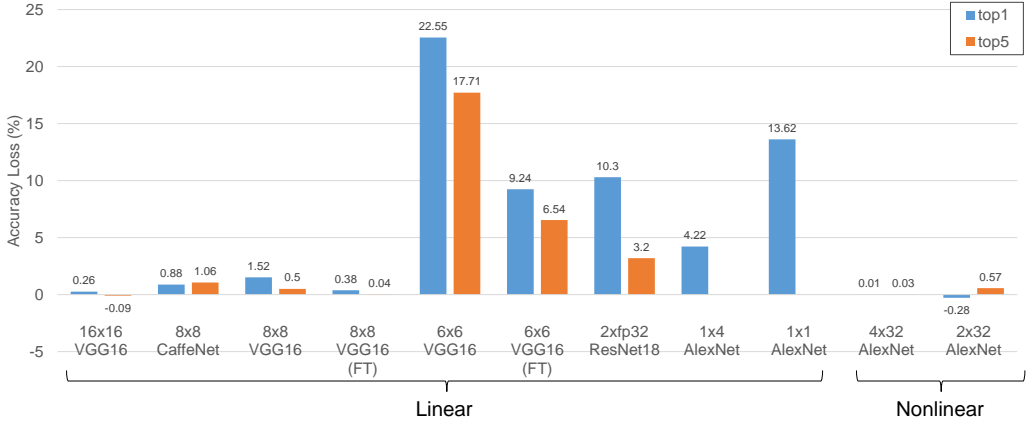


Fig. 3. Comparison between different quantization methods from [11, 14, 23, 40, 65, 66]. The quantization configuration is expressed as (weight bit-width) \times (activation bit-width). The "(FT)" denotes that the network is fine-tuned after a linear quantization.

4.1.3 Comparison. We compare some typical quantization methods from [11, 14, 23, 40, 65, 66] in Figure 3. All the quantization results are tested on ImageNet data set and the absolute accuracy loss compared with corresponding baseline floating point models is recorded. Comparing different methods on different models is a little bit unfair. But it still gives some insights. For linear quantization, 8-bit is a clear bound to ensure negligible accuracy loss. With 6 or less bits, using fine-tune or even training each weight from the beginning, will cause obvious accuracy degradation. If we require that 1% accuracy loss is within the acceptable range, linear quantization with at least 8×8 configuration and the listed non-linear quantization are available. We will further discuss the performance gain of quantization in section 5.

4.2 Weight Reduction

Besides narrowing the bit-width of activations and weights, another method for model compression is to reduce the number of weights. One kind of method is to approximate the weight matrix with a low rank representation. Qiu, et al. [40] compress the weight matrix W of an FC layer with singular value decomposition. An $m \times n$ weight matrix W is replaced by the multiplication of two matrices $A_{m \times p} B_{p \times n}$. For a sufficiently small p , the total number of weights is reduced. This work compress the largest FC layer of VGG network to 36% of its original size with 0.04% classification accuracy degradation. Zhang, et al. [63] use similar method for convolution layers and takes the effect of the following non-linear layer into the decomposition optimization process. The proposed method achieves $4\times$ speed up on state-of-the-art CNN model targeting at ImageNet, with only 0.9% accuracy loss.

Pruning is another kind of method to reduce the number of weights. This kind of methods directly remove the zeros in weights or remove those with small absolute values. The challenge in

pruning is the tradeoff between the ratio of zero weights and the model accuracy. One solution is the application of lasso method, which applies L1 normalization to the weights during training. Liu, et al. [26] apply the sparse group-lasso method on the AlexNet [22] model. 90% weights are removed after training with less than 1% accuracy loss. Another solution is to prune the zero weights during training. Han, et al. [14] directly removes the values in network with zero or small absolute value. The left weights are then fine-tuned on training set to recover accuracy. Experimental result on AlexNet show that 89% weights can be removed while keeping the model accuracy.

The hardware gain from weight reduction is the reciprocal of the compression ratio. According to the above results, the improvement from weight reduction is upto 10 \times .

5 HARDWARE DESIGN: EFFICIENT ARCHITECTURE

In this section, we investigate the hardware level techniques used in state-of-the-art FPGA based neural network accelerator design to achieve high performance and high energy efficiency. We classify the techniques into 3 levels: computation unit level, loop unrolling level, and system level.

5.1 Computation Unit Designs

Computation unit level design affect the peak performance of the neural network accelerator. With a certain FPGA chip, the available resource is limited. A smaller computation unit design means more computation units and higher peak performance. If the computation units are simplified or the actual number of computation number is reduced, then this also a carefully designed computation unit array can also increase the working frequency of the system and thus improve peak performance.

5.1.1 Low Bit-width Unit. Reduce the number of bit-width for computation is a direct way to reduce the size of computation units. The feasibility of using less bits comes from the quantization methods as introduced in section 4.1. Most of the state-of-the-art FPGA designs replace the 32-bit floating point units with fixed point units. Podili, et al. [38] implement 32-bit fixed point units for the proposed system. 16-bit fixed point units are widely adopted in [8, 24, 40, 57, 58]. ESE [13] adopts 12-bit fixed-point weight and 16-bit fixed point neurons design. Guo, et al. [11] use 8-bit units for their design on embedded FPGA. Recent work is also focusing on extremely narrow bit-width design. Prost-Boucle, et al. [39] implements 2-bit multiplication with 1 LUT for ternary network. Experiments in [37] shows that FPGA implementation of Binarized Neural Network (BNN) outperforms that on CPU and GPU. Though BNN suffers from accuracy loss, many designs explore the benefit of using 1 bit for computation [21, 25, 32, 34, 35, 50, 64].

The designs mentioned above are focused on computation units for linear quantization. For non-linear quantization, translating the data back to full precision for computation is still of high cost. Samragh, et al. [42] proposes the factorized coefficients based dot product implementation. As the possible values of weights are quite limited for non-linear quantization, the proposed computation unit accumulates the multiplier for each possible weight value and calculate the result as the weighted sum of the values in look-up table. In this way, the multiplication needed for one output neuron equals to the number of values in look-up table. The original multiplications are replaced by random addressed accumulations.

Most of the designs use a same bit-width through the process of a neural network. Qiu, et al. [40] finds that neurons and weights in FC layers can use less bits compared with CONV layers while the accuracy is maintained. Heterogeneous computation units are used in the designs of [10, 64].

The size of computation units of different bit-widths is compared in Table 1. Three kinds of implementations are tested: separate multiplier and adder with only logic resource on Xilinx FPGA, multiply-add function with DSP units on Xilinx FPGA, and multiply-add function with DSP units

on Altera FPGA The resource consumption is the synthesis result by Vivado 2018.1 targeting Xilinx XCKU060 FPGA and Quartus Prime 16.0 targeting Altera Arria 10 GX1150 FPGA. The pure logic modules and the floating point multiply and add modules are generated with IP core. The fixed point multiply and add modules are implemented with $A * B + C$ in verilog and automatically mapped to DSP by Vivado/Quartus.

We first give an overview of the size of the computation units by logic-only implementations. By compressing the weights and activations from 32-bit floating point number to 8-bit fixed point number, the multiplier and the adder are scaled down to about 1/10 and 1/50 respectively. Using 4-bit or smaller operations can bring further advantage but also incur significant accuracy loss as introduced in section 4.1.

Recent FPGAs consist of large number of DSP units, each of which implements hard multiplier, pre-adder and accumulator core. The basic pattern of NN computation, multiplication and sum, also fits into this design. So we also test the multiply and add function implemented with DSP units. Because of the different DSP architectures, we test on both Xilinx and Altera platforms. Compared with the 32-bit floating point function, fixed point functions with narrow bit-width still shows advantage. But for Altera FPGA, this advantage is not obvious as where the DSP units natively supports floating point operations.

Fixed point functions with 16-or-less-bit fixed point data are well fit into 1 DSP unit on either Xilinx or Altera FPGA. This shows that quantization hardly benefits the hardware if we use narrower bit-width like 8 or 4 in the aspect of computation. The problem is that the wide multipliers and adders in DSP units are under utilized in these cases. Nguyen, et al. [36] propose the design to implement two narrow bit-width fixed-point multiplication with a single wide bit-width fixed-point multiplier. In this design, two multiplications, AB and AC , are executed with in the form of $A(B << k + C)$. If k is sufficiently large, the bits for AB and AC does not overlap in the multiplication result and can be directly seperated. The design in [36] implements two 8-bit multiplications with one 25×18 multiplier, where k is 9. Similar method can be applied on other bit-width and DSPs.

Table 1. FPGA resource consumption comparison for multiplier and adder with different types of data.

	Xilinx Logic				Xilinx DSP			Altera DSP	
	multiplier		adder		multiply & add			multiply & add	
	LUT	FF	LUT	FF	LUT	FF	DSP	ALM	DSP
fp32	708	858	430	749	800	1284	2	1	1
fp16	221	303	211	337	451	686	1	213	1
fixed32	1112	1143	32	32	111	64	4	64	3
fixed16	289	301	16	16	0	0	1	0	1
fixed8	75	80	8	8	0	0	1	0	1
fixed4	17	20	4	4	0	0	1	0	1

5.1.2 Fast Convolution Unit. For CONV layers, the convolution operations can be accelerated by special algorithms. Discrete Fourier Transformation (DFT) based fast convolution is widely adopted in digital signal processing. Zhang, et al. [60] propose a 2D DFT based hardware design for efficient CONV layer execution. For an $F \times F$ filter convolved with $K \times K$ filter, DFT converts the $(F - K + 1)^2 K^2$ multiplications in sapce domain to F^2 complex multiplications in frequency domain. For a CONV layer with M input channel and N output channel, MN times of frequency domain multiplications are needed while only $(M + N)$ times DFT/IDFT are needed. The conversion of convolution kernels is once for all. So the domain conversion process are of low cost for CONV

layers. This technique does not work for CONV layers with stride>1 or 1×1 convolution. Ding, et al. [6] suggests that a block-wise circular constraint can be applied on the weight matrix. In this way, the matrix vector multiplication in FC layers are converted to a set of 1D convolutions and can further accelerated in frequency domain. This method can also be applied to CONV layers by treating the $K \times K$ convolution kernels as $K \times K$ matrices and is not limited by K or stride.

Frequency domain methods require complex number multiplication. Another kind of fast convolution involves only real number multiplication [55]. The convolution of a 2D feature map F_{in} with a kernel K using Winograd algorithm is expressed by equation 5.

$$F_{out} = A^T[(GF_{in}G^T) \odot (BF_{in}B^T)]A \quad (5)$$

G , B and A are transformation matrix which only related to the sizes of kernel and feature map. \odot denotes an element-wise multiplication of two matrices. For a 4×4 feature map convolved with 3×3 kernel, the transformation matrices are described as follows:

$$G = \begin{bmatrix} 1 & 0 & 0 \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \\ \frac{1}{2} & -\frac{1}{2} & \frac{1}{2} \\ 0 & 0 & 1 \end{bmatrix} \quad B = \begin{bmatrix} 1 & 0 & -1 & 0 \\ 0 & 1 & 1 & 0 \\ 0 & -1 & 1 & 0 \\ 0 & 1 & 0 & -1 \end{bmatrix} \quad A = \begin{bmatrix} 1 & 0 \\ 1 & 1 \\ 1 & -1 \\ 0 & -1 \end{bmatrix}$$

Winograd based methods are also limited by the kernel size and stride as DFT based methods. The most commonly used Winograd transformation is for 3×3 convolution in [28, 57].

The theoretical performance gain from fast convolution depends on the transformation kernel size. As DFT based method uses complex multiplication and costs more hardware, we estimate the theoretical gain according to the 6×6 Winograd used in [28], which is $4\times$.

5.1.3 Frequency Optimization Methods. All the above techniques introduced targets at increasing the number of computation units within a certain FPGA. Increasing the working frequency of the computation units also improves the peak performance.

To implement high parallelism, neural network accelerators usually implements matrix-vector multiplication or matrix-matrix multiplications rather than vector inner product as the basic operation. Different computation units share operators. Simply broadcast data to different computation units leads to large fan-out and high routing cost and thus reduce the working frequency. Wei, et al. [54] use the systolic array structure in their design. The shared data are transferred from one computation unit to the next in a chain mode. So the data is not broadcasted and only local connections between different computation units are needed. The drawback is the increase in latency. As the process of a neural network model is determined and the systolic structure is fully pipelined, the latency overhead can be fully covered.

Latest FPGAs support 700-900MHz DSP theoretical peak working frequency. But existing designs usually work at 100-300MHz [11, 30, 40, 58]. As claimed in [56], the working frequency is limited by the routing between on-chip SRAM and DSP units. The design in [56] use different working frequencies for DSP units and surrounding logic. Neighbour slices to each DSP unit are used as local RAMs to separate the clock domain. The prototype design in [56] achieves the peak DSP working frequency at 741MHz and 891MHz on FPGA chips of different speed grades. Yet this method is not adopted by a complete neural network accelerator design. Existing designs achieve 300MHz without this technique, so we estimate the theoretical hardware performance gain as $2\times$.

5.2 Loop Unrolling Strategies

CONV layers and FC layers contribute to most of the computations and storage requirment of a neural network as introduced in section 2. We express the CONV layer function in Figure 1(b) as nested loops in Algorithm 1. To make the code clear to read, we merge the loops along x and y

directions for feature maps and 2-D convolution kernels respectively. An FC layer can be treated as a CONV layer with feature map and kernel both of size 1×1 . Besides the loops in Algorithm 1, we also call the parallelism of the process of multiple inputs as a batch. This forms the batch loop.

Algorithm 1 Convolution Layer

Require: feature map F_{in} of size $M \times Y \times X$; convolution kernel Ker of size $N \times M \times K \times K$; bias vector b of size N

Ensure: feature map F_{out}

```

1: function CONV_LAYER( $F_{in}, Ker$ )
2:   Let  $F_{out} \leftarrow$  zero array of size  $N \times (Y - K + 1) \times (X - K + 1)$ 
3:   for  $n = 1; n < N; n++$  do                                      $\triangleright$  Output channel loop
4:     for  $m = 1; m < M; m++$  do                                      $\triangleright$  Input channel loop
5:       for each  $(y, x)$  within  $(Y - K + 1, X - K + 1)$  do          $\triangleright$  Feature map loop
6:         for each  $(ky, kx)$  within  $(K, K)$  do                      $\triangleright$  Kernel loop
7:            $F_{out}[n][y][x] += F_{in}[m][y - ky + 1][x - kx + 1] * K[n][m][ky][kx]$ 
8:        $F_{out}[n] += b[n]$ 
9:   return  $F_{out}$ 
  
```

To parallelize the execution of the loops, we unroll the loops and parallelize the process of a certain number of iterations on hardware. The number of the parallelized iterations on hardware is called the unroll parameter. Inappropriate unroll parameter selection may lead to serious hardware underutilization. Take a single loop as an example. Suppose the trip count of the loop is M and the parallelism is m . The utilization ratio of the hardware is limited by $m/M \lceil M/m \rceil$. If M is not divisible by m , then the utilization ratio is less than 1. Furthermore, in the case of NN process, the total utilization ratio will be the product of the utilization ratio along each of the loops.

For a CNN model, the loop dimension varies greatly among different layers. For a common network used on ImageNet classification like ResNet [16], the channel numbers vary from 3 to 2048, the feature map sizes vary from 224×224 to 7×7 , the convolution kernel sizes vary from 7×7 to 1×1 . Besides the under utilization problem, loop unrolling also affect the datapath and on-chip memory design. Thus loop unrolling strategy is a key feature for a neural network accelerator design.

Various work are proposed focusing on how the unroll parameter should be chosen. Zhang, et al. [59] propose the idea of unrolling the input channel and output channel loops and choose the optimized unroll parameter by design space exploration. Along these two loops, there is no input data cross dependency between neighbouring iterations. So no multiplexer is needed to route data from on-chip buffer to computation units. But the parallelism is limited as $7 \times 64 = 448$ multipliers. For larger parallelism, this solution is easy to suffer from the under utilization problem. Ma, et al. [30] further extends the design space by allowing parallelism on the feature map loop. The parallelism reaches $1 \times 16 \times 14 \times 14 = 3136$ multipliers. A shift register structure is used to route feature map pixels to the computation units.

The kernel loop is not chosen in the above work because kernel sizes vary greatly. Motamedi, et al [33] use kernel unrolling on AlexNet. Even with 3×3 unrolling for the 11×11 and 5×5 kernels, the overall system performance still reaches 97.4% of its peak performance for the convolution layers. For certain networks like VGG [47], only 3×3 convolution kernels are used. Qiu, et al. [40] use the line-buffer structure to achieve 3×3 sliding window function and fully parallelize the kernel loop. Another reason to unroll kernel loop is to achieve acceleration with fast convolution algorithms. Design in [60] implements fully parallelized frequency domain multiplication on 4×4

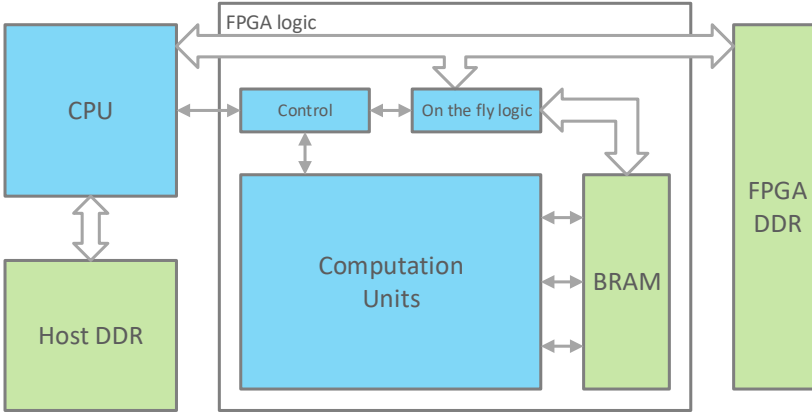


Fig. 4. Block graph of a typical FPGA based neural network accelerator system

feature map and 3×3 kernel. Lu, et al. [28] implement Winograd algorithm on FPGA with a dedicated pipeline for equation 5. The convolution of 3×3 kernel on 6×6 kernel is fully parallelized.

The above solutions are only for a single layer. But there is hardly a one-size-fits-all solution for a whole network, especially when we need high parallelism. Designs in [24, 27] propose fully pipelined structure with each layer a pipe stage. As each layer is executed with an independent part of hardware and each part is small, loop unrolling method can be easily chosen. This method is memory consuming because ping-pong buffers are needed between neighbouring layers for the feature maps. Design in [61] is similar but implemented on FPGA clusters to resolve the scalability problem. Shen, et al. [45] group the layers of a CNN by the loops' trip count and map each group onto one hardware module. Actually these solutions can be treated as unrolling the batch loop, because different inputs are processed in parallel on different layer pipe stages. The design in [28] implements parallelized batch both within a layer and among different layers. The drawback of batch parallel method is that the latency is higher compared with a *batch* = 1 design with a same parallelism.

Most of the current designs follow one of the above methods for loop unrolling. A special kind of design is for sparse neural network. Han, et al. [13] propose the ESE architecture for sparse LSTM network acceleration. Unlike processing a dense network, all the computation units will not work synchronously. This causes difficulty in sharing data between different computation units. ESE implements only the output channel (the output neurons of the FC layers in LSTM) loop unrolling within a layer to simplify hardware design and parallelize batch process.

5.3 System Design

A typical FPGA based neural network accelerator system is shown in Figure 4. The logic part of the whole system are denoted with the blue boxes. The host CPU issues workload or commands to the FPGA logic part and monitors its working status. On the FPGA logic part, a controller is usually implemented to communicate with host and generates control signals to all the other modules on FPGA. The controller can be an FSM or an instruction decoder. The on the fly logic part is implemented for certain designs if the data loaded from external memory needs preprocess. This module can be data arrangement module, data shifter [40], FFT module [60], etc. The computation units are as discussed in section 5.1 and section 5.2.

The memory hierarchy of the system mainly contains three parts, denoted as the green boxes in Figure 4: Host DDR, FPGA DDR and on-chip block RAM. For state-of-the-art network, the number of weights can reach up to 100M. Using even 8-bit or less bit-width quantization will result in tens of MB storage requirement. Most of the current FPGAs implements less than 10MB on-chip memory and 1-8GB external DDR integrated on board. So for common designs, a two level memory hierarchy is used with DDR and on-chip memory.

From system level, the performance of a neural network accelerator is limited by two factors: the on-chip computation resource and the off-chip memory bandwidth. Various researches have been proposed to achieve the best performance within a certain off-chip memory bandwidth. Zhang, et al. [59] introduce the roofline model in their work to analyze whether a design is memory bounded or computation bounded. An example of a roofline model is shown in Figure 5.

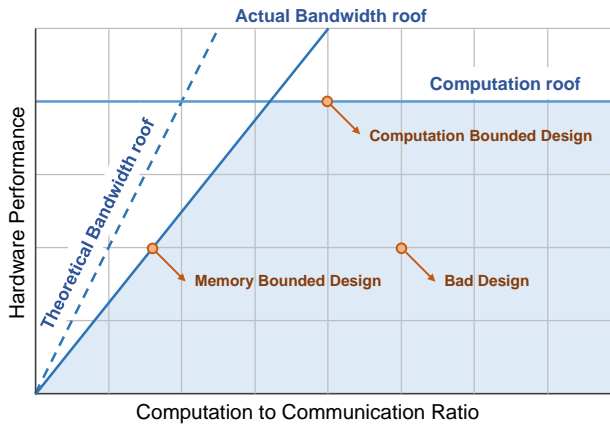


Fig. 5. An example of the roofline model. The shaded part denotes the valid design space given bandwidth and resource limitation.

The figure uses the computation to communication (CTC) ratio as x -axis and hardware performance as y -axis. CTC is the number of operations that can be executed with a unit size of memory access. Each hardware design can be treated as a point in the figure. So y/x equals to the bandwidth requirement of the design. Given a certain platform, the available bandwidth is limited and can be described as the theoretical bandwidth roof in Figure 5. But the actual bandwidth roof is below the theoretical roof because for DDR access, the achievable bandwidth depends on the data access pattern. Sequential DDR access achieves much higher bandwidth than random access. The other roof is the computation roof, which is limited by the available resource on FPGA.

So a higher CTC ratio means the hardware is more likely to achieve the computation bound. Increasing the CTC ratio also reduces DDR access, which greatly reduces the energy cost according to [17]. In section 5.2, we have discussed the loop unrolling strategies to increase the parallelism while reducing the waste of computation for a certain network. When the loop unrolling strategy is decided, the scheduling of the rest part of the loops decides how the hardware can reuse data with on-chip buffer. This involves loop tiling and loop interchange strategy.

Loop tiling is a higher level of loop unrolling. All the input data of a loop tile will be stored on-chip and the loop unrolling hardware kernel works on these data. A larger loop tile size means that each tile will be loaded from external memory to on-chip memory less times. Loop interchange strategy decides the processing order of the loop tiles. External memory access happens when the hardware is moving from one tile to the next. Neighbouring tile may share a part of data. For

example in a CONV layer, neighbouring tile can share input feature map or the weights. This is decided by the execution order of the loops.

In [30, 59], design space exploration is done on all the possible loop tiling sizes and loop orders. Many designs also explore the design space though some of the loop unrolling, tiling and loop order is already decided [33, 40]. Shen, et al. [46] also discuss the affect of batch parallelism over the CTC for different layers. This is a loop dimension not focused on in previous work.

All the above work give one optimized loop unrolling strategy and loop order for a whole network. Guo, et al. [11] implements flexible unrolling and loop order configuration for different layers with an instruction interface. The data arrangement in on-chip buffers is controlled through instructions to fit with different feature map sizes. This means the hardware can always fully utilize the on-chip buffer to use the largest tiling size according to on-chip buffer size. This work also propose the "back and forth" loop execution order to avoid total on-chip data refresh when a innermost loop finishes.

Alwani, et al. [2] address the external memory access problem by fusing two neighbouring layers together to avoid the intermediate result transfer between the two layers. This strategy helps reduce 95% off-chip data transfer with extra 20% on-chip memory cost. Even software program gains 2 \times speedup with this scheduling strategy.

Besides increasing CTC, increasing the actual bandwidth roof helps improve the attainable performance with a certain CTC ratio. This is achieved by regularize the DDR access pattern. Common data format in external memory includes *NCHW* or *CHWN*, where *N* means the batch dimension, *C* means the channel dimension, *H* and *W* means the feature map *y* and *x* dimension. Using any of these formats, a feature map tile may be cut into small data blocks stored in discontinuous addresses. Guan [8] suggest that a channel major storage format should be used for their design. This format avoids data duplication while long DDR access burst is ensured. Qiu et al. [40] propose a feature map storage format that arranges the $H \times W$ feature map into (HW/rc) tile blocks of size $r \times c$. So the write burst size can be increased from $c/2$ to $rc/2$.

6 EVALUTATION

In this section, we compare the performance of state-of-the-art neural network accelerator designs and try to evaluate the techniques mentiond in section 4 and section 5. We mainly reviewed the FPGA based designs published in the top FPGA conferences (FPGA, FCCM, FPL, FPT), EDA conferences (DAC, ASPDAC, DATE, ICCAD), architecture conferences (MICRO, HPCA, ISCA, ASPLOS) since 2015. Because of the diversity in the adopted techniques, target FPGA chips, and experiments, we need to tradeoff between the fairness of comparison and the number of designs we can use. In this paper, we pick the designs with: 1) whole system implementation; 2) experiments on real NN models with reported speed, power, and energy efficiency.

The designs used for comparison are listed in Table 2. For data format, the "INT A/B" means that activations are A-bit fixed point data and weights are B-bit fixed point data. We also investigate the resource utilization and draw advices to both accelerator designers and FPGA manufacturers.

Each of the designs in Table 2 drawn as a point in Figure 6, using $\log_{10}(\text{power})$ as x coordinate and $\log_{10}(\text{speed})$ as y axis. Therefore, $y - x = \log_{10}(\text{energy_efficiency})$. Besides the FPGA based designs, we also plot the GPU experimental results used in [11, 13] as standards to measure the FPGA designs' performance.

Bit-width Reduction. Among all the designs, 1-2 bit based designs show outstanding speed and energy efficiency. This shows that extremely low bitwidth is a promising solution for high performance design. As introduced in section 4.1, linear quantized 1-2 bit network models suffer from great accuracy loss, so this technique is better applied on simple tasks now. The energy

Table 2. Performance and resource utilization of state-of-the-art neural network accelerator designs

	Data Format	Speed (GOP/s)	Power (W)	Efficiency (GOP/J)	Resource(%)			FPGA chip
					DSP	logic	BRAM	
[3]	FP16	1382	45	30.7	97	58	92	Arria 10 GX1150
[13]	INT16/12	2520	41	61.5	54.4	88.6	87.7	XCKU060
[51]	INT16	12.73	1.75	7.27	94.54	66.64	6.07	XC7Z020
[60]	FP32	123.5	13.18	9.37	87.5	85.4	64	Stratix V
[62]	INT16	1790	37.46	47.8	91	43	53	GX1150
	FP32	866	41.73	20.75	87	-	46	
[30]	INT16/8	645.25	21.2	30.43	100	38	70	GX1150
[40]	INT16	136.97	9.63	14.22	89.2	83.5	86.7	XC7Z045
[48]	INT16/8	117.8	19.1	6.2	12.5	22	65.2	5SGSD8
[59]	FP32	61.62	18.61	3.3	80	61.3	50	XC7VX485T
[8]	INT16	364.4	25	14.6	65	25	46	5SGSMD5
[28]	INT16	2940.7	23.6	124.6	-	-	-	ZCU102
[38]	INT32	229	8.04	28.5	100	83.7	17.6	Stratix V
[34]	1bit	329.47	2.3	143.2	0.5	34.4	11.4	Zynq XC7Z020
[21]	2bit	410.22	2.26	181.51	40.5	82.7	37.7	Zynq XC7Z020
[32]	1bit	40770	48	849.38	-	-	-	GX1155
[24]	INT16	565.94	30.2	22.15	59.56	63.21	65.07	XC7VX690T
[27]	INT16/8	222.1	24.8	8.96	39.9	26.6	39.7	XC7VX690T
[61]	INT16	1280.3	160	8	-	-	-	XC7Z020+ XC7VX690T×6
[11]	INT8	84.3	3.5	24.1	87	84	89	XC7Z020
[57]	INT16	229.5	9.4	24.42	91.9	71	83.2	XC7Z045
[9]	FP32	7.26	19.63	0.37	42	65.31	52.04	XC7VX485T
[58]	INT16	354	26	13.6	78	81	42	XC7VX690T
[44]	INT16	431	25	17.1	42	56	52	XC7VX690T
		785	26	30.2	53	8.3	30	XCVU440

efficiency is improved by about 100× compared with 32-bit floating point designs. But there is still a great gap towards the 1000× improvement estimation. This shows that memory access becomes the bottleneck for 1-2 bit designs [21, 32, 34], which only scales linearly with the bit-width. INT16/8, INT16 and INT8 are commonly adopted. But the difference between these designs are not obvious. This is due to the fact that current FPGAs implement wide multipliers in DSPs like 18×25 or 18×18 . Using a less bits for computation will not benefit the DSPs. The double MAC technique by [36] serves as a solution but is not adopted in the listed designs.

Fast Convolution Algorithm. Among all the 16-bit designs, [28] achieves the best energy efficiency and the highest speed with the help of the 6×6 Winograd fast convolution, which is 1.7× faster and 2.6× energy efficient than the 16-bit design in [62]. The design in [60] achieves 2× speedup and 3× energy efficiency compared with [59] where both designs use 32-bit floating point data. Overall, the improvement does not match the estimation but can still reach 2-3×.

System Level Optimization. The overall system optimization is not well addressed in most of the work. As this is also related to the HDL design quality, we can just roughly evaluate the

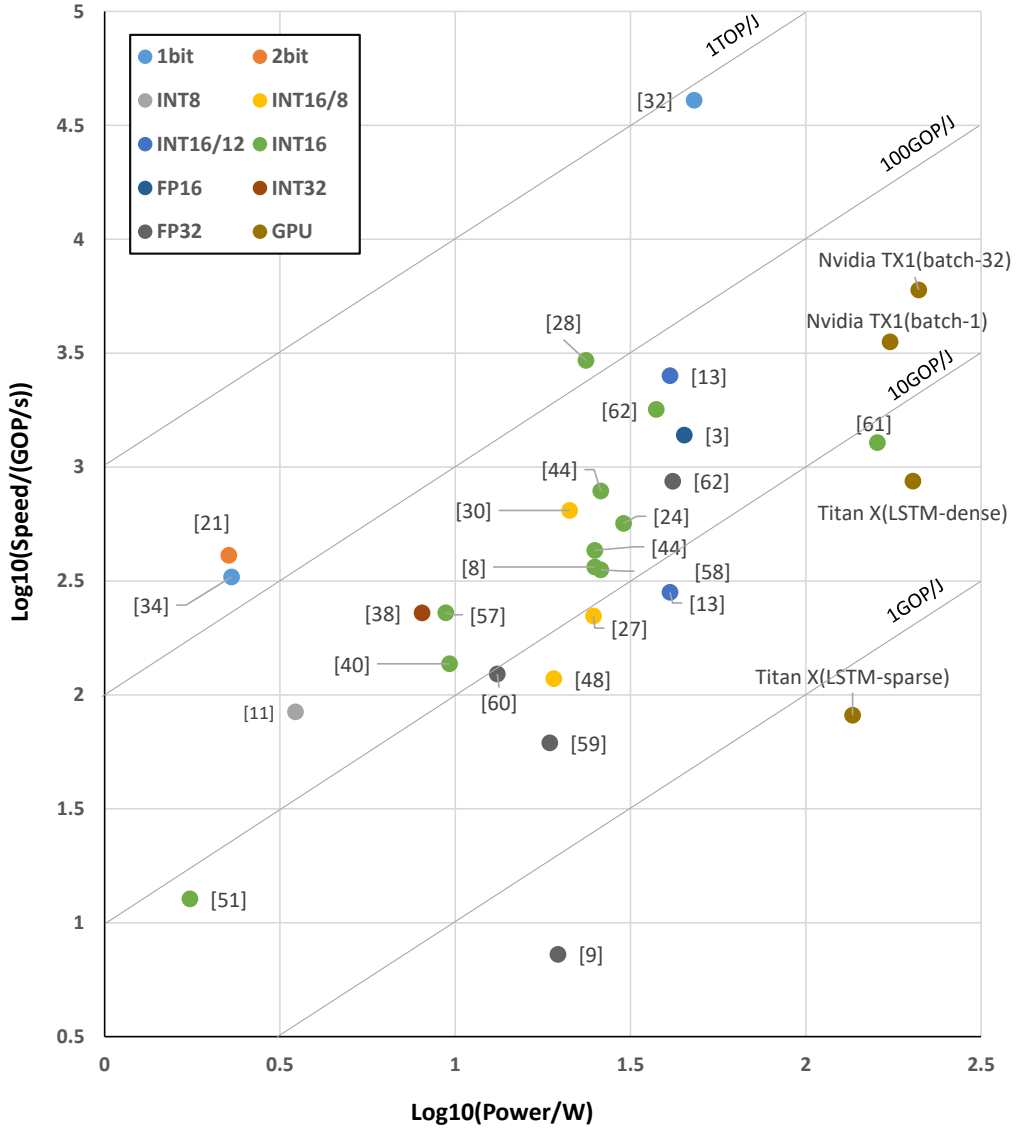


Fig. 6. A comparison between different designs on a logarithm coordinate of power and performance.

effect. Here we compare three designs[24, 27, 58] on the same XC7VX690T platform and try to evaluate the effect. All the three designs implement 16-bit fixed-point data format except that [27] uses 8-bit for weights. No fast convolution or sparsity is utilized in any of the work. Even though, [24] achieves 2.5 \times the energy efficiency of [27]. It shows that a system level optimization has a strong effect even comparable to the usage of fast convolution algorithm.

We also investigate the resource utilization of the designs in Table 2. Three kinds of resource are considered, DSP, BRAM, and logic. We plot the designs in Figure 7 using two of the utilization ratio as x and y coordinate. We draw the diagonal line of each figure to show the designs' preference on

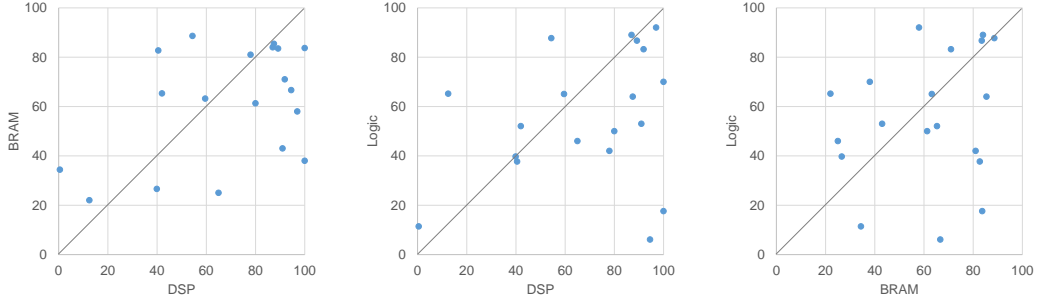


Fig. 7. Resource utilization ratio of different accelerator designs.

hardware resource. The BRAM-DSP figure shows a obvious preference of hardware on DSP over BRAM. Similar preference is also between DSP and logic. This indicates that current FPGA designs are more likely computation bounded. FPGA manufacturers targeting neural network applications can adjust the resource allocation accordingly.

Comparison with GPU. In general, FPGA based designs have achieved comparable energy efficiency to GPU with 10-100GOP/J. But the speed of GPUs still surpass FPGAs. Scaling up the FPGA based design is still a problem. Zhang, et al. [61] propose the FPGA cluster based solution using 16-bit fixed point computation. But the energy efficiency is worse than the other 16-bit fixed-point designs.

Here we estimate the achievable speed of an ideal design. We use the 16-bit fixed point design in [28] as a baseline, which is the best 16-bit fixed point design with both the highest speed and energy efficiency. 8-bit linear quantization can be adopted according to the analysis in section 4.1, which achieves another 2× energy efficiency and speedup by utilizing 1 DSP as 2 multipliers. Fast convolution and frequency optimization further improves the system by 4× and 2× respectively. Consider a sparse model which is similar to the one in [13] with 10% non-zero values. We can estimate a similar 6× improvement as [13]. In general about 12× speedup and better energy efficiency can be achieved, which means 36TOP/s speed with about 25W. This shows that it is possible to achieve over 1 magnitude higher energy efficiency on FPGA over 32-bit floating point process on GPU.

Two problems are left. The first problem is: does all the techniques: reuse of DSP, sparsification, quantization, fast convolution can work well together? Pruning a single element in a 2D convlution kernel is of no use for fast convolution because the 2D kernel is always processed together. So each 2D kernels should be pruned as a whole

The other problem is whether the utilization ratio can be kept when the parallelism in the accelerator scales up. Both of the reference designs we used for estimation [13, 28] uses batch mode. Further increasing the batch size or implementing layer pipeline introduces higher CTC ratio, which means the bandwidth may become the bottleneck. Otherwise, more flexible hardware should be designed to be better fit into different layers.

On the other hand, 1/2-bit designs already shows outstanding speed and energy efficiency. But current network accuracy is still far away from real applications.

7 DESIGN AUTOMATION AND FLEXIBILITY

In certain application senarios, various NN models are to be supported with the FPGA accelerator. Whether the accelerator can response to the change in network model promptly and keeps high

performance becomes a key feature. To address this problem, various researches have been carried out to automatically map a NN model to FPGA. Mainly two kinds of methods are used: hardware design automation and software design automation. Hardware design automation generates different hardware designs according to different NN models. Software design automation keeps a same accelerator and generates different inputs to the accelerator.

7.1 Hardware Design Automation

Hardware design automation is widely adopted in FPGA based accelerators because of the reconfigurability of FPGAs [5, 29, 31, 43, 51–53]. These proposed techniques focus on automatically generate the HDL design based on the network parameter. Difference between these methods is the selection of an intermediate level description of the network to cover the gap between high level network description and low level hardware design.

A straight forward way is no intermediate description. The design flow in [29] search the optimized parameter for a hand coded verilog template with the input network description and platform constraint. This method is similar to the optimization methods mentioned in section 5. DiCecco, et al. [5] uses similar idea but based on OpenCL model. This enables that the development tool be integrated with Caffe and one network can be executed on different platforms.

Venireis, et al. [52] describes the network model as a DFG in their design tool. Then the network computaion process is translated to hardware design with DFG mapping method.

DnnWeaver [43] use an virtual instruction set to describe a network. The network model is first translated into instruction sequence. Then the sequence is mapped as hardware FSM states but not executed like traditional CPU instructions.

Hardware design automation directly modifies the hardware design to support different networks. This means the hardware can always achieve the best performance on the target platform. This is suitable for FPGA because of its reconfigurability. It works in situations where network switching is not frequent and the reconfiguration overhead is not cared. For example, in the large scale cloud service, the change in network models can be covered by switching between different FPGA chips. So each of the FPGA do not need to be configured frequently.

7.2 Software Design Automation

Software design automation try to run different networks on a same hardware accelerator by simply changing the input, in most cases, an instruction sequence. The difference between these work is the granularity of instruction. At a lower level, Guo, et al. [11] propose the instruction set with only three kinds of instructions: LOAD, CALC, and SAVE. The granularity of the LOAD and SAVE instructions are the same as the data tiling size. Each CONV executes a set of 2-D convolutions given the feature map size encoded in the instruction. The channel number is fixed as the hardware unrolling parameter. At this level, the software compiler is able to carry out static scheduling and dynamic data reuse strategy according the certain layer.

Zhang et al. [58] uses a layer level instruction set. The control of a CNN layer is designed as a configurable hardware FSM. Compared with [11], this reduce the memory access for instruction access while increase the hardware cost on the configurable FSM.

Instruction based methods do not modify hardware and thus enables that the accelerator can switch between networks at run time. An example of the application senario is the real-time video processing system on a mobile platform. The process of a single frame can involve different networks if the task is complex enough. Reconfigure the hardware causes unacceptable overhead while instruction based methods can solve the problem if all the instructions of all the networks are prepared in memory.

7.3 Mixed Method

Wang, et al. [53] propose a design automation framework mixing the above two by both optimizing hardware design and compile software instructions. The hardware is first assembled with pre-defined HDL templates using the optimized hardware parameter. The data control flow of the computation process is controlled by software binaries, which is compiled according to the network description. It is possible that the hardware can be used for a new network by simply changing the software binaries.

8 CONCLUSION

In this paper, we review state-of-the-art neural network accelerator designs and summarize the techniques used. According to the evaluation result in section 6, with software hardware co-design, FPGA is able to achieve $13\times$ better energy efficiency than state-of-the-art GPU while using 30% power with conservative estimation. This shows that FPGA is a promising candidate for neural network acceleration. We also review the methods used for flexible accelerator design, which shows that current development flow is able to achieve both high performance and run-time network switch.

But there is still gap between current designs and the estimation. Combining all the techniques requires software-hardware co-design. Using quantization and weight reduction together while maintaining the performance is challenging. Scaling up the design is another problem. Future work should focus on solving these challenges. There is still $10\times$ potential performance gain from using $1/2$ bits for neuron and weight representation. Future work should try to improve the model accuracy in these cases.

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