

# [DL] A Survey of FPGA Based Neural Network Accelerator

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Recent researches on neural network have shown great improvement in computer vision over traditional algorithms based on handcrafted features and models. Neural network is now greatly adopted in regions like image, speech and video recognition. But the great computation and storage complexity of neural network based algorithms poses great difficulty on its application. CPU platforms are hard to offer enough computation capacity. While GPU platforms are highly parallelized, the energy efficiency is low. The high energy cost of GPU causes problems for a wide application of neural network.

To address the above problems, various FPGA based hardware accelerators for neural networks have been proposed. Specialized hardware are designed to achieve high speed and low power neural network process. In this paper, we give an overview of previous work on neural network accelerators based on FPGA and summarize the main techniques used. Investigation from software to hardware, from circuit level to system level is carried out to complete analysis of FPGA based neural network accelerator design and serves as a guide to future work.

Additional Key Words and Phrases: FPGA, Neural Network

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## 1 INTRODUCTION

Recent research on Neural Network (NN) is showing great improvement over traditional algorithms in computer vision. Various network models, like convolutional neural network (CNN), recurrent neural network (RNN), have been proposed for image, video, and speech process. CNN [10] improves the top-5 image classification accuracy on ImageNet [13] dataset from 73.8% to 84.7% and further helps improve object detection [3] with its outstanding ability in feature extraction. RNN [6] achieves state-of-the-art word error rate on speech recognition. In general, NN features a high fitting ability to a wide range of pattern recognition problems. This makes NN a promising candidate to many artificial intelligence applications.

But the computation and storage complexity of NN models are high. The research on NN is also increasing the size of NN models. The largest neural network model for an  $224 \times 224$  image classification requires upto 39 billion floating point operations (FLOP) and more than 500MB model parameters [14]. As the computation complexity is proportional to the input image size, processing images with higher resolutions may need more than 100 billion operations.

Traditional hardware platforms are not suitable for neural network process. A common CPU can perform 10-100G FLOP per second, and the power efficiency is usually below 1GOPS/W. So CPUs neither meet the high performance requirements in cloud applications nor the low power

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requirements in mobile applications. In contrast, GPUs offer upto 10TOP/s peak performance and is a good choice for high performance neural network applications. Development frameworks like Caffe [9] and Tensorflow [1] also offers easy-to-use interfaces which makes GPU the first choice of neural network acceleration. But GPUs are power consuming and thus not suitable for mobile applications.

On the other hand, FPGA is becoming a candidate to implement energy efficient neural network accelerator. With a specific hardware design, FPGAs are able to implement high parallelism and make use of the properties of neural network computation to remove unnecessary logic. Therefore FPGAs are possible to achieve higher energy efficiency compared with CPU and GPU.

But FPGA based accelerator designs are still faced with two problems:

- Current FPGAs usually support working frequency at 100-300MHz, which is much less than CPU and GPU. The FPGA's logic overhead for reconfigurability also reduces the overall system performance. Straight forward design on FPGA is hard to achieve high performance and high energy efficiency.
- Implementation of neural networks on FPGAs is much harder than that on CPUs or GPUs. Development framework like Caffe and Tensorflow for CPU and GPU is needed for FPGA.

Many researches on the above two problems have been carried out for energy efficient and flexible FPGA based neural network accelerator. In this paper, we summarize the techniques proposed in these work. Specifically, we will introduce the techniques from the following aspects:

- We investigate current techniques for high performance and energy efficient neural network accelerator designs. Techniques in both software level and hardware level are evaluated.
- We investigate state-of-the-art automatic design methods of FPGA based neural network accelerators.

The rest part of this paper is organized as follows:

## 2 PRELIMINARY ON NEURAL NETWORK

In this section, we introduce the basic operations included in neural network algorithms. Neural network is a bio-inspired model, which usually includes several layers. Each layer receives input from a set of neurons and output a set of neurons. The synapses connecting input and output neurons are modeled as parameters, which is referred to as weights in this paper. In the rest part of this section, we introduce different types of layers in neural network models.

**Fully connected (FC) layer** implements a connection between every input neuron and output neuron with a weight. This type of layer is adopted in both CNN and RNN. The input and output neurons of an FC layer are two vectors  $\mathbf{x}$  and  $\mathbf{y}$ . The weights of this layer can be modeled as a matrix  $W$ . A bias vector  $\mathbf{b}$  is added to each of the output neuron. The computation of this layer is described as equation 1.

$$\mathbf{x} = W\mathbf{y} + \mathbf{b} \quad (1)$$

**Convolution (CONV) layer** is used for 2-d neuron process. This is commonly adopted in CNN for image process. The input and output neurons of this layer can be described as sets of 2-d feature maps,  $F_{in}$  and  $F_{out}$ . Each feature map is denoted as a channel. A CONV layer implements a 2-d convolution kernel  $K_{ij}$  for each input and output channel pair and a bias scalar  $b_i$  for each output channel. The computation of a CONV layer with  $M$  input channels and  $N$  output channels can be described as equation 2.

$$F_{out}(j) = \sum_{i=0}^{M-1} \text{conv2d}(F_{in}(i), K_{ij}) + b_j, j = 0, 1, \dots, N-1 \quad (2)$$

There are varieties of 2-d convolutions in CONV layer. Usually standard convolution with padding is used when the kernel size is  $3 \times 3$ . For larger kernels like  $5 \times 5$  and  $7 \times 7$ , a stride larger than 1 is usually used to reduce the number of operation. Recent work is also using  $1 \times 1$  convolution kernels [7, 8].

**Non-linear layer** applies a non-linear function on each of the input neurons. Sigmoid function and tanh function are commonly adopted in early models and are still used in RNN for acoustic or speech recognition. Rectified linear unit (ReLU) [10] is the adopted in many state-of-the-art models. This function maintains the positive neurons and filters negative neurons as zero. Varieties of ReLU are also used, such as PReLU and Leaky ReLU [15].

**Pooling layer** is also used for 2-d neuron process like CONV layer. A pooling layer downsamples each of the input channel respectively, which helps reduce feature dimension. There are two kinds of down sampling method: average pooling and max pooling. Average pooling splits a feature map into small windows, i.e.  $2 \times 2$  windows, and finds the average value of each window. Max pooling method finds the maximum value in each window. Common window size includes  $2 \times 2$ , stride=2 and  $3 \times 3$ , stride=2.

**Element-wise layer** is usually used in RNN and is introduced in ResNet [7]. This layer receives two neuron vectors of the same size and applies element-wise operations on corresponding neurons of the two vectors. In ResNet, this layer is element-wise addition. For RNN, this layer can be element-wise subtraction or multiplication.

Among these types of layers, FC layer and CONV layer contributes to most of the computation and storage in neural networks. In the following sections, both software level and hardware level designs focus on these two types of layers.

### 3 SOFTWARE DESIGN: MODEL COMPRESSION

The design of energy efficient and high performance neural network accelerator involves software and hardware co-design. In this section, we investigate the software level network model compression methods. Many researches on this topic have been proposed to reduce the number of weights or reduce the number of bitwidth for the neurons and weights, which helps reduce the computation and storage complexity. But these methods can also sacrifice the model accuracy. The trade-off between model compression and model accuracy loss is discussed in this section.

#### 3.1 Data Quantization

One of the most commonly used method for model compression is the quantization on the weights and neurons. The neurons and weights of a neural network is usually represented by floating point data in common developing frameworks. Recent work try to replace this representation with low-bit fixed-point data or even a small set of trained values. On one hand, using less bits for each neuron or weight helps reduce the bandwidth and storage requirement of the neural network processing system. On the other hand, using a simplified representation reduce the hardware cost for each operation. The benefit on hardware will be discussed in detail in section ???. Two kinds of quantization methods are discussed in this section: linear quantization and non-linear quantization.

**3.1.1 Linear Quantization.** Linear quantization finds the nearest fixed-point representation of each weight and neuron. The problem of this method is that the dynamic range of floating point data greatly exceeds that for fixed point data. Most of the weights and neurons will suffer from overflow or underflow. Qiu, et al. [12] finds that the dynamic range of the weights and neurons in a single layer is much more limited and differs across different layers. Therefore they assign different fractional bit-widths to the weights and neurons in different layers. To decide the fractional bit-width of a set of data, i.e. the neurons or weights of a layer, the data distribution is first analyzed.

A set of possible fractional bit-widths are chosen as candidate solutions. Then the solution with the best model performance on training data set is chosen. In [12], the optimized solution of a network is chosen layer by layer to avoid an exponential design space exploration. Guo, et al. [4] further improves this method by fine tuning the model after the fraction bit-width of all the layers are fixed.

The method of choosing certain fractional bit-width equals to scale the data with a scaling factor of  $2^k$ . Li, et al. [11] scales the weights with trained parameter  $W^l$  for each layer and quantize the weights with 2-bit data, representing  $W^l$ , 0 and  $-W^l$ . Zhou, et al. [16] further quantize the weights of a layer with only 1 bit to  $\pm s$ , where  $s = E(|w^l|)$  is the expectation of the absolute value of the weights of this layer.

**3.1.2 Non-linear Quantization.** Compared with linear quantization, non-linear quantization independently assigns values to different binary code. The translation from a non-linear quantized code to its corresponding value is thus a look-up table. This kind of methods helps further reduce the bit-width used for each neuron or weight. Chen, et al. [2] assign each of the weight to an item in the look-up table by a pre-defined hash function and train the values in look-up table. Han et al. [5] assigns the values in look-up table to the weights by clustering the weights of a trained model. Each look-up table value is set as the cluster center and further fine-tuned with training data set. This method is able to compress the weights of state-of-the-art CNN models to 4-bit without accuracy loss. Zhu, et al. [17] propose the ternary quantized network where all the weights of a layer are quantized to three values:  $W^n$ , 0, and  $W^p$ . Both the quantized value and the correspondance between weights and look-up table are trained. This method sacrifices less than 2% accuracy loss on ImageNet data set on state-of-the-art network models. The weight bit-width is reduced from 32-bit to 2-bit, which means about  $16\times$  model size compression.

Experimental results of this method on VGG-16 model [14] are shown in Figure ?? according to [12] and [4]. 16-bit fixed point data format shows a similar performance to the 32-bit floating point baseline. By introducing different fractional bit-widths for different layers, 8-bit fixed point format also introduces negligible accuracy loss. Further narrowing the bit-width to 6 causes an obvious accuracy loss.

### 3.2 Network Pruning

Network pruning reduces the number of connections between input and output neurons.

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