Reviewer: 1

Comments to the Author

The writing is still very poor. This paper will need a lot of copy editing. We can start with the title:

A Survey of FPGA Based Neural Network Inference Accelerator

should be

A Survey of FPGA-Based Neural Network Inference Accelerators

Following up with another response to Reviewer 3. If "Most of the techniques introduced are suitable to both CNN and RNN or other state-of-the-art networks" then it would be good to discuss this some more as the paper seems to be more about CNNs.

Section 3:

This section was changed to address comments of Reviewer 3, but I now find it worse that it was before. Before, there was at least some textual discussion that made more sense. Now there are just equations with little to no discusson about the equations and what they are showing. You have to use Table 1 to decipher what the equations mean. Table 1 is still a good idea, but you should keep the textual descriptions and formalize them with the equations.

p 11.16: "... there is still 1.3 1.5x gap ..." Should this be "... there is still 1.3 - 1.5x gap ..."?

p 11.17: Fig. 7. You have not addressed my concern. You make comments on BRAM/DSP and Logic/DSP. You still do not comment on the Logic/BRAM chart. I previously said that if you do not comment about it in the text, it should be removed. However, I would say that you need it and the text should make an observation about what that chart shows.

Reviewer: 2

Comments to the Author

(There are no comments.)

Reviewer: 3

Comments to the Author

Do include a citation to Stylianos I. Venieris, Alexandros Kouris, Christos-Savvas Bouganis: Toolflows for Mapping Convolutional Neural Networks on FPGAs: A Survey and Future Directions. ACM Comput. Surv. 51(3): 56:1-56:39 (2018)