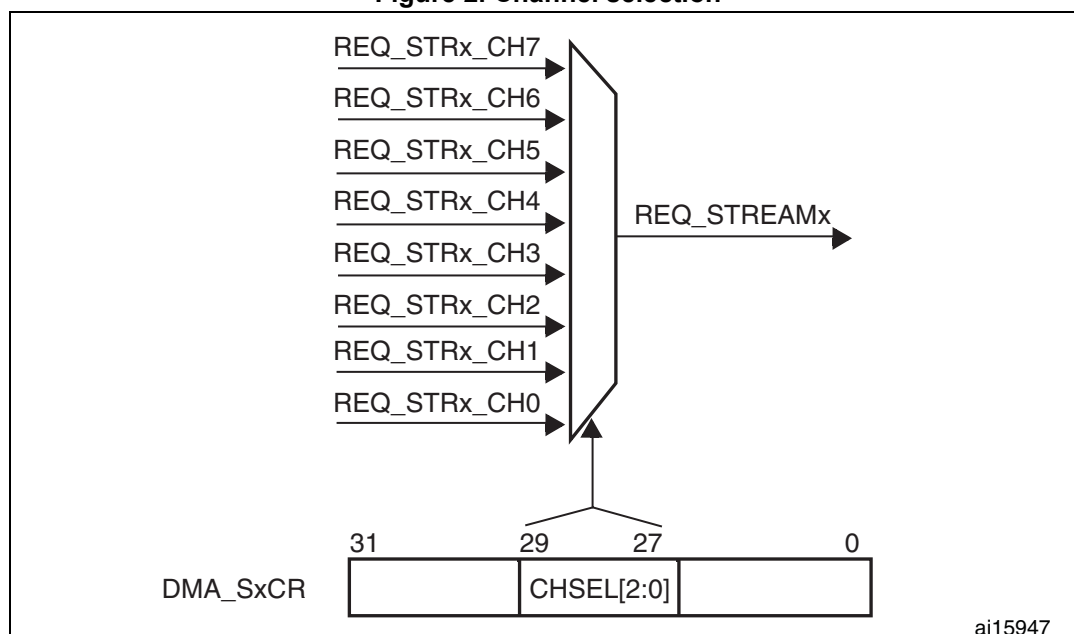


Figure 2. Channel selection



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**Note:** Only one channel/request can be active at the same time in a stream.  
 More than one enabled DMA stream must not serve the same peripheral request.

[Table 2](#) and [Table 3](#) show the possible configurations of DMA streams/channels versus peripheral requests for all the supported products except STM32F401, which is described in [Table 4](#) and [Table 5](#).

Table 2. DMA1 request mapping

Peripheral requests	Stream 0	Stream 1	Stream 2	Stream 3	Stream 4	Stream 5	Stream 6	Stream 7
<u>Channel 0</u>	SPI3_RX	-	SPI3_RX	SPI2_RX	SPI2_TX	SPI3_TX	-	SPI3_TX
Channel 1	I2C1_RX	-	TIM7_UP		TIM7_UP	I2C1_RX	I2C1_TX	I2C1_TX
Channel 2	TIM4_CH1	-	I2S3_EXT_RX	TIM4_CH2	I2S2_EXT_TX	I2S3_EXT_TX	TIM4_UP	TIM4_CH3
Channel 3	I2S3_EXT_RX	TIM2_UP TIM2_CH3	I2C3_RX	I2S2_EXT_RX	I2C3_TX	TIM2_CH1	TIM2_CH2 TIM2_CH4	TIM2_UP TIM2_CH4
<u>Channel 4</u>	UART5_RX	USART3_RX	UART4_RX	USART3_TX	UART4_TX	USART2_RX	USART2_TX	UART5_TX
Channel 5	UART8_TX <sup>(1)</sup>	UART7_TX <sup>(1)</sup>	TIM3_CH4 TIM3_UP	UART7_RX <sup>(1)</sup>	TIM3_CH1 TIM3_TRIG	TIM3_CH2	UART8_RX <sup>(1)</sup>	TIM3_CH3
Channel 6	TIM5_CH3 TIM5_UP	TIM5_CH4 TIM5_TRIG	TIM5_CH1	TIM5_CH4 TIM5_TRIG	TIM5_CH2	-	TIM5_UP	-
Channel 7	-	TIM6_UP	I2C2_RX	I2C2_RX	USART3_TX	DAC1	DAC2	I2C2_TX

1. These requests are available on STM32F42xx and STM32F43xx only.

Table 3. DMA2 request mapping

Peripheral requests	Stream 0	Stream 1	Stream 2	Stream 3	Stream 4	Stream 5	Stream 6	Stream 7
Channel 0	ADC1	SAI1_A <sup>(1)</sup>	TIM8_CH1 TIM8_CH2 TIM8_CH3	SAI1_A <sup>(1)</sup>	ADC1	SAI1_B <sup>(1)</sup>	TIM1_CH1 TIM1_CH2 TIM1_CH3	-
Channel 1	-	DCMI	ADC2	ADC2	SAI1_B <sup>(1)</sup>	SPI6_TX <sup>(1)</sup>	SPI6_RX <sup>(1)</sup>	DCMI
Channel 2	ADC3	ADC3	-	SPI5_RX <sup>(1)</sup>	SPI5_TX <sup>(1)</sup>	CRYP_OUT	CRYP_IN	HASH_IN
Channel 3	SPI1_RX	-	SPI1_RX	SPI1_TX	-	SPI1_TX	-	-
Channel 4	SPI4_RX <sup>(1)</sup>	SPI4_TX <sup>(1)</sup>	USART1_RX	SDIO	-	USART1_RX	SDIO	USART1_TX
Channel 5	-	USART6_RX	USART6_RX	SPI4_RX <sup>(1)</sup>	SPI4_TX <sup>(1)</sup>	-	USART6_TX	USART6_TX
Channel 6	TIM1_TRIG	TIM1_CH1	TIM1_CH2	TIM1_CH1	TIM1_CH4 TIM1_TRIG TIM1_COM	TIM1_UP	TIM1_CH3	-
Channel 7	-	TIM8_UP	TIM8_CH1	TIM8_CH2	TIM8_CH3	SPI5_RX <sup>(1)</sup>	SPI5_TX <sup>(1)</sup>	TIM8_CH4 TIM8_TRIG TIM8_COM

1. These requests are available on STM32F42xx and STM32F43xx only.

[Table 4](#) and [Table 5](#) show the possible configurations of DMA streams/channels versus peripheral requests for STM32F401 products.

Table 4. DMA1 request mapping for STM32F401

Peripheral requests	Stream 0	Stream 1	Stream 2	Stream 3	Stream 4	Stream 5	Stream 6	Stream 7
Channel 0	SPI3_RX	-	SPI3_RX	SPI2_RX	SPI2_TX	SPI3_TX	-	SPI3_TX
Channel 1	I2C1_RX	I2C3_RX	-	-	-	I2C1_RX	I2C1_TX	I2C1_TX
Channel 2	TIM4_CH1	-	I2S3_EXT_RX	TIM4_CH2	I2S2_EXT_TX	I2S3_EXT_TX	TIM4_UP	TIM4_CH3
Channel 3	I2S3_EXT_RX	TIM2_UP TIM2_CH3	I2C3_RX	I2S2_EXT_RX	I2C3_TX	TIM2_CH1	TIM2_CH2 TIM2_CH4	TIM2_UP TIM2_CH4
Channel 4	-	-	-	-	-	USART2_RX	USART2_TX	-
Channel 5	-	-	TIM3_CH4 TIM3_UP	-	TIM3_CH1 TIM3_TRIG	TIM3_CH2	-	TIM3_CH3
Channel 6	TIM5_CH3 TIM5_UP	TIM5_CH4 TIM5_TRIG	TIM5_CH1	TIM5_CH4 TIM5_TRIG	TIM5_CH2	I2C3_TX	TIM5_UP	-
Channel 7	-	-	I2C2_RX	I2C2_RX	-	-	-	I2C2_TX