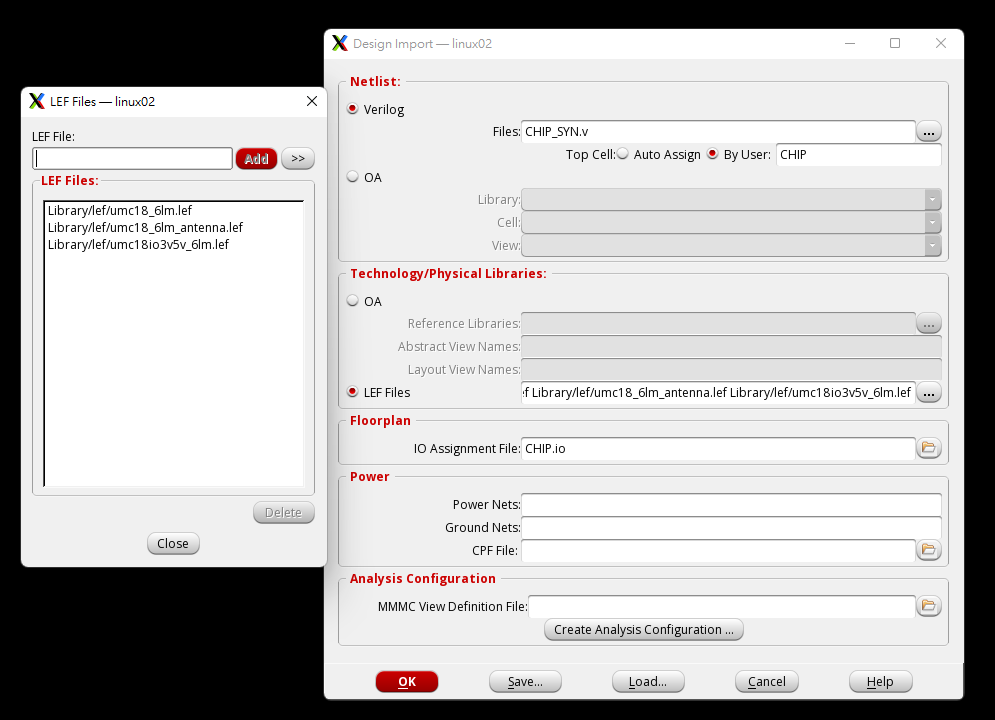
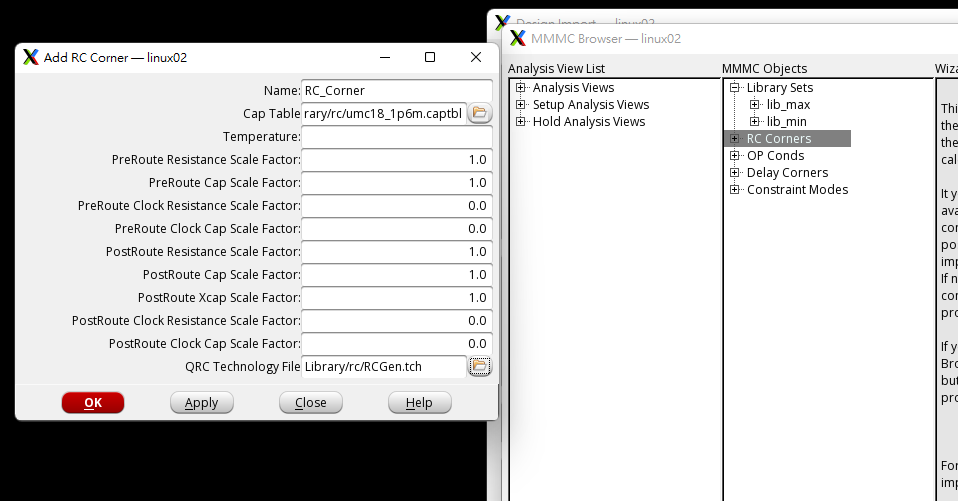
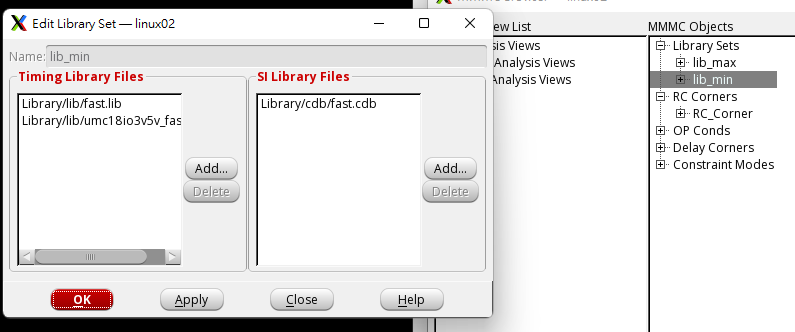
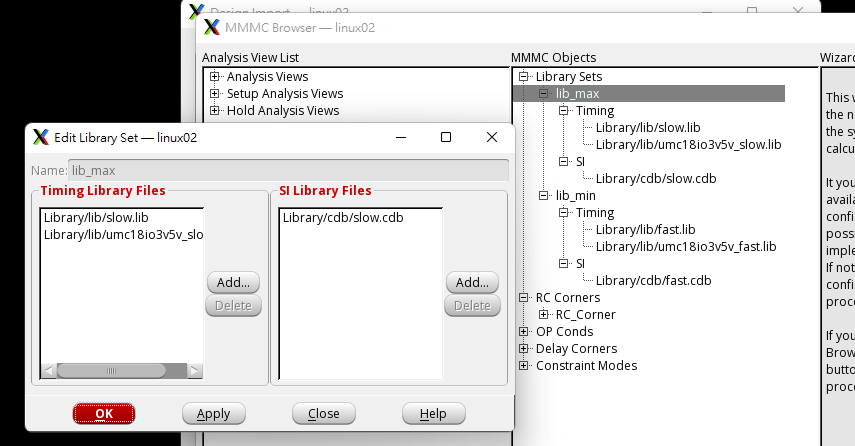
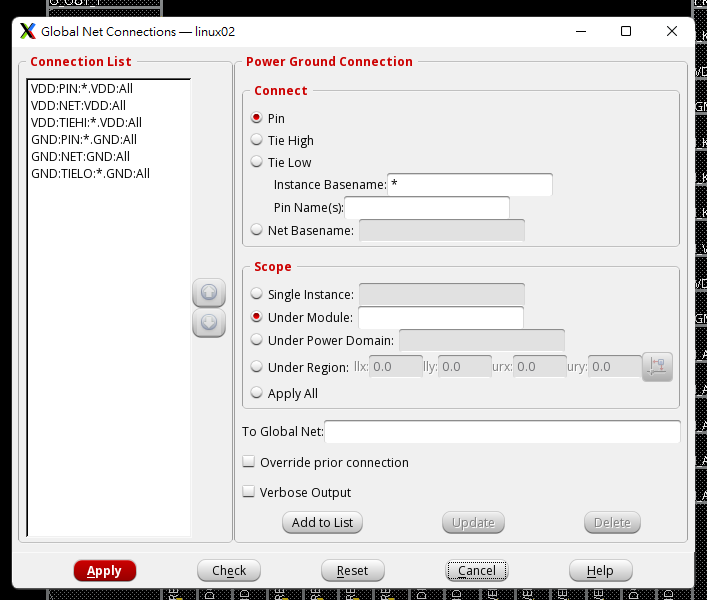
**2. Reading Cell Library information and Netlist for APR**



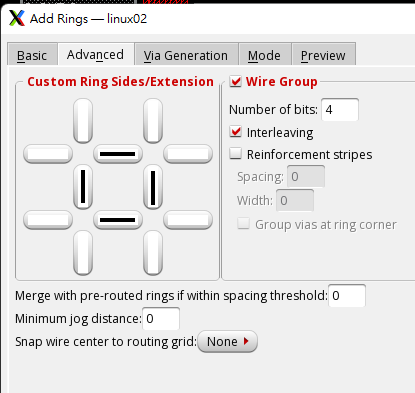
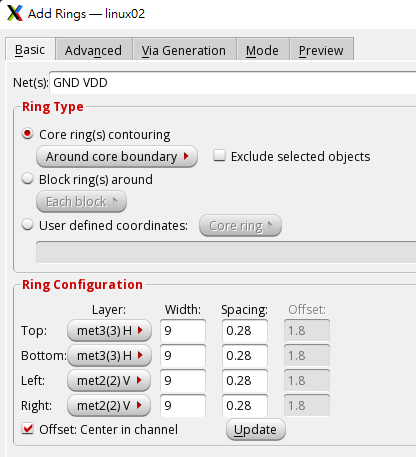




**4. Connect/Define Global Net**

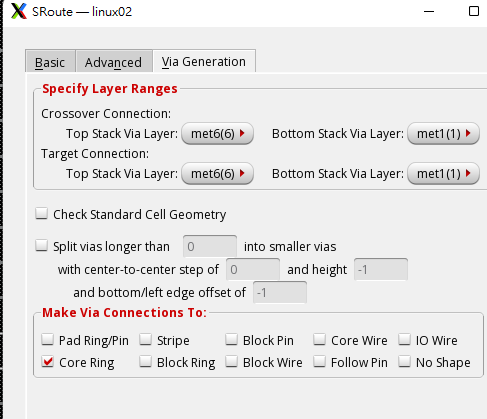
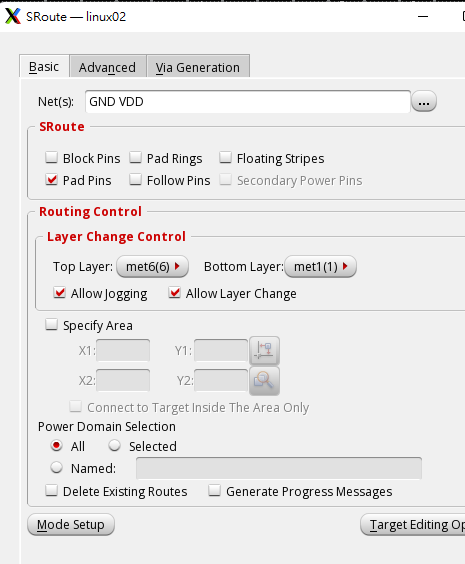


**5. Power Planning (Add Core Power Rings)**

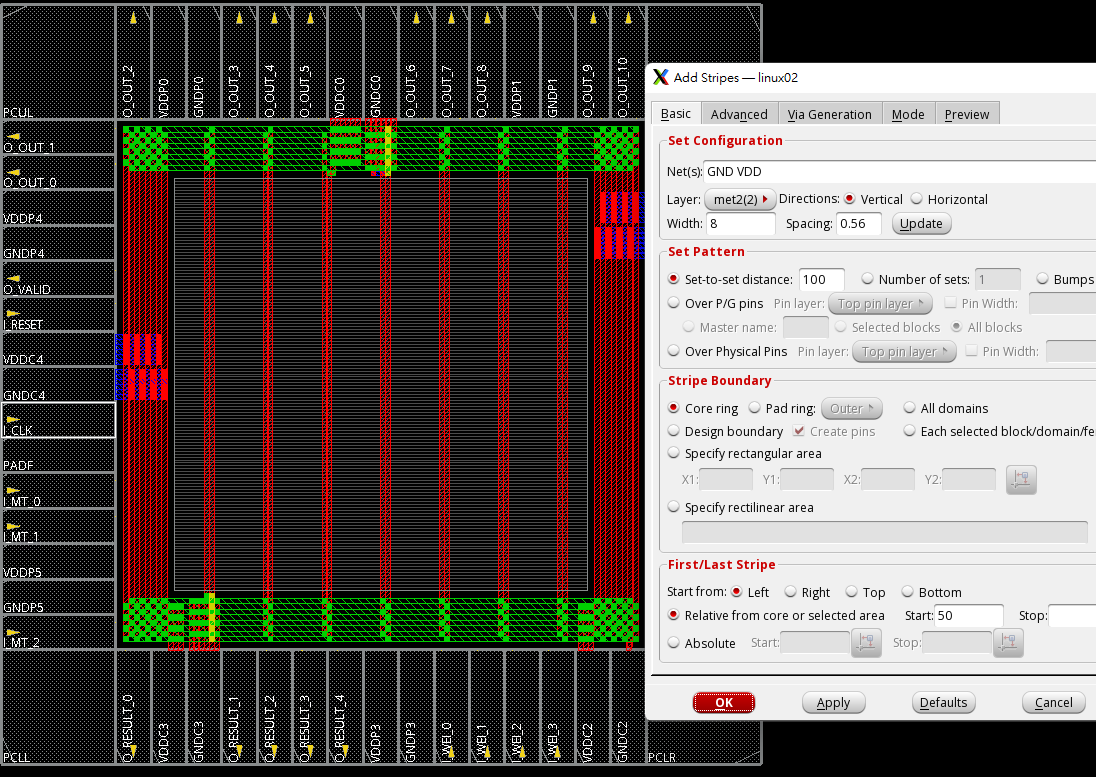


Pass block ring because no hard marco

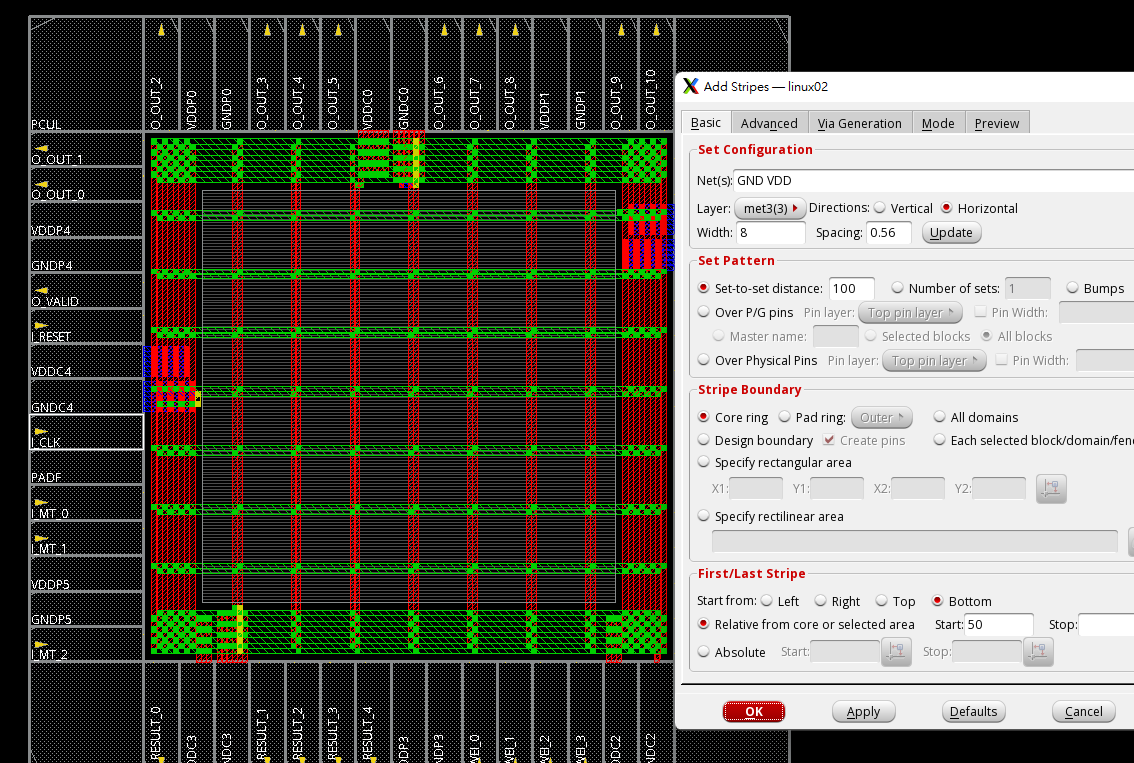
**7. Connect Core Power Pin**



**8. Power Planning (Add Stripes)**



vertical

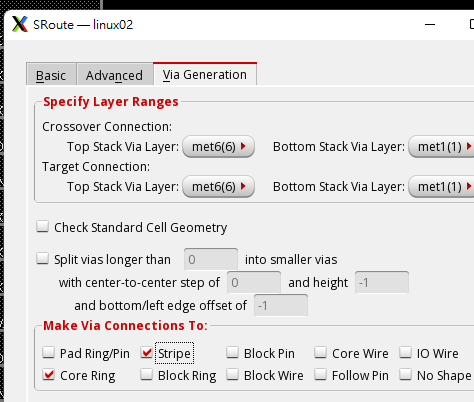
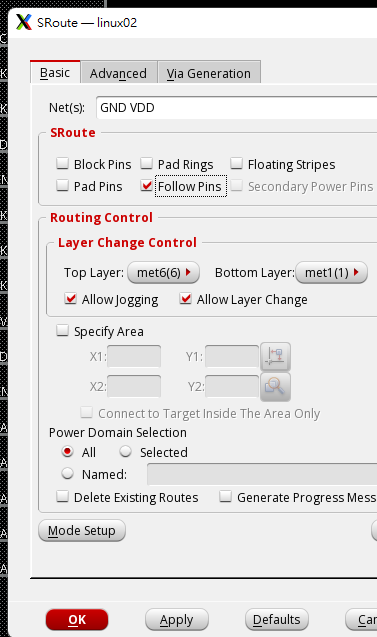


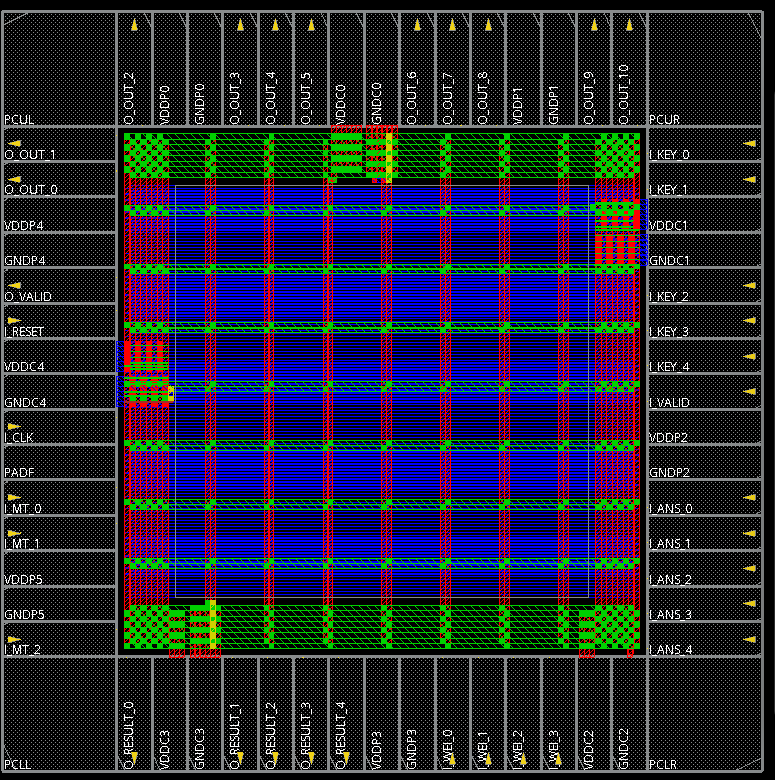
horizontal

不知道這樣行不行

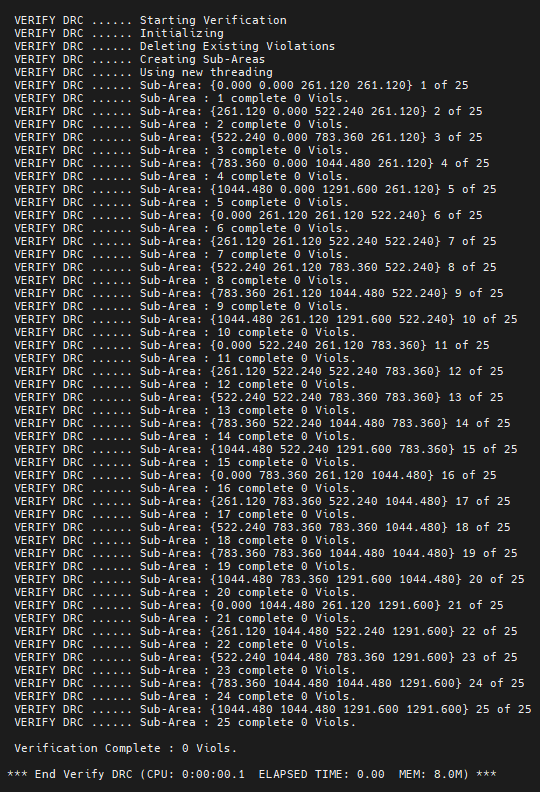
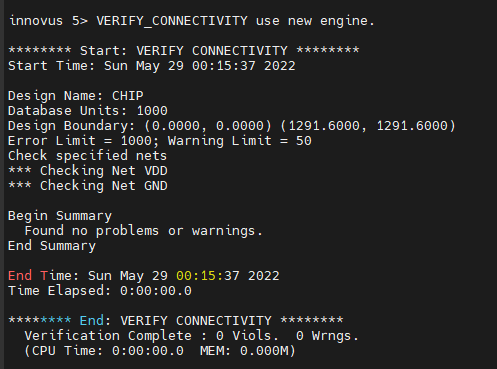
待會存兩個檔案

**9. Connect Standard Cell Power Line**

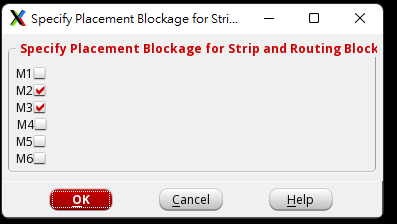




**10. Verify DRC and LVS**

**11. Place Standard Cells**



In innovus menu, open ***Place → Place Standard Cells…***

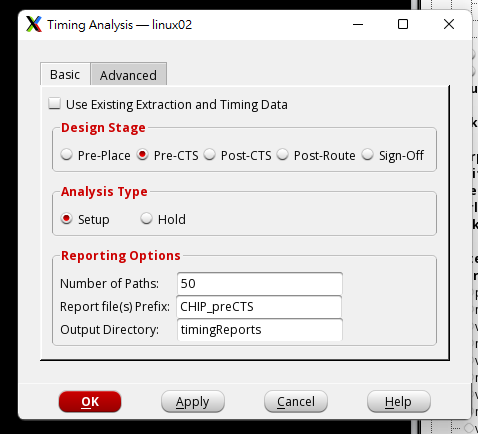
⮚ ◆ Run Full Placement

Optimization Options

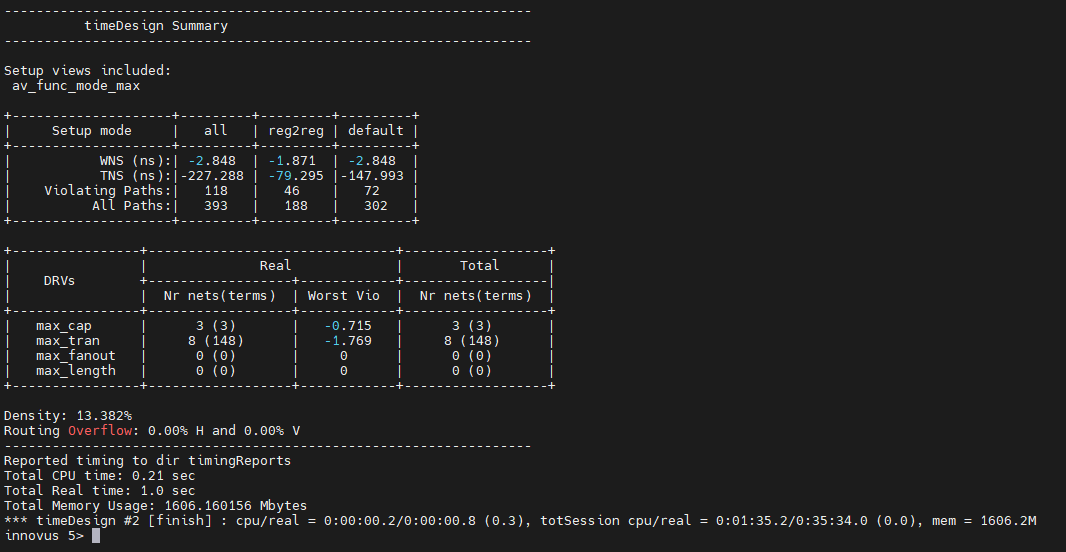
⮚ ◇ Include Pre-Place Optimization



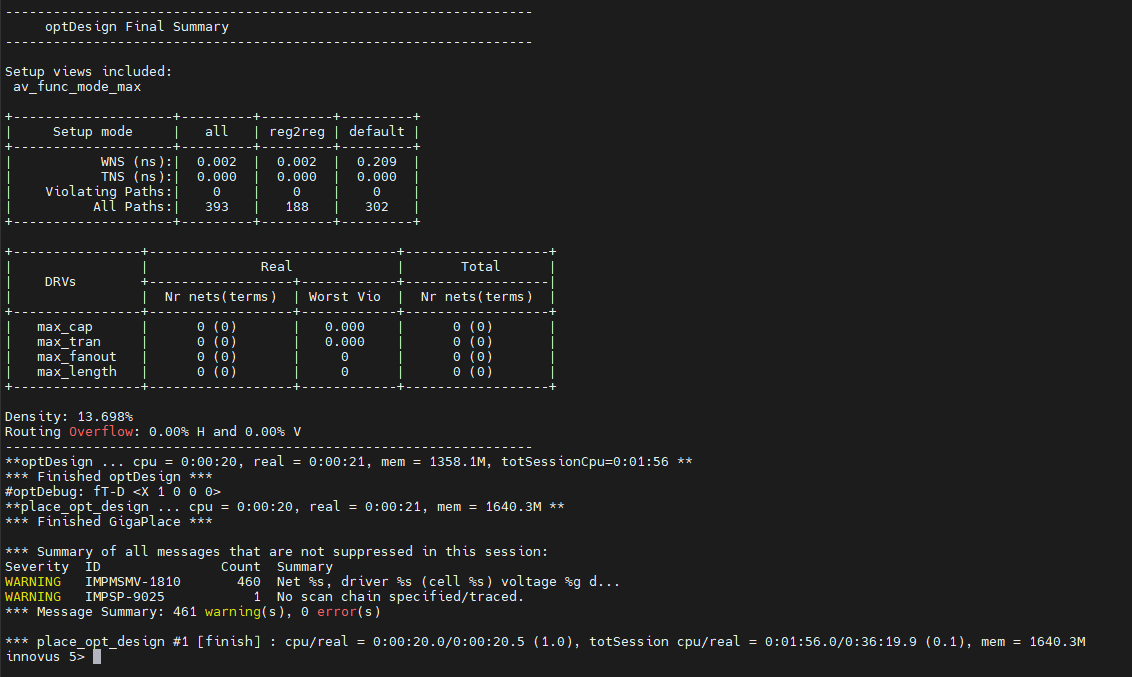
**12. In-Place Optimization (IPO)**

- Before Clock Tree Synthesis

Pre\_CTS



ECO no error , no negative slack DRV=0



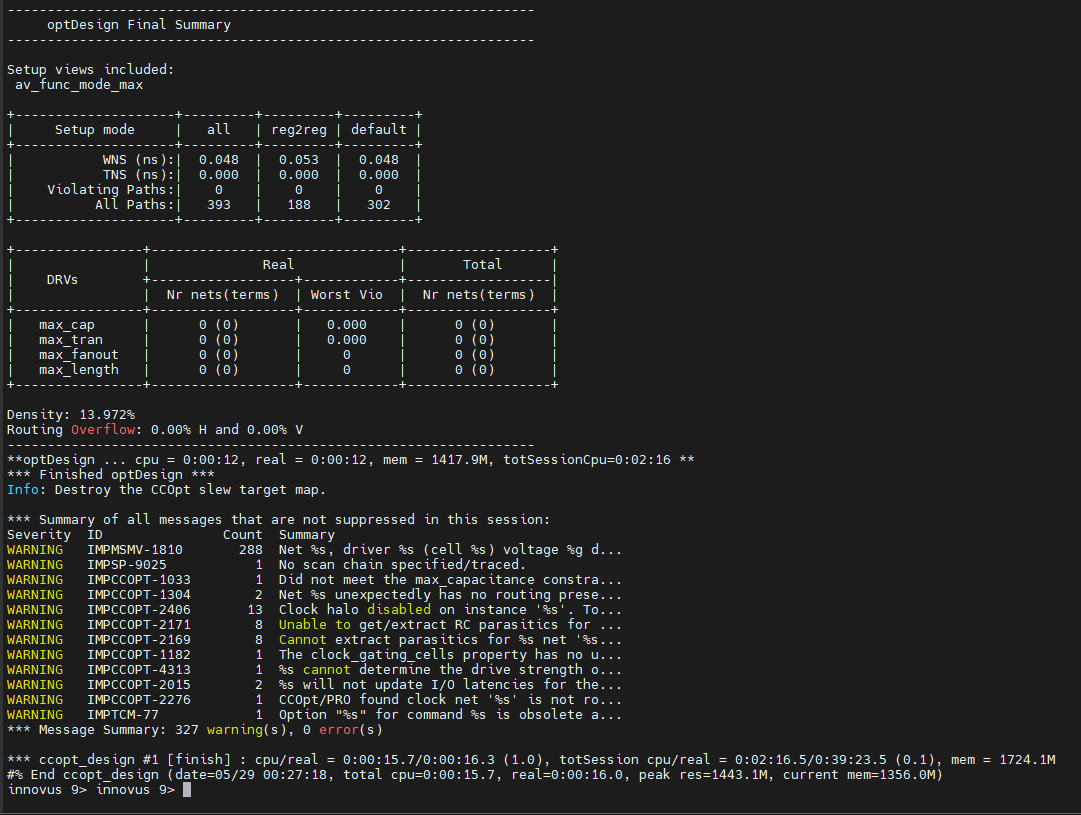
**13. Clock Tree Synthesis (CTS)**

innovus > set\_ccopt\_property update\_io\_latency false

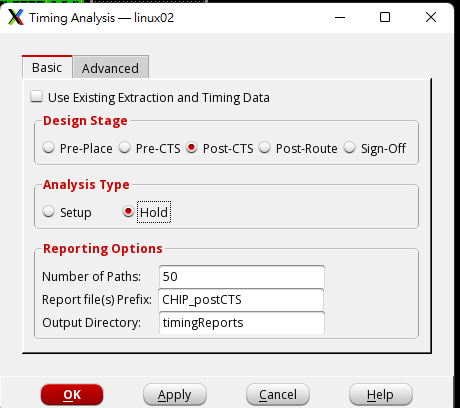
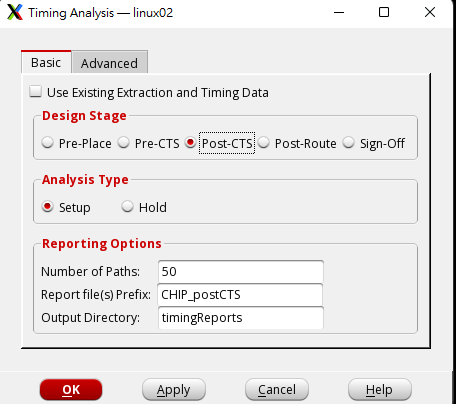
innovus > create\_ccopt\_clock\_tree\_spec -file CHIP.CCOPT.spec -keep\_all\_sdc\_clocks

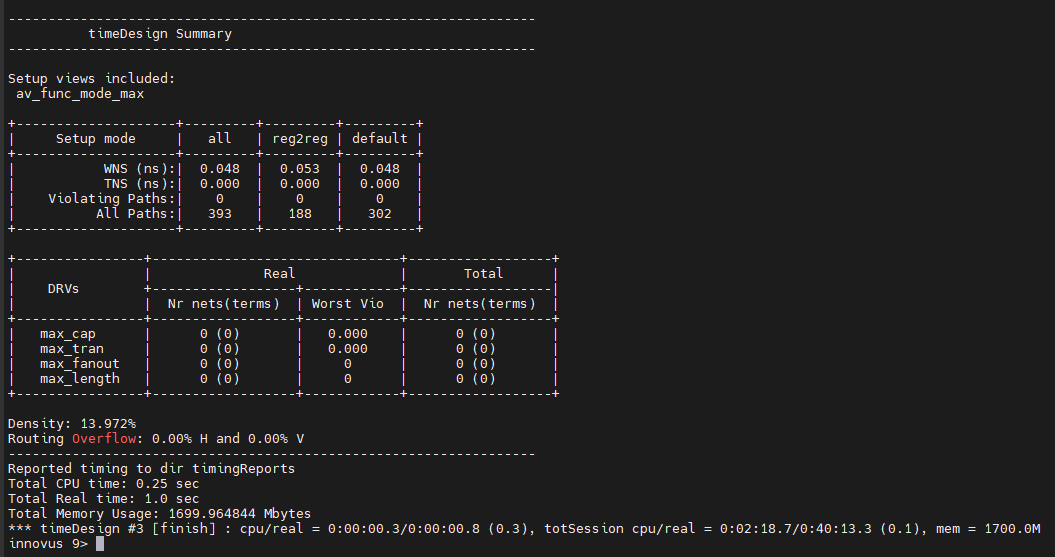
innovus > source CHIP.CCOPT.spec

innovus > ccopt\_design



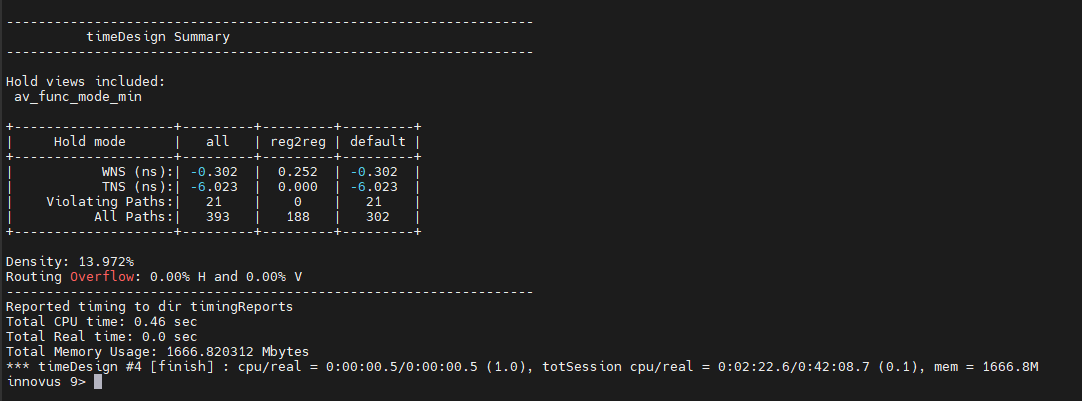
**14. In-Place Optimization (IPO)**

**- After Clock Tree Synthesis**



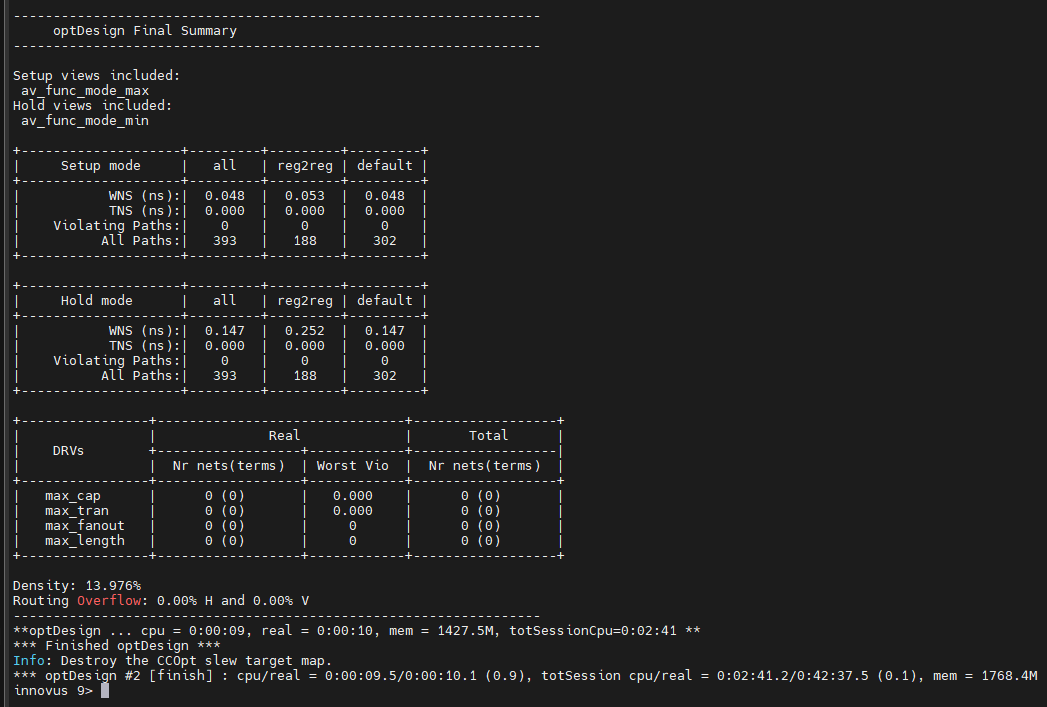
no error , no negative slack, DRV=0

hold time



There are negative slack

ECO



no error , no negative slack, DRV=0

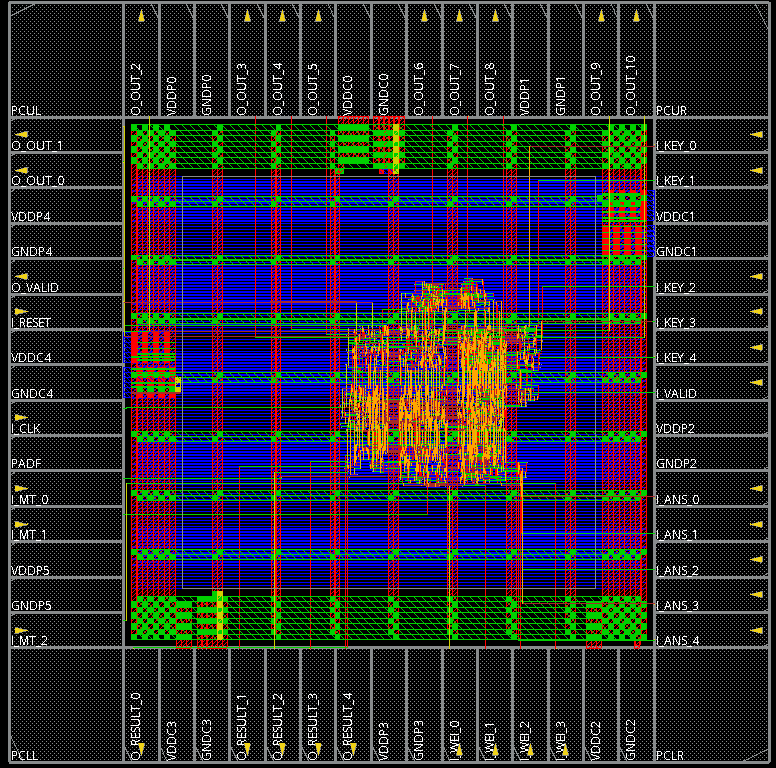
**15. Add PAD Filler**

addIoFiller -cell PFILL -prefix IOFILLER

addIoFiller -cell PFILL\_9 -prefix IOFILLER

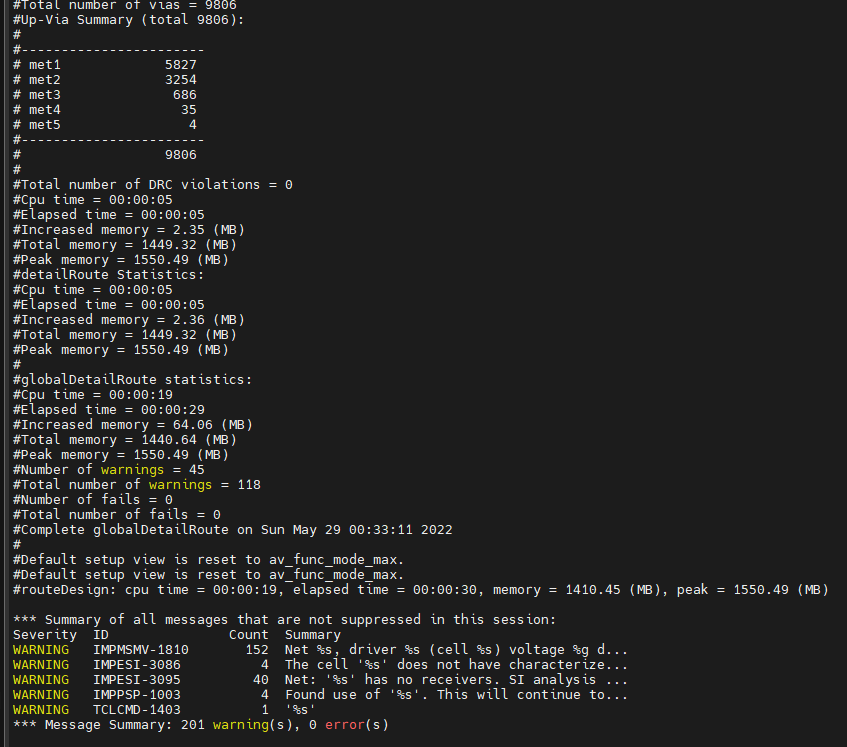
addIoFiller -cell PFILL\_1 -prefix IOFILLER

addIoFiller -cell PFILL\_01 -prefix IOFILLER –fillAnyGap



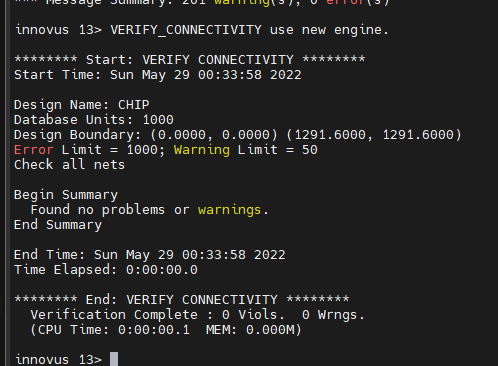
**16. SI-Prevention Detail Route (NanoRoute)**



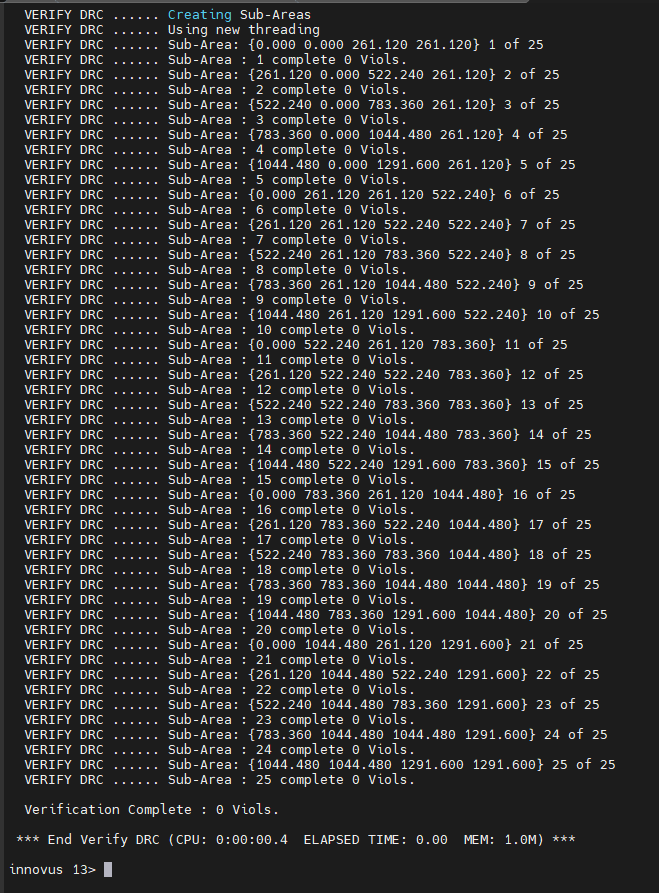


No error

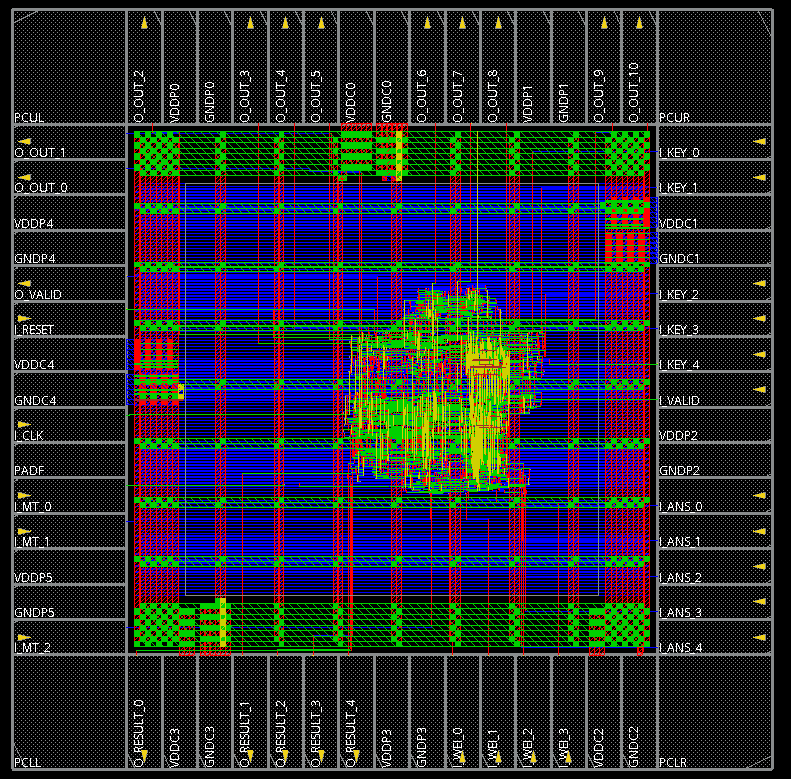
***Verify → Connectivity*** no viols



Verify → DRC no viols

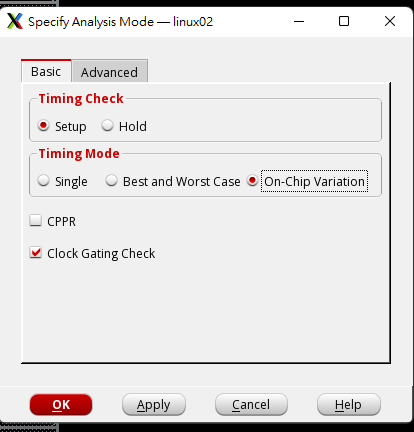
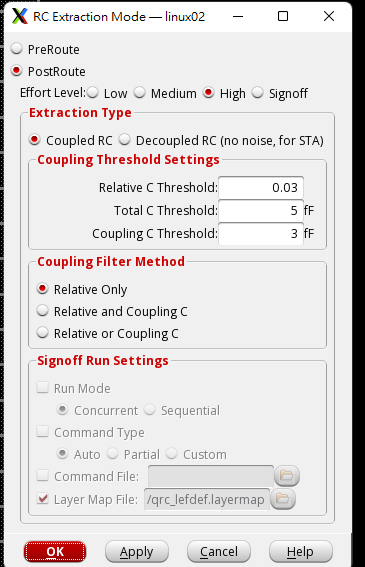


Save design as CHIP\_nanoRoute.inn



No X at layout

**17. In-Place Optimization (consider crosstalk effects)**

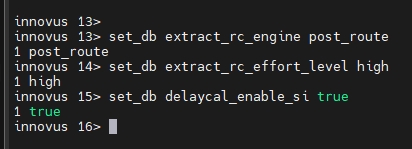
**- After Detail Route** **** 

***3. Setting rc and si***

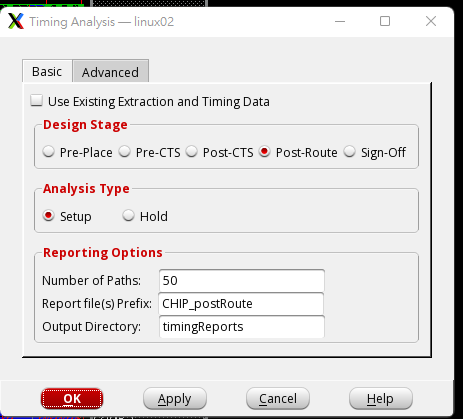
innovus > set\_db extract\_rc\_engine post\_route

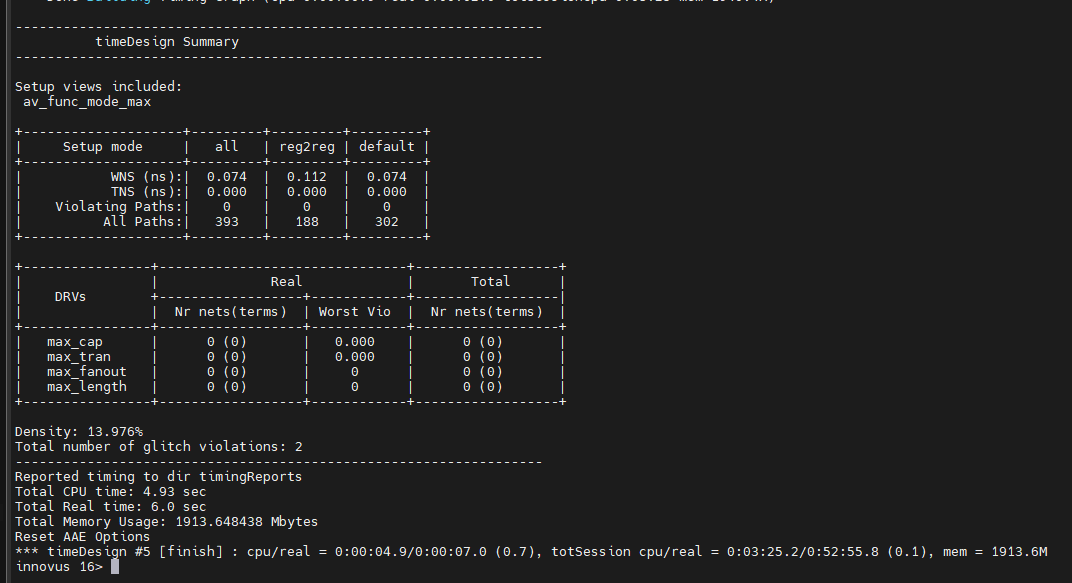
innovus > set\_db extract\_rc\_effort\_level high

innovus > set\_db delaycal\_enable\_si true

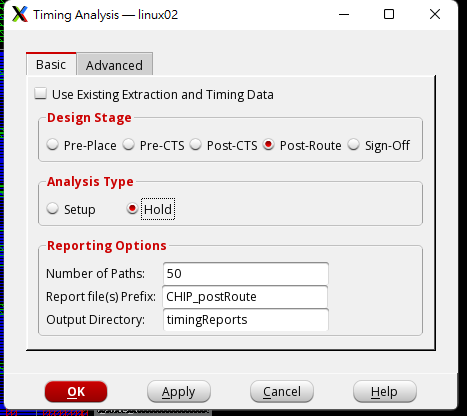


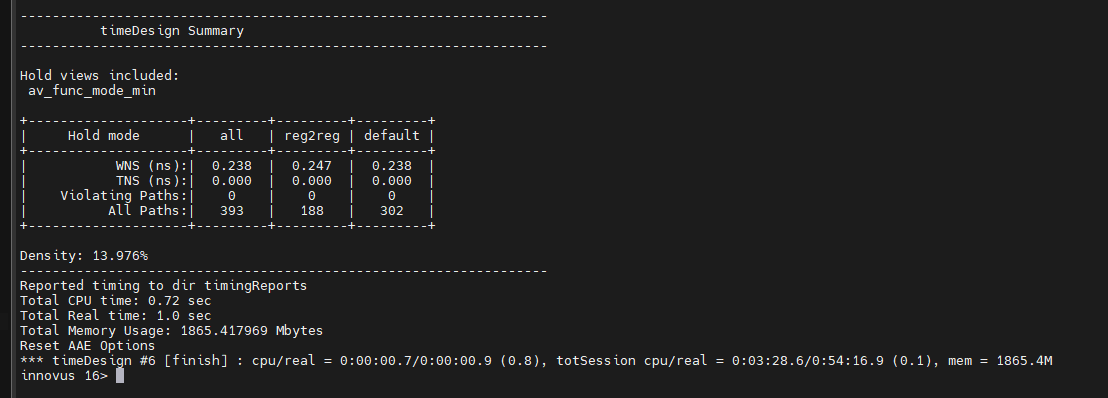
postRoute setup time

 no error , no negative slack, DRV=0

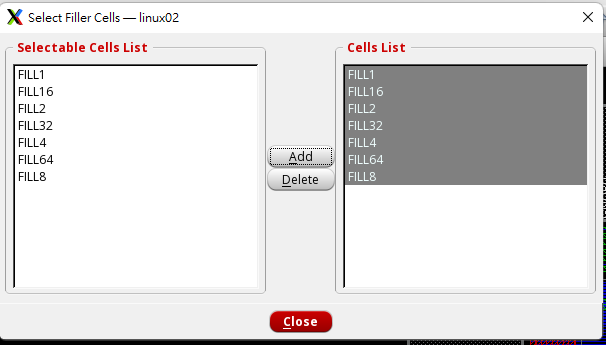
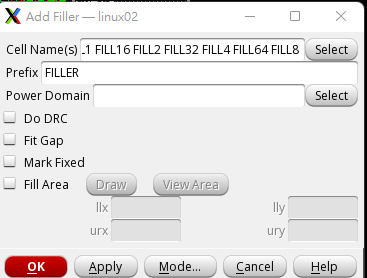


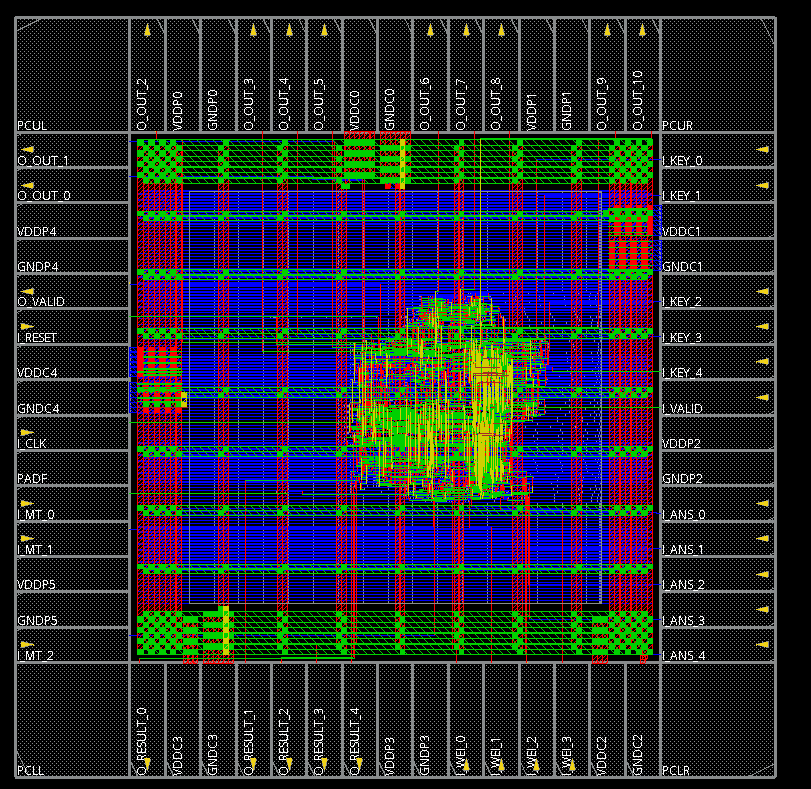
postRoute hold time

 no error , no negative slack, DRV=0

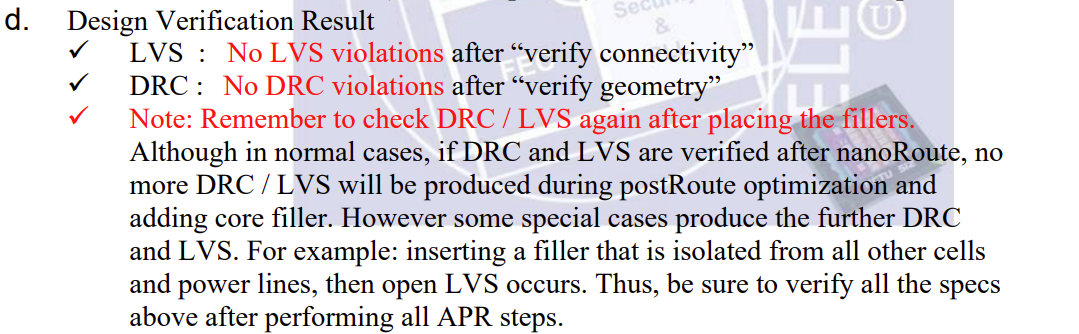


**19. Add CORE Filler Cells**

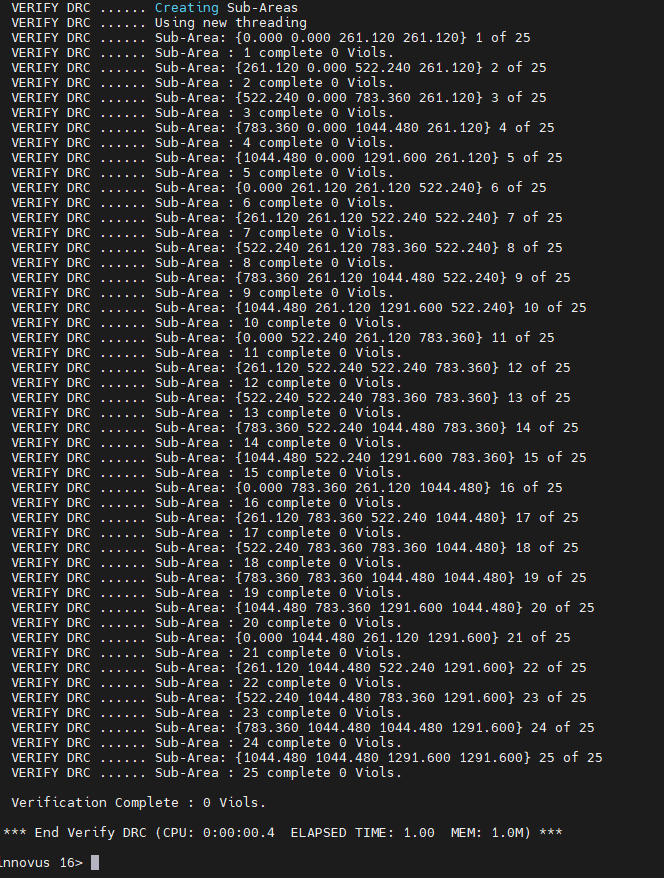
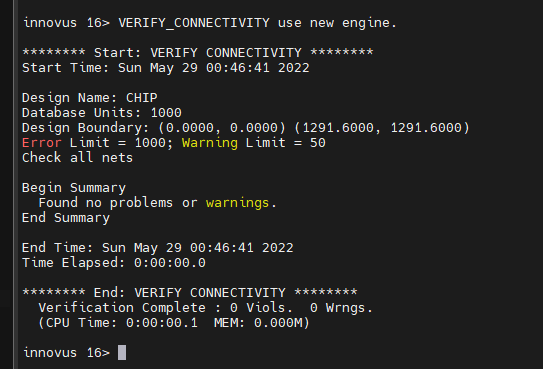
 



Remember to check DRC / LVS again after placing the fillers.



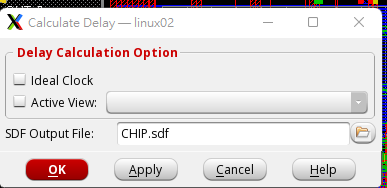
DRC no viols , LVD no viols

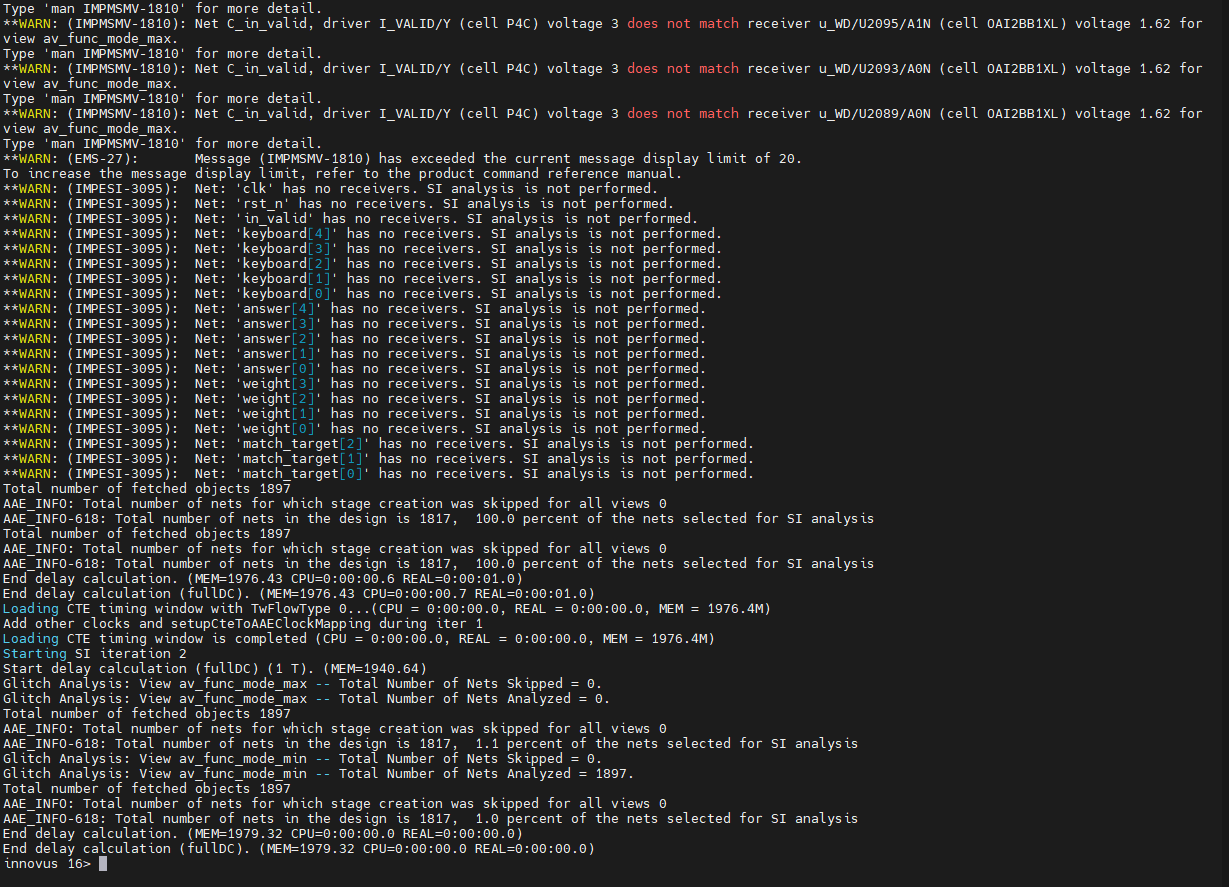
 

**20. Stream Out and Write Netlist**

1. Save design as CHIP.inn

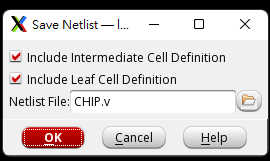
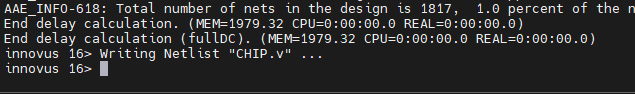
* 1. 2. Write CHIP.sdf ***a.*** In innovus menu, open ***Timing → Write SDF***
  2. **b. Delay Calculation Option** ⮚ ◇ Ideal Clock (Ideal Clock should be disabled)





Lots of warn but no error

* 1. Save design netlist CHIP.v for post-layout simulation: ***a.*** In innovus menu, open ***File→ Save → Netlist…***

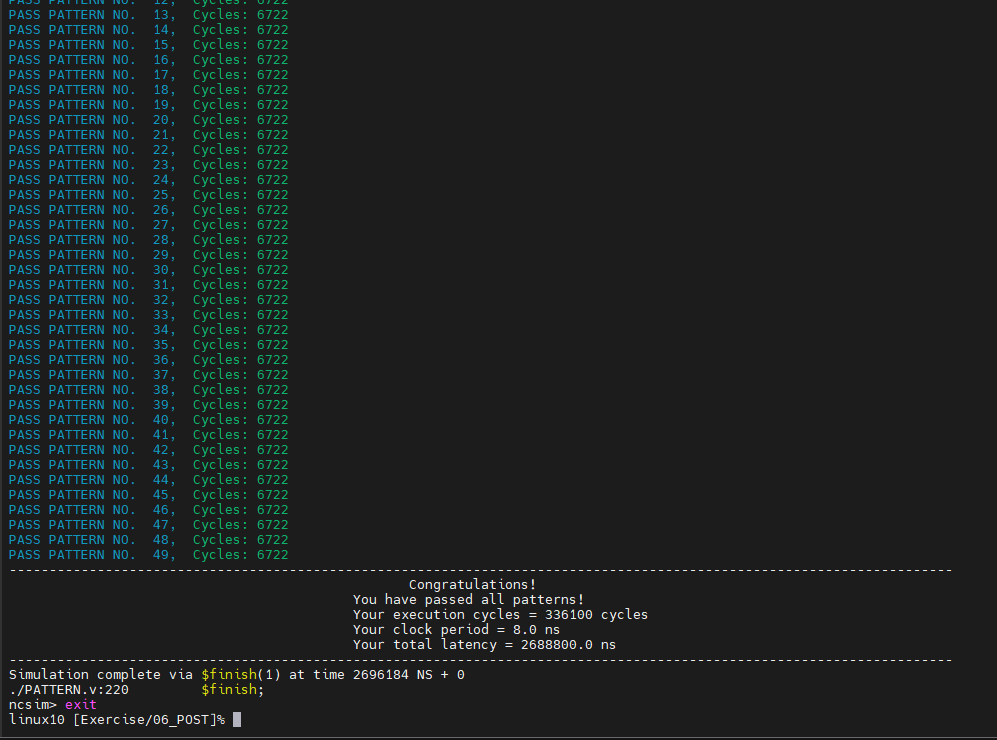
 

**21. Post-Layout Gate-Level Simulation**

**1.** Change to directory **06\_POST**

2. Perform Post-Layout Gate-level simulation of CHIP.v

**% ./01\_run** The latency should be the same as gate level simulation



Power part

2. Set environment

cd Lab12/Practice/05\_APR

⚫unix% mkdir power\_log (You will save all the things here)

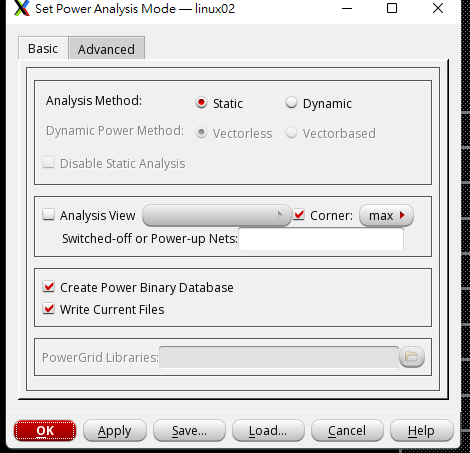
⚫Restore the design **DBS/CHIP.inn**

3. Static Power Analysis

**1. Save CHIP.v**

**2. Write CHIP.sdf**

**3.** Run post simulation at 06\_POST, the generated waveform CHIP\_POST.fsdb will be used for power rail analysis.



**5.** In the innovus menu, open ***Power*** -> ***Power Analysis*** -> ***Run***

i ◆Activity FILE ◆FSDB

ii. Fill the information:

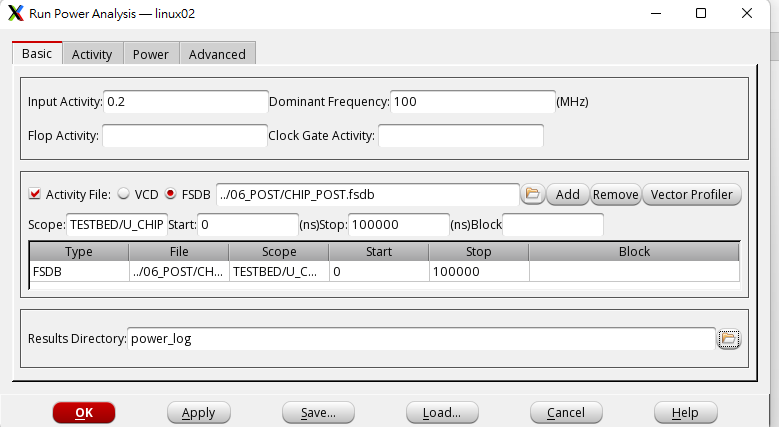
⚫Select CHIP\_POST.fsdb (from 06\_POST)

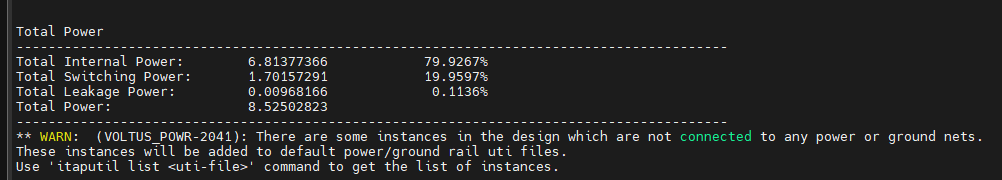
⚫Scope: TESTBED/U\_CHIP

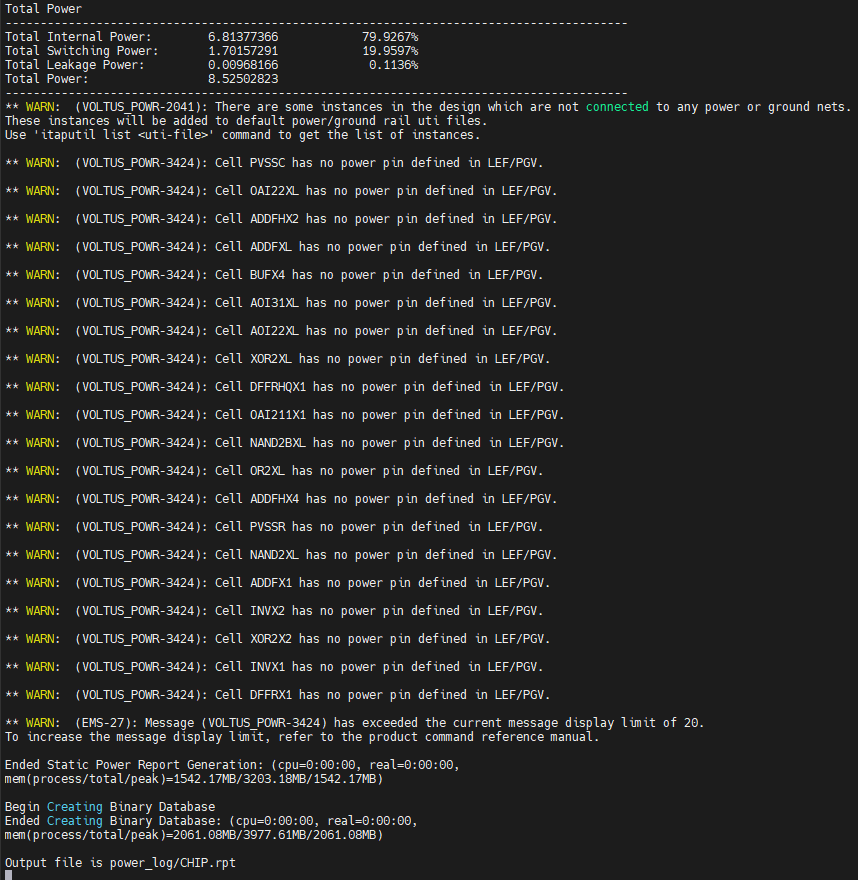
⚫Start: 0; Stop: 100000

⚫Press Add

* 1. iii. Results Directory: power\_log
  2. iv. Click OK.

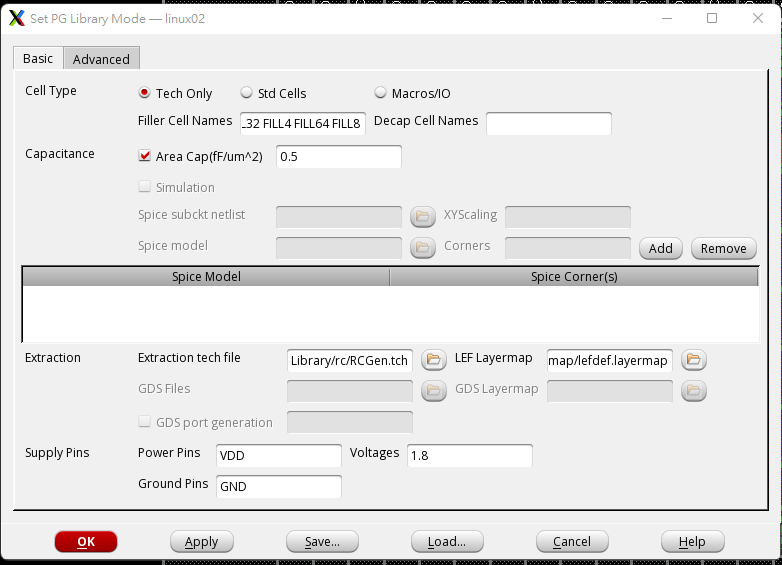




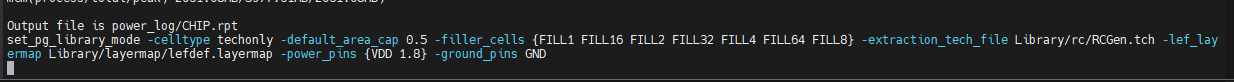


4. Create Power Grid Library

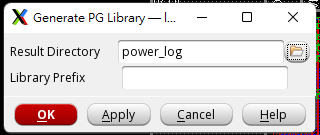
**1.** In the innovus menu, open ***Power*** -> ***Rail Analysis*** -> ***Set PG Library Mode***



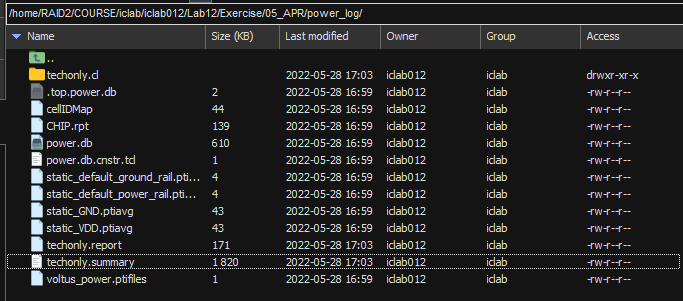
No hard marco so Ground Pins is only GND no VSS



**2.** In the innovus menu, open ***Power -> Rail Analysis -> Generate PG Library***



iii. Check if the directory **techonly.cl** exists (under power\_log/)



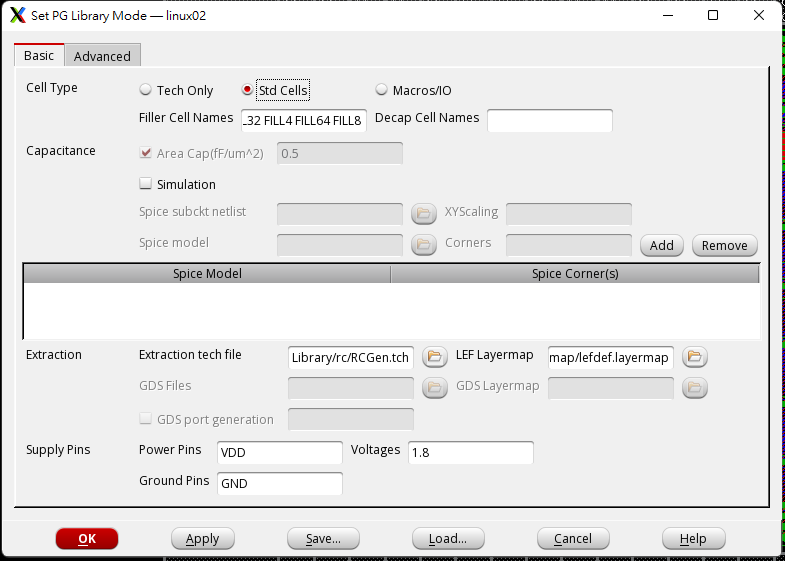
There it is

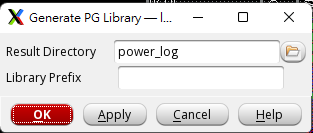
This is acceptable

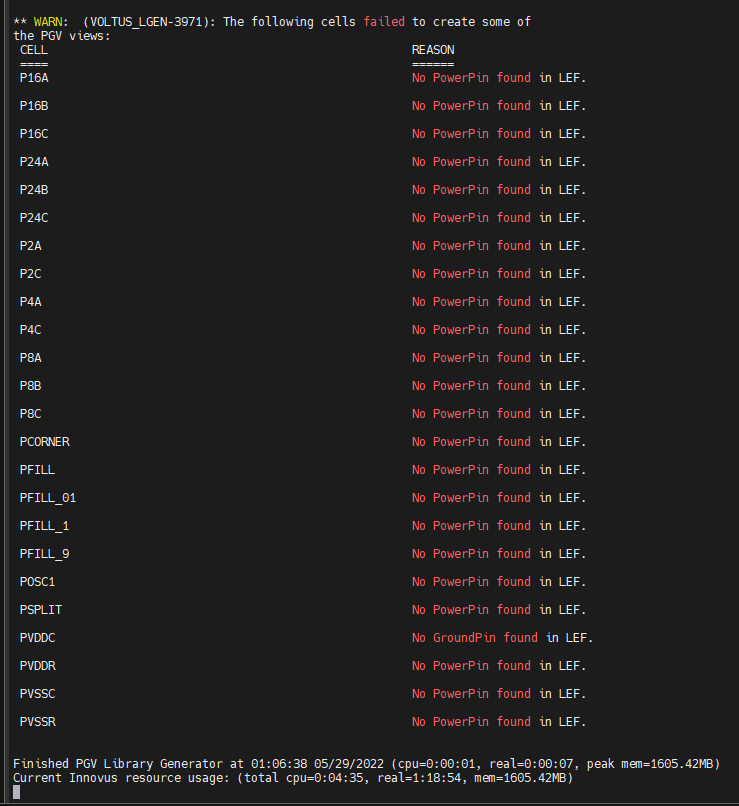
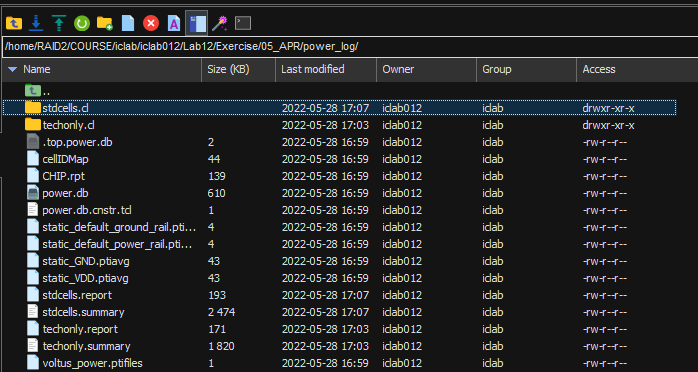
**3.** In the innovus menu, open ***Power -> Rail Analysis -> Set PG Library Mode***

◆Std Cells



**4.** In the innovus menu, open ***Power -> Rail Analysis -> Generate PG Library***

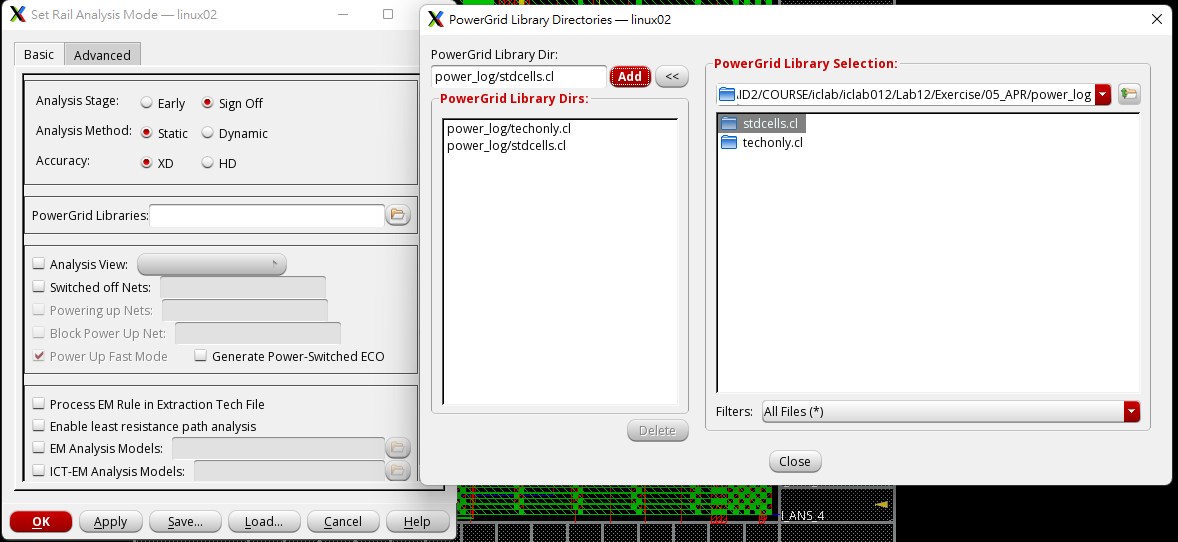




Still have warn and it is acceptable

5. Rail Analysis

**1.** In the innovus menu, open ***Power -> Rail Analysis -> Setup Rail Analysis***



**2.** In the innovus menu, open ***Power -> Rail Analysis -> Run Rail Analysis***

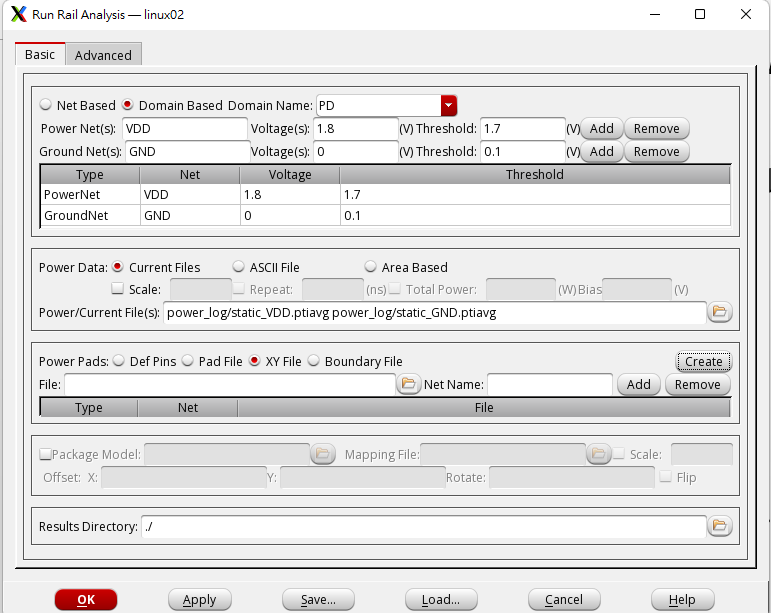
i. ◆ Domain Based Domain Name: PD

ii. Power Net(s): VDD Voltage(s): 1.8 Threshold:1.7 (Press ADD)

iii. Power/Current Files(s):

**power\_log/static\_VDD.ptiavg**

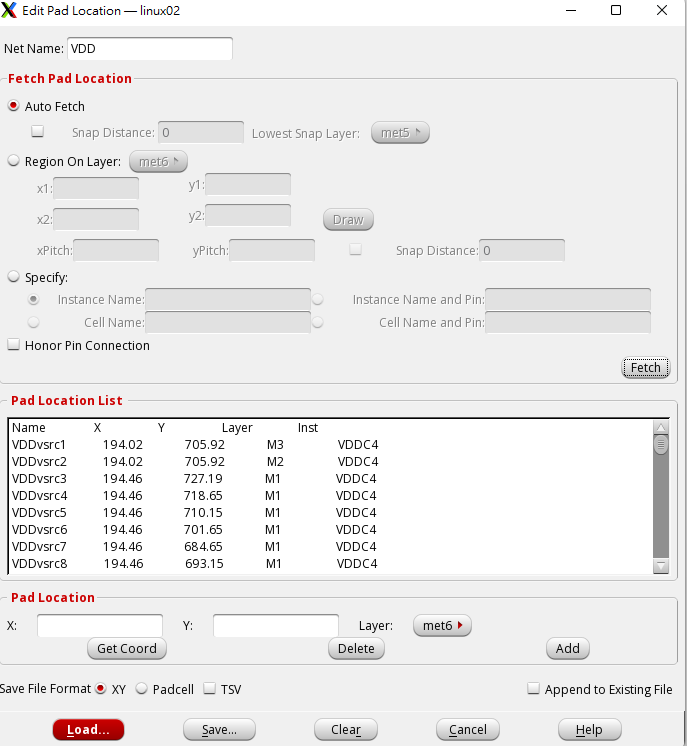
**power\_log/static\_GND.ptiavg**

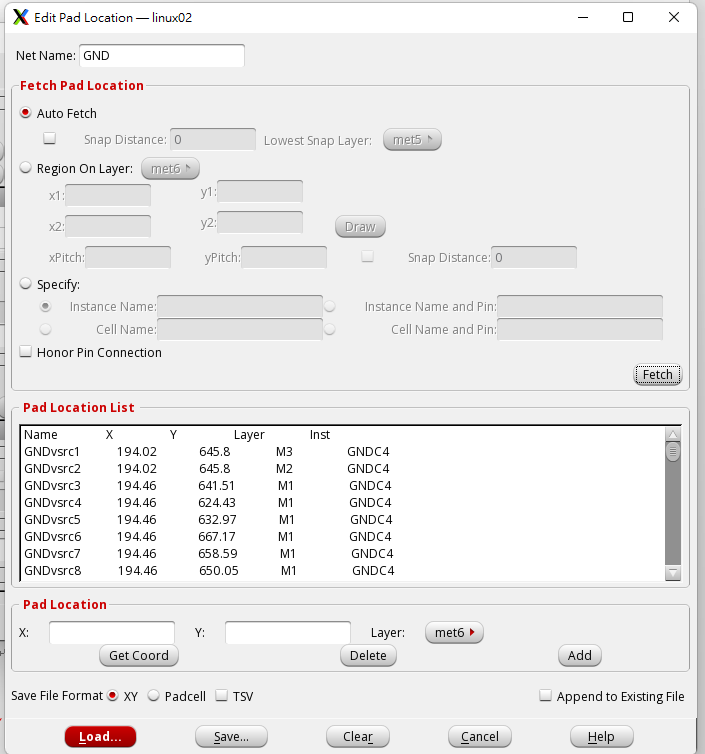


iv. Power Pads: ◆ XY File

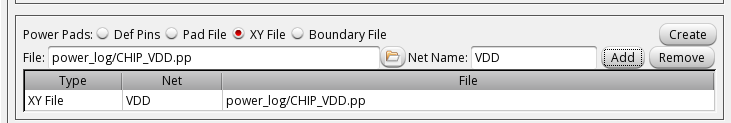
v. Click **Create**

Net Name: VDD Click Fetch

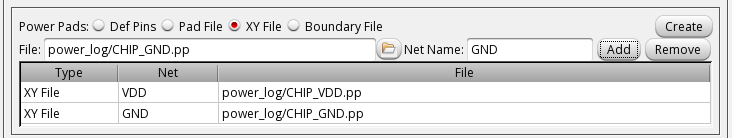
Save as **power\_log/CHIP\_VDD.pp**

 Save as **power\_log/CHIP\_GND.pp**

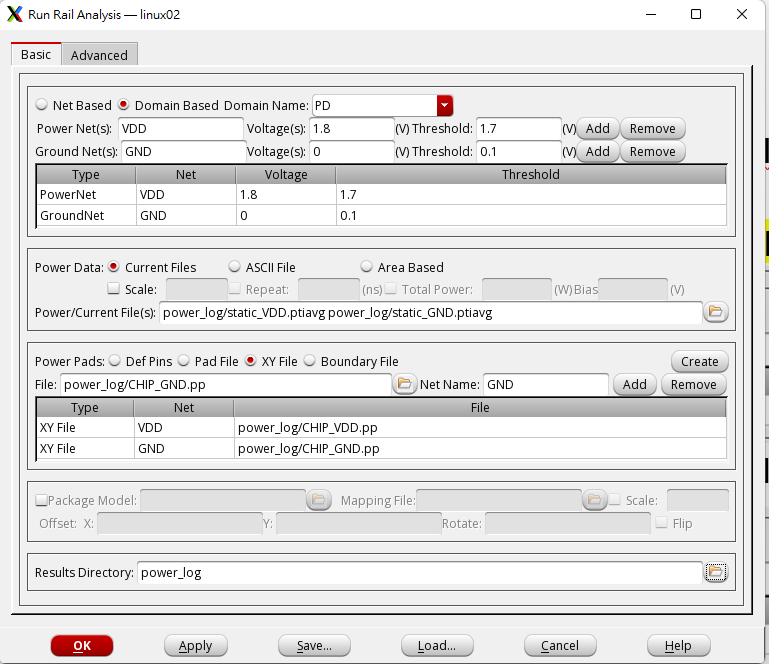
File: **power\_log/CHIP\_VDD.pp** Net Name: VDD (press ADD)

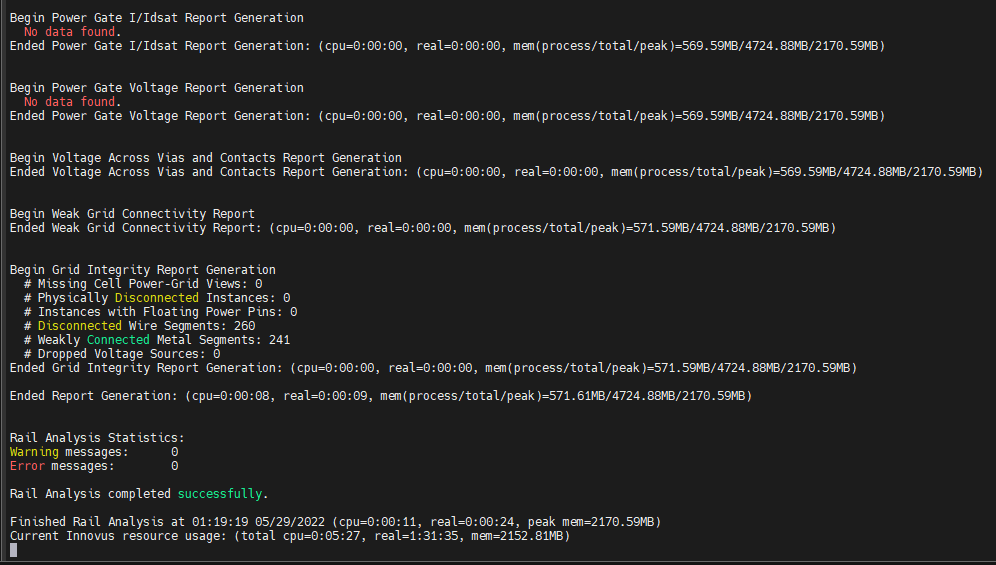


File: **power\_log/CHIP\_GND.pp** Net Name: GND (press ADD )

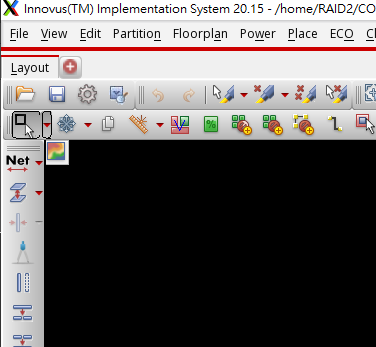


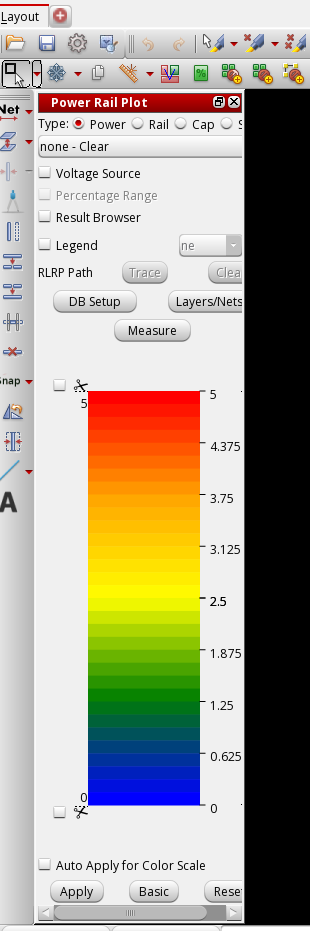
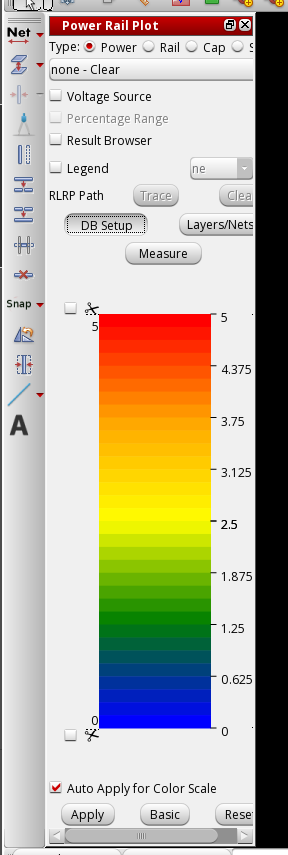
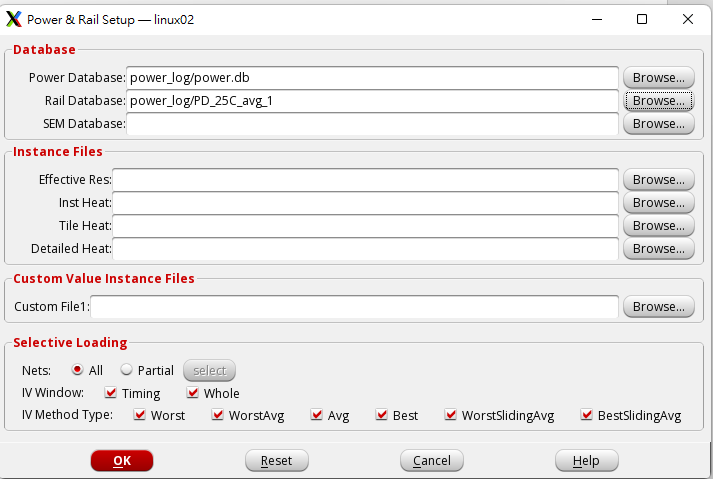
Results Directory: **power\_log**

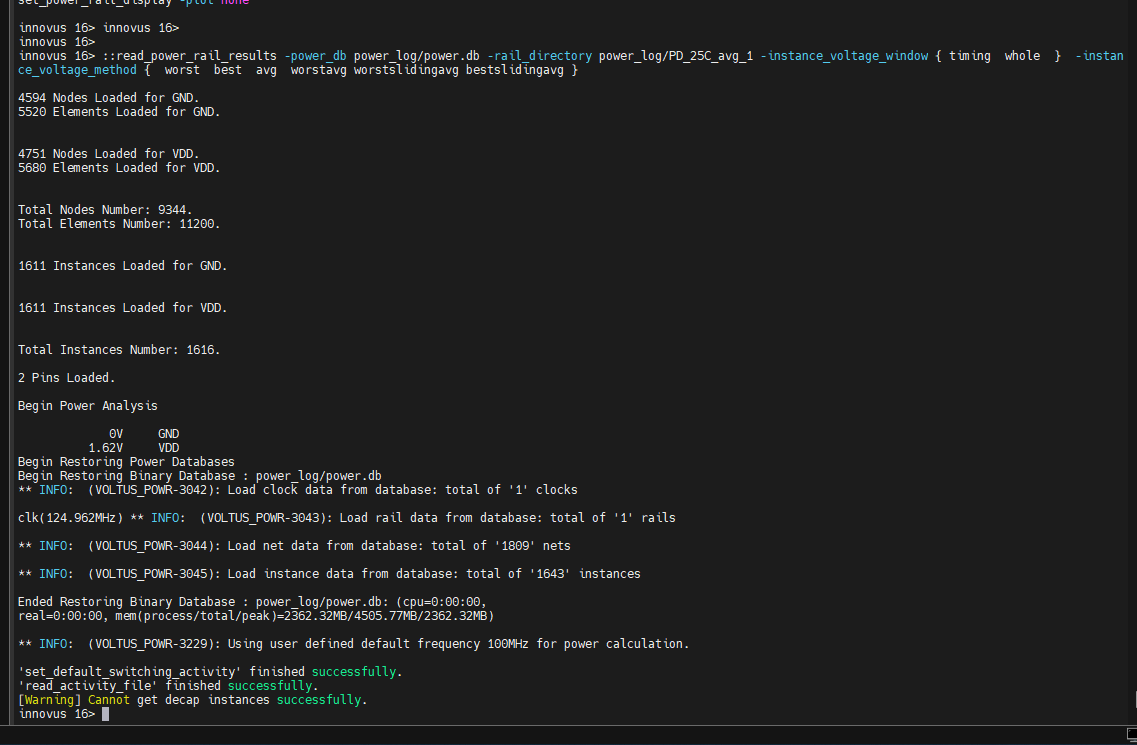
會跑一下



6. Power & IR Drop Results **1.** In the innovus menu, open ***Power -> Report -> Power & Rail Result***

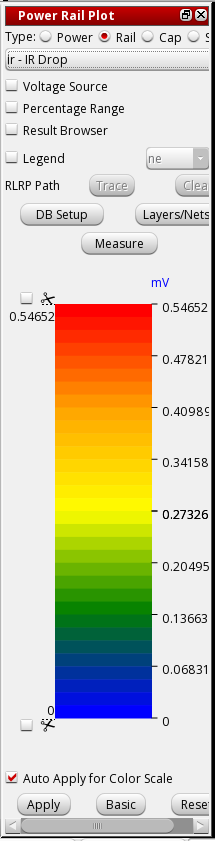
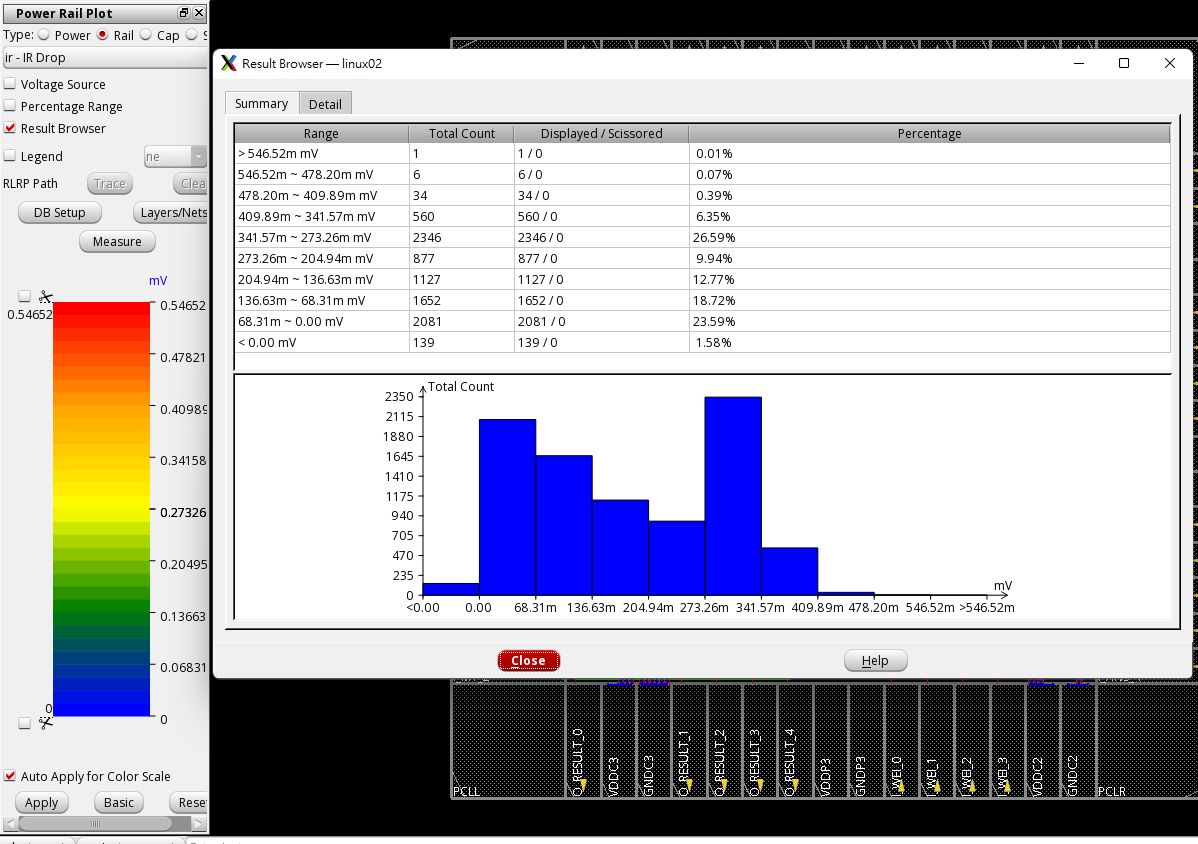
回Innovus找左上角那個圖

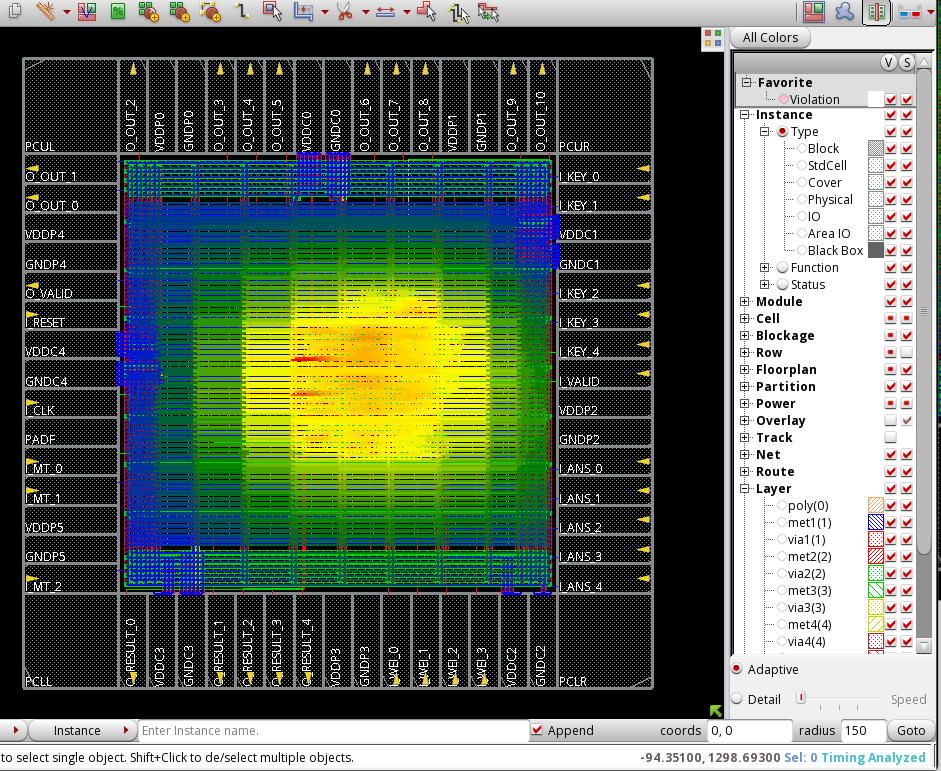
點開變這樣 

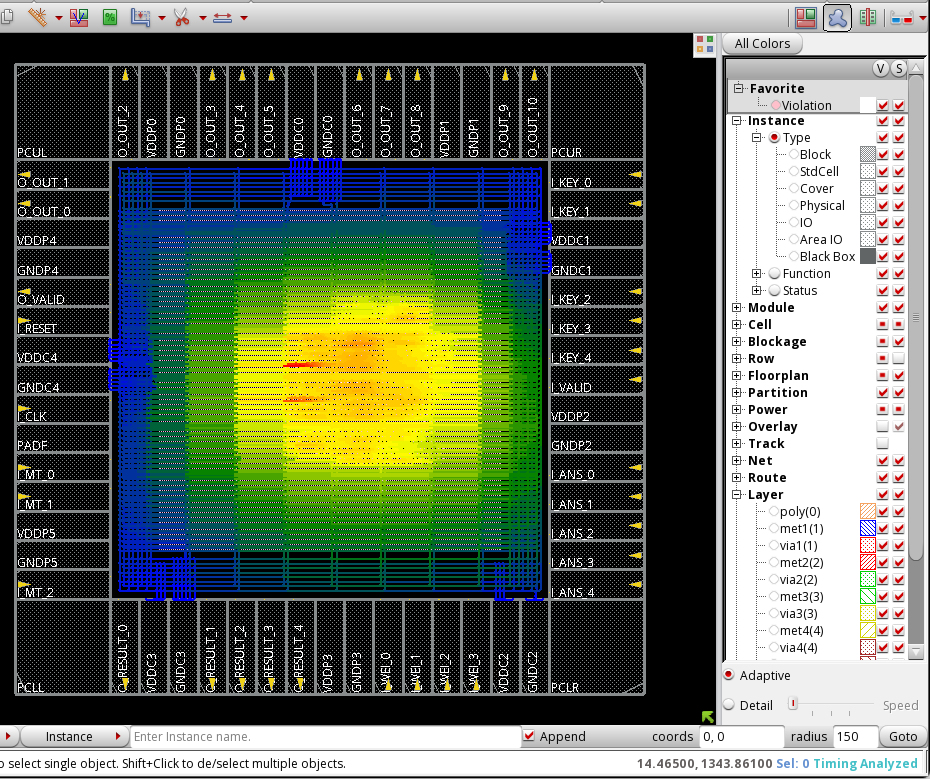


i. ◆Result Browser

The following shows the distribution of IR Drop (they should in the range **0.1V**)





And DONE No IR drop is allowed larger than 5mV