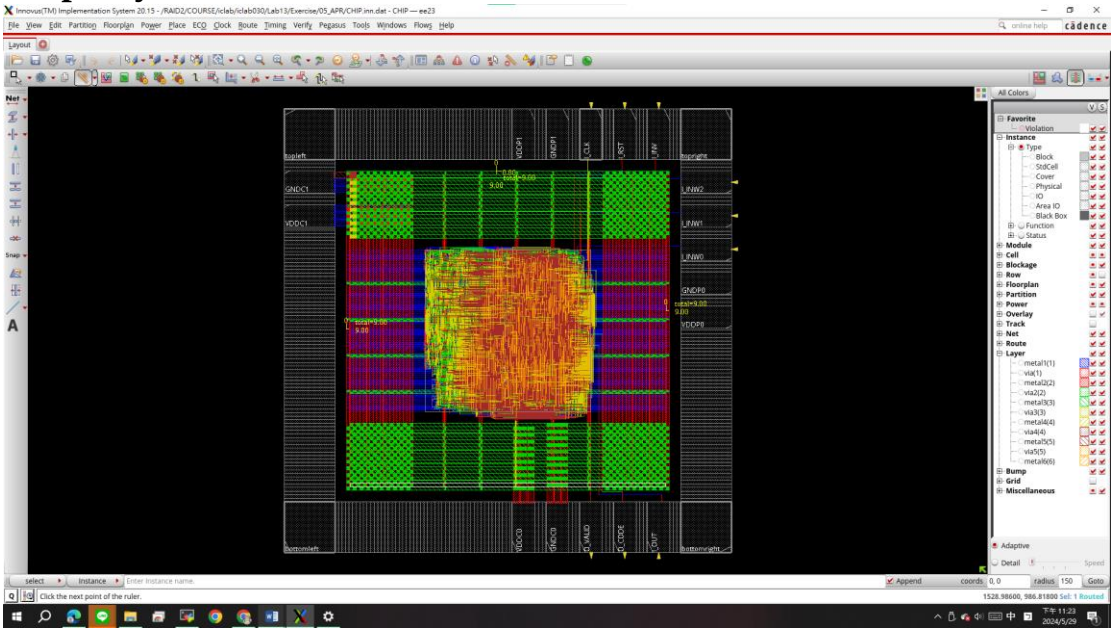
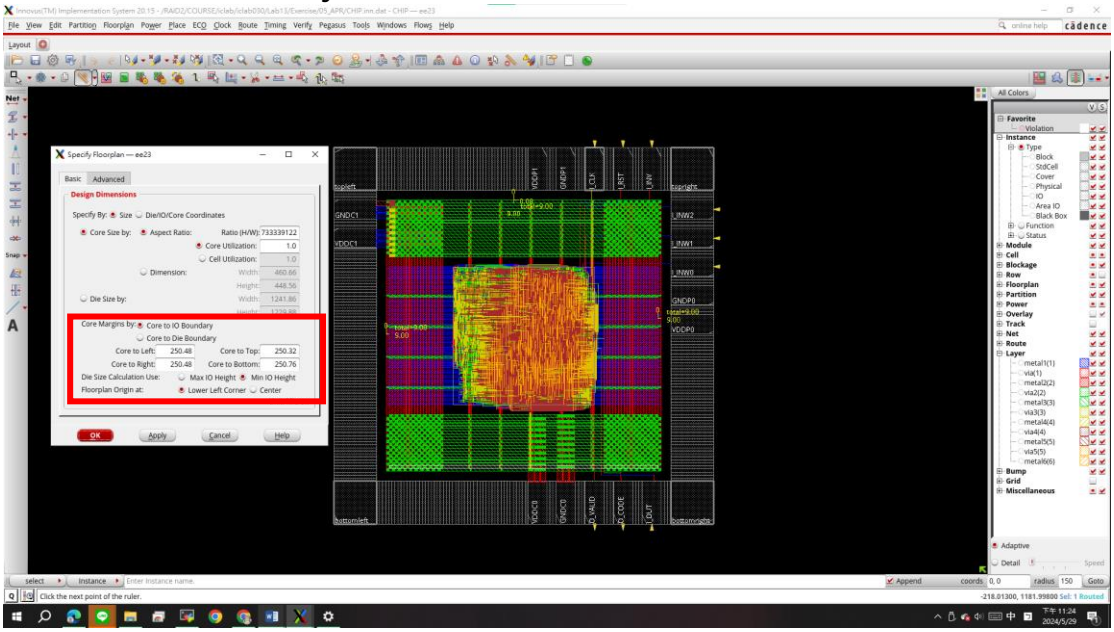
Report

1. Chip Layout View :

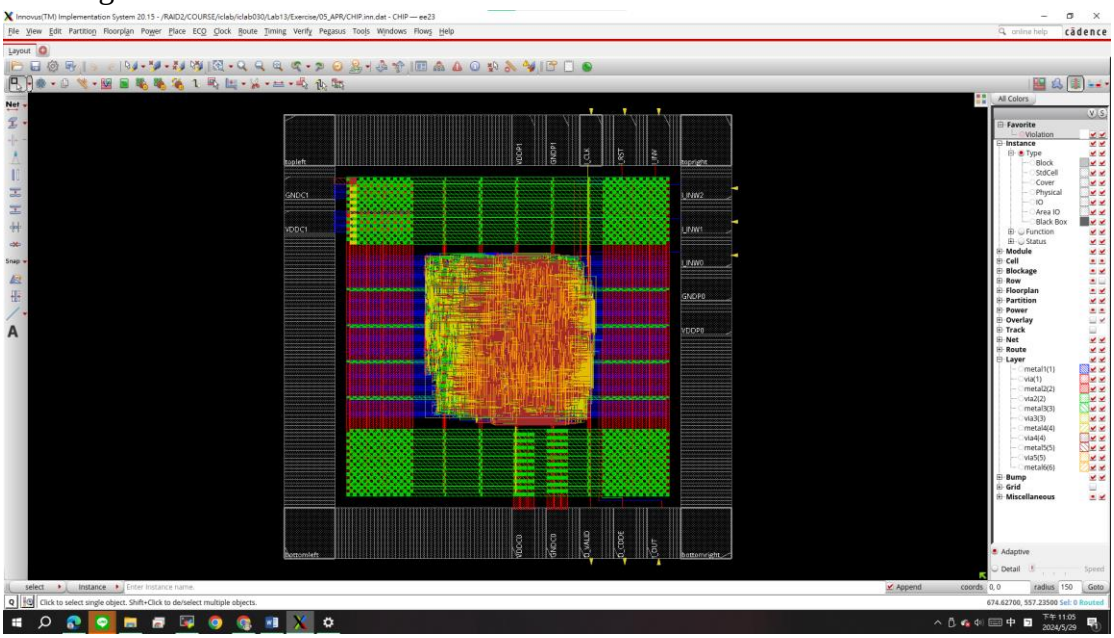


2. Core to IO boundary :

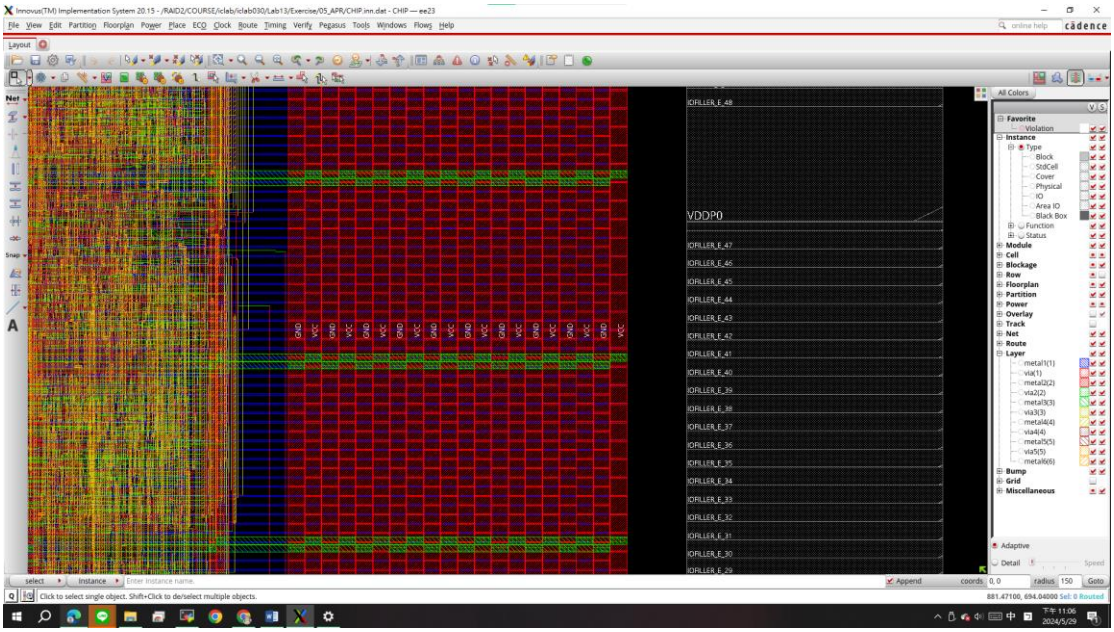


3. Core Ring :

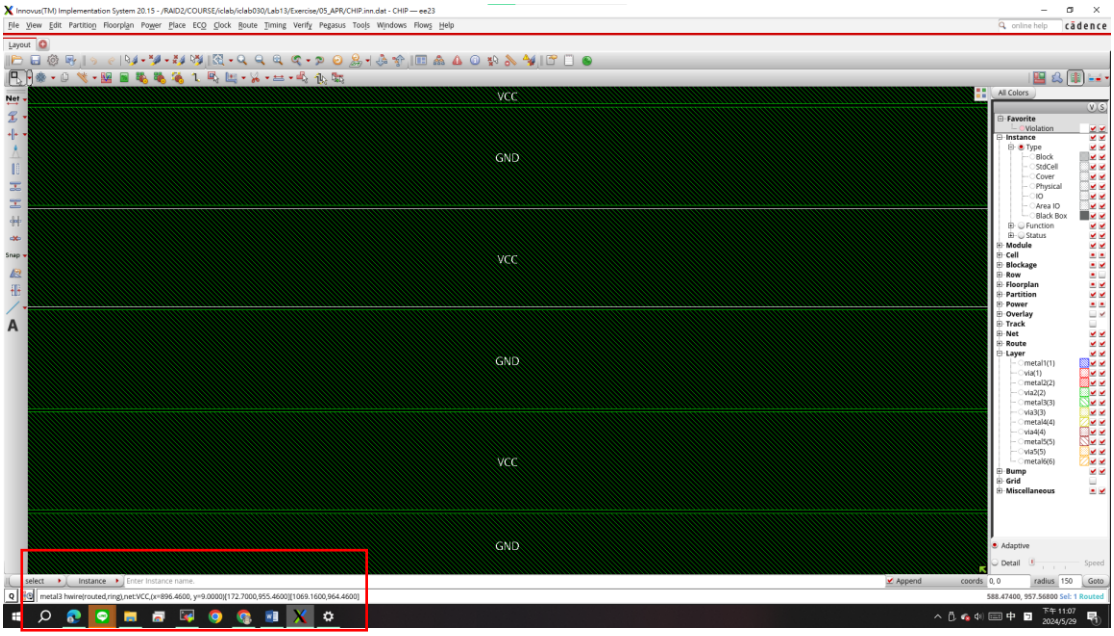
- All Ring

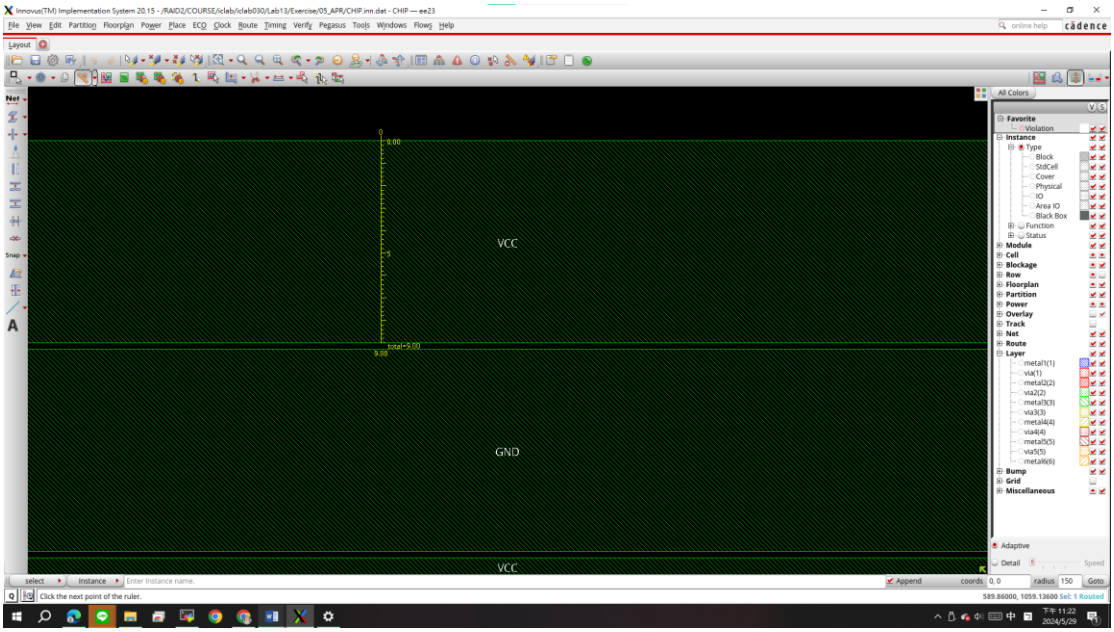


- 10 pairs

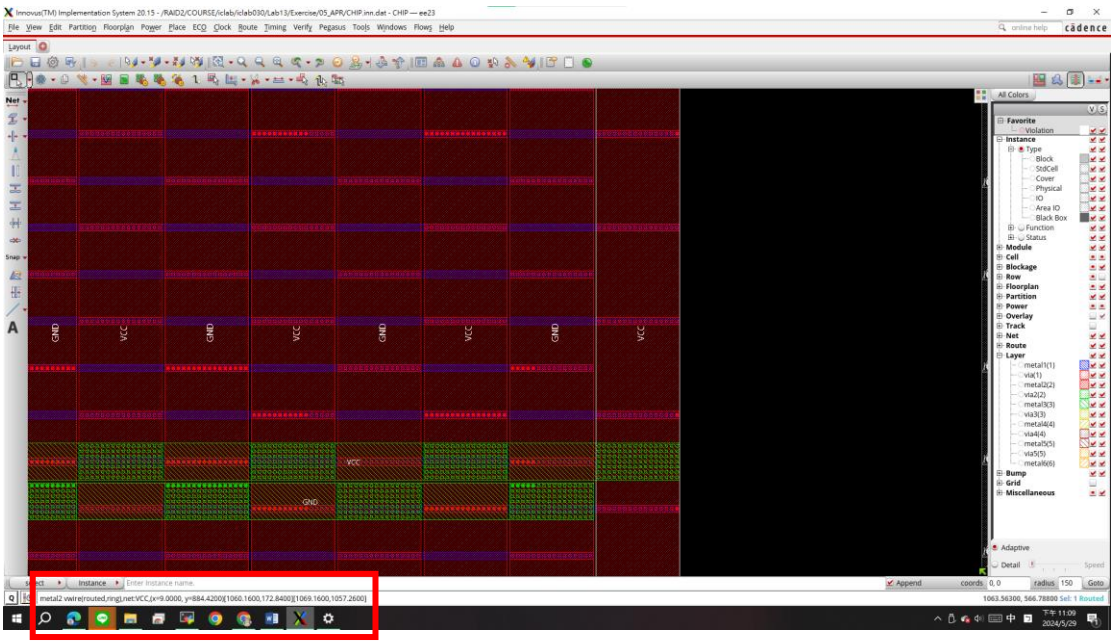


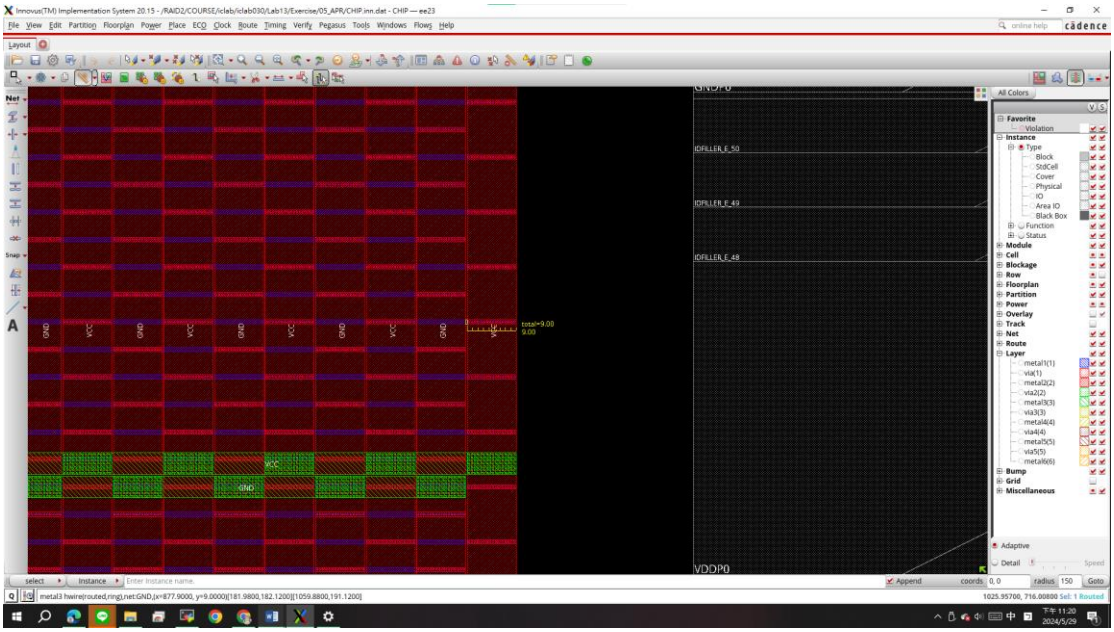
- Top
- VCC :



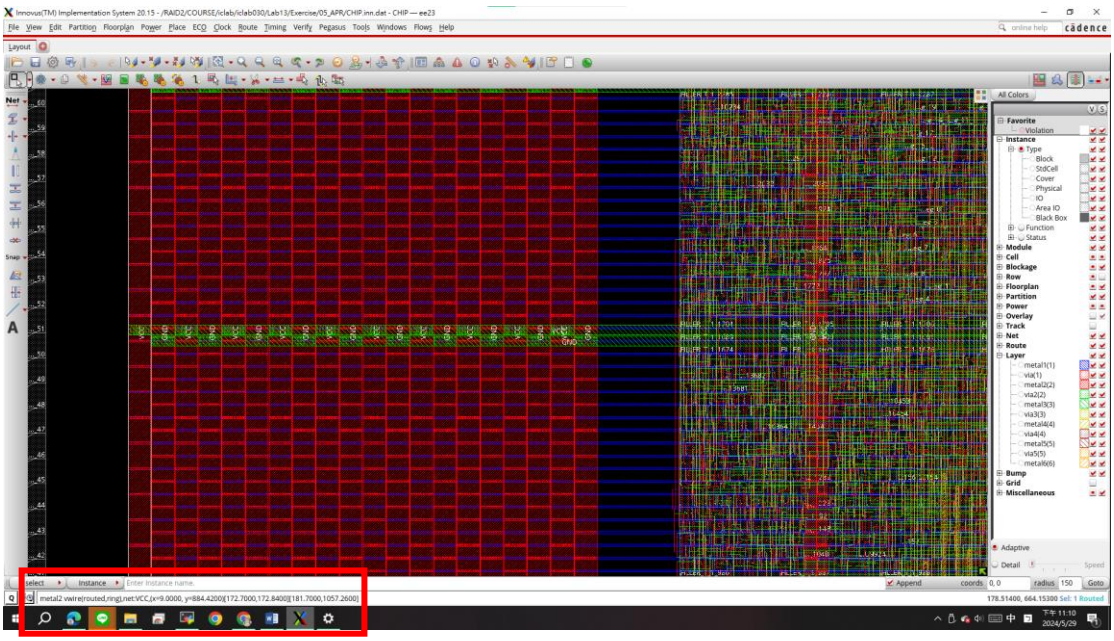


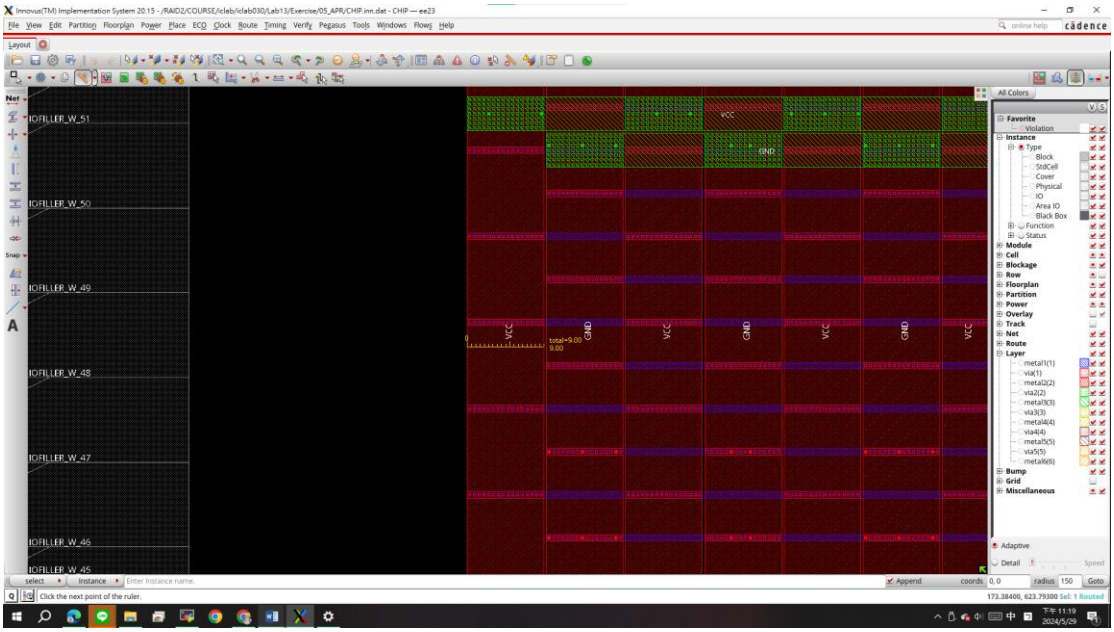
- Right
- VCC :


GND
VCC
GND
VCC
GND
VCC
GND
VCC
VCC
GND

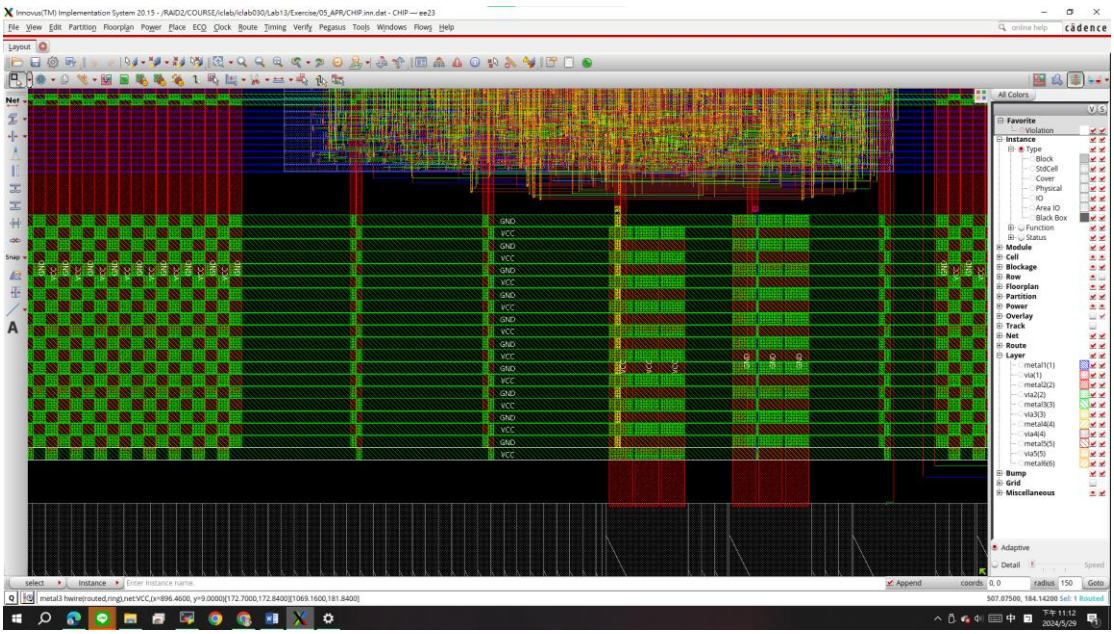

IOFILLER_E_50
IOFILLER_E_49
IOFILLER_E_48
GND
VCC
GND
VCC
GND
VCC
GND
VCC
GND
VCC
VCC
GND
VDDP0

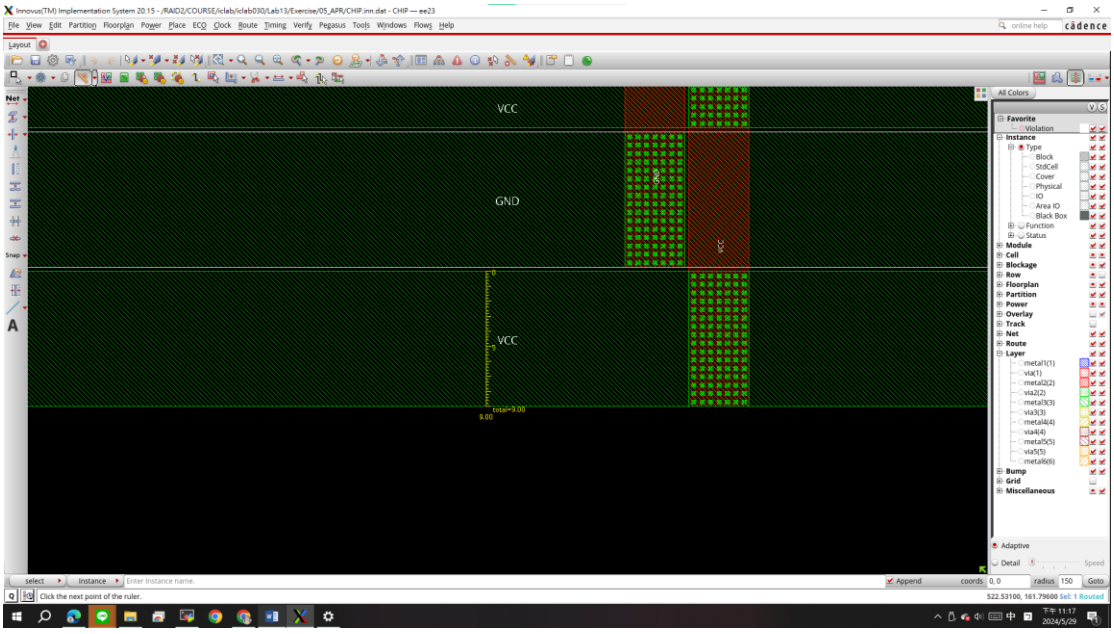
- Left
- VCC :



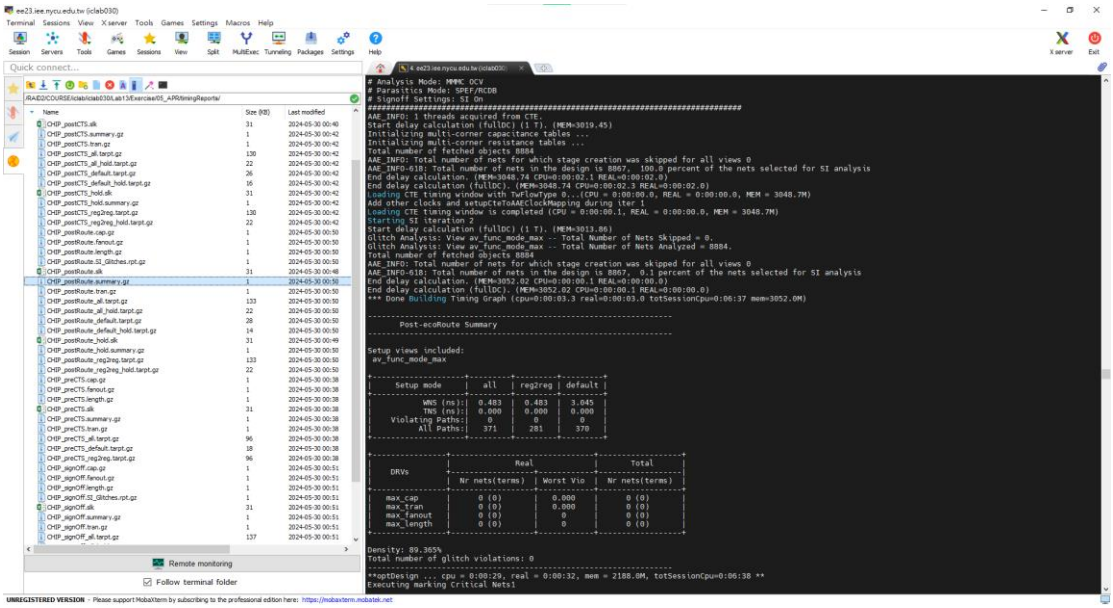


- BOTTOM
- VCC

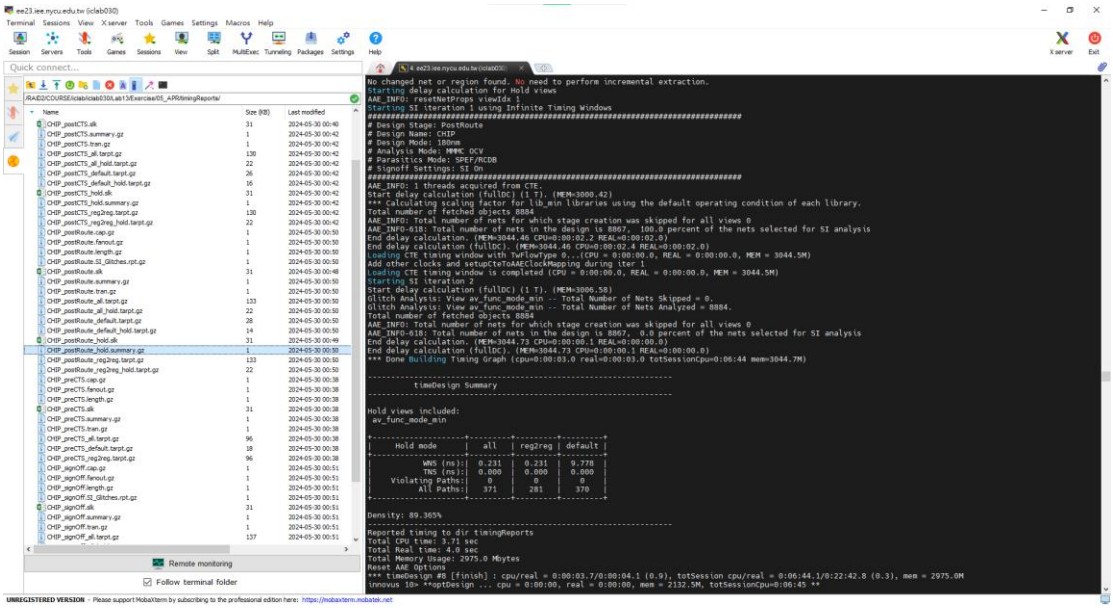




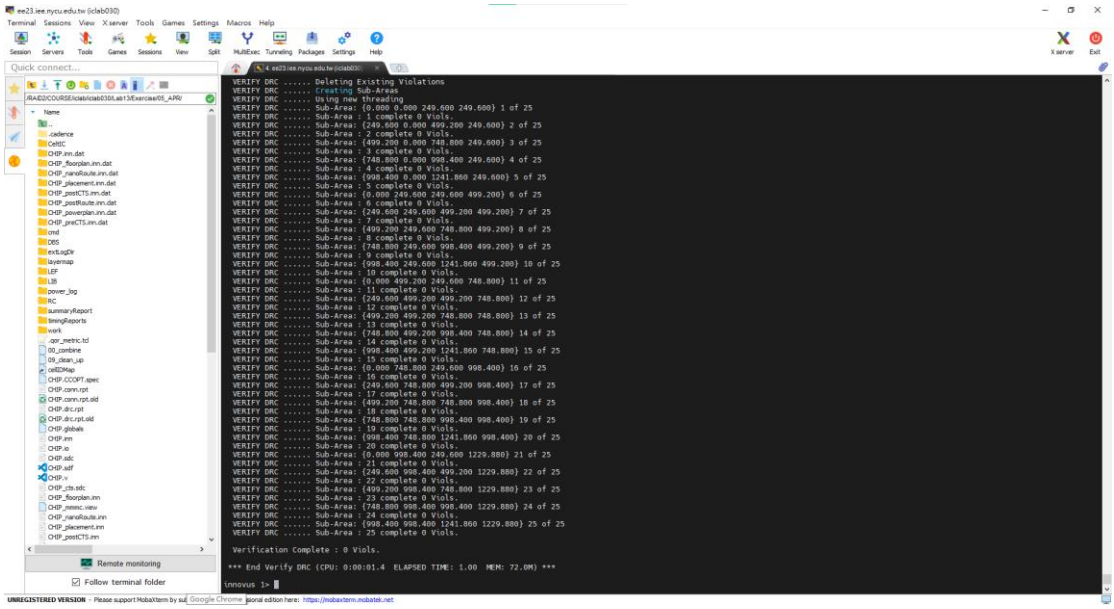
4. Post-Route setup time analysis :



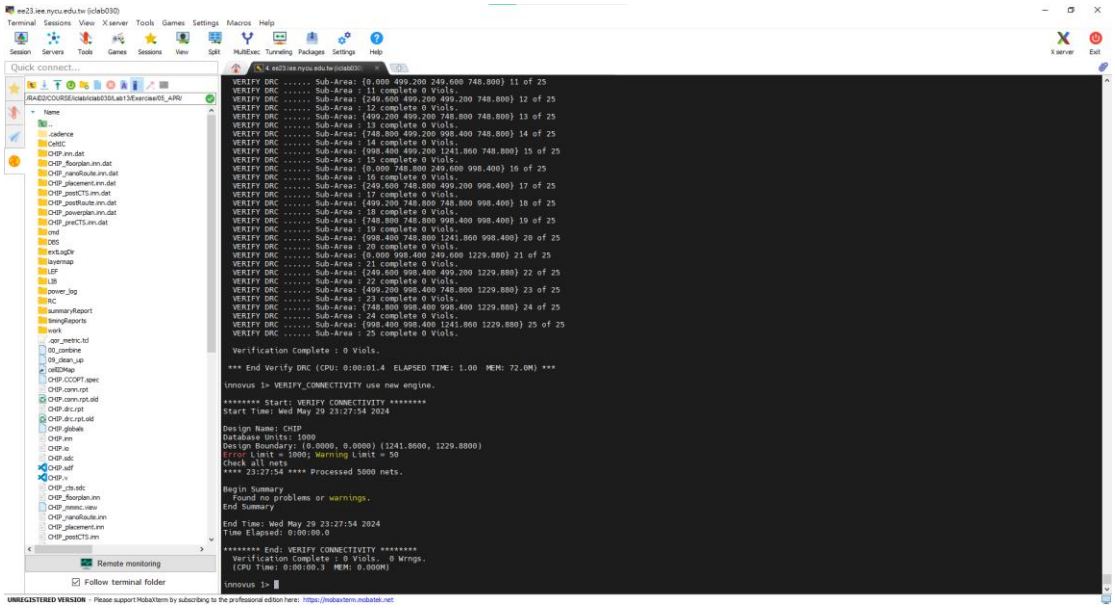
5. Post-Route hold time analysis :

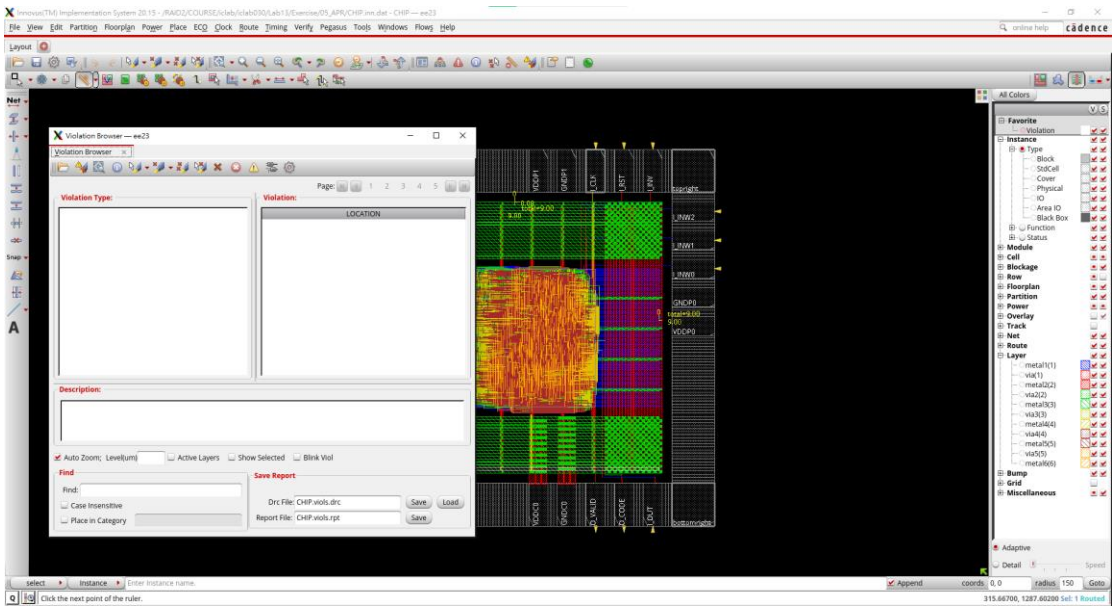


6. DRC result :

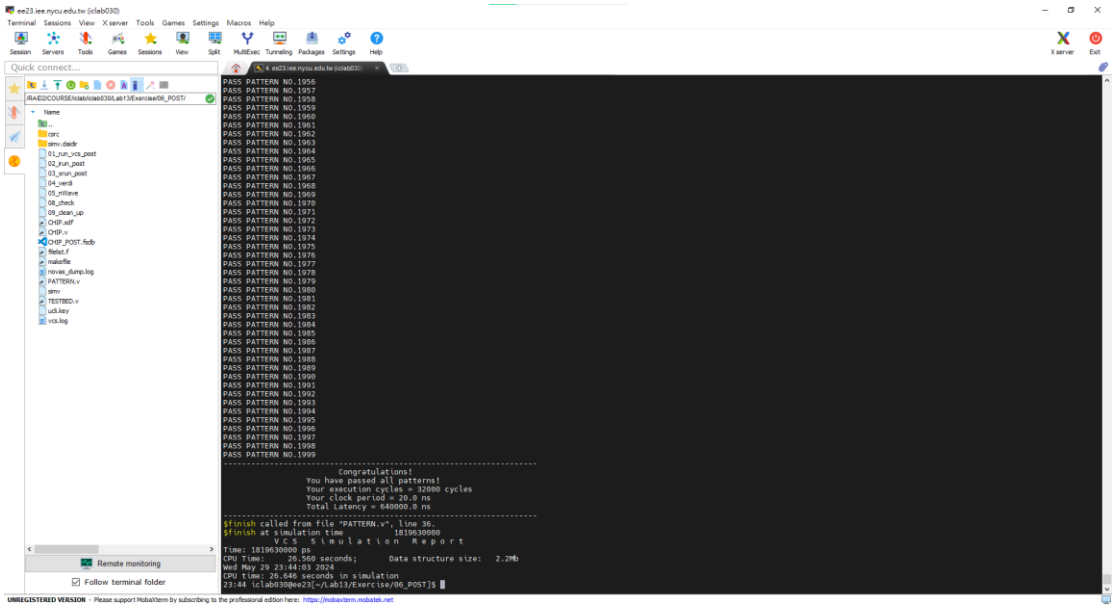

VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 249.600 249.600} 1 of 25
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {249.600 0.000 499.200 249.600} 2 of 25
VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {499.200 0.000 748.800 249.600} 3 of 25
VERIFY DRC ..... Sub-Area : 3 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {748.800 0.000 998.400 249.600} 4 of 25
VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {998.400 0.000 1241.860 249.600} 5 of 25
VERIFY DRC ..... Sub-Area : 5 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 249.600 249.600 499.200} 6 of 25
VERIFY DRC ..... Sub-Area : 6 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {249.600 249.600 499.200 499.200} 7 of 25
VERIFY DRC ..... Sub-Area : 7 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {499.200 249.600 748.800 499.200} 8 of 25
VERIFY DRC ..... Sub-Area : 8 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {748.800 249.600 998.400 499.200} 9 of 25
VERIFY DRC ..... Sub-Area : 9 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {998.400 249.600 1241.860 499.200} 10 of 25
VERIFY DRC ..... Sub-Area : 10 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 499.200 249.600 748.800} 11 of 25
VERIFY DRC ..... Sub-Area : 11 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {249.600 499.200 499.200 748.800} 12 of 25
VERIFY DRC ..... Sub-Area : 12 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {499.200 499.200 748.800 748.800} 13 of 25
VERIFY DRC ..... Sub-Area : 13 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {748.800 499.200 998.400 748.800} 14 of 25
VERIFY DRC ..... Sub-Area : 14 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {998.400 499.200 1241.860 748.800} 15 of 25
VERIFY DRC ..... Sub-Area : 15 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 748.800 249.600 998.400} 16 of 25
VERIFY DRC ..... Sub-Area : 16 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {249.600 748.800 499.200 998.400} 17 of 25
VERIFY DRC ..... Sub-Area : 17 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {499.200 748.800 748.800 998.400} 18 of 25
VERIFY DRC ..... Sub-Area : 18 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {748.800 748.800 998.400 998.400} 19 of 25
VERIFY DRC ..... Sub-Area : 19 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {998.400 748.800 1241.860 998.400} 20 of 25
VERIFY DRC ..... Sub-Area : 20 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 998.400 249.600 1229.880} 21 of 25
VERIFY DRC ..... Sub-Area : 21 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {249.600 998.400 499.200 1229.880} 22 of 25
VERIFY DRC ..... Sub-Area : 22 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {499.200 998.400 748.800 1229.880} 23 of 25
VERIFY DRC ..... Sub-Area : 23 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {748.800 998.400 998.400 1229.880} 24 of 25
VERIFY DRC ..... Sub-Area : 24 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {998.400 998.400 1241.860 1229.880} 25 of 25
VERIFY DRC ..... Sub-Area : 25 complete 0 Viols.
Verification Complete : 0 Viols.
*** End Verify DRC (CPU: 0:00:01.4 ELAPSED TIME: 1.00 MEM: 72.0M) ***
innovus 1>

7. LVS result :

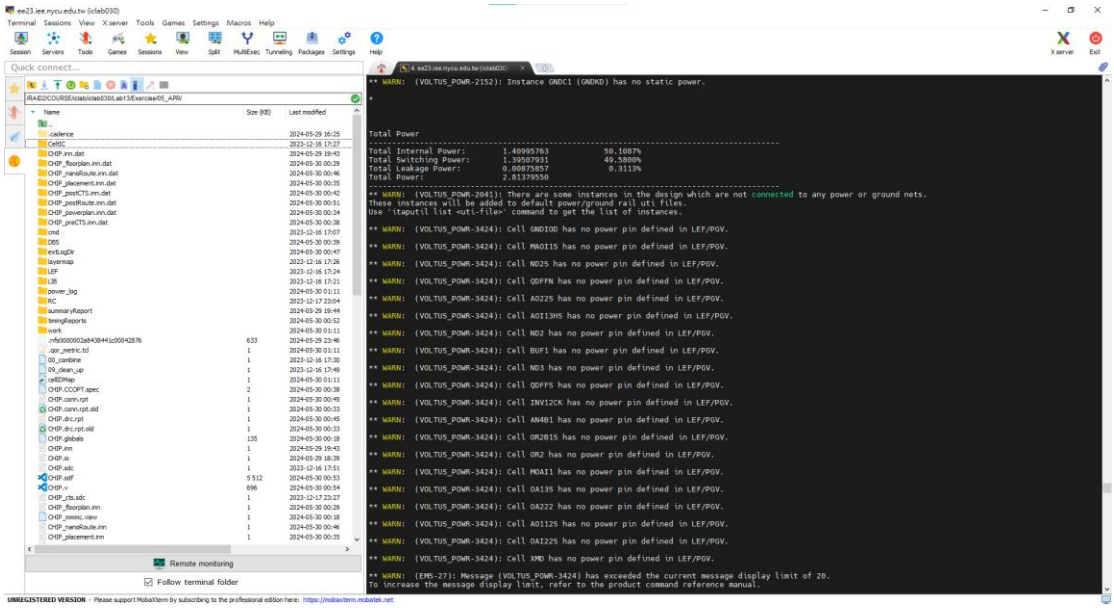

VERIFY DRC ..... Sub-Area: {0.000 499.200 249.600 748.800} 11 of 25
VERIFY DRC ..... Sub-Area : 11 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {249.600 499.200 499.200 748.800} 12 of 25
VERIFY DRC ..... Sub-Area : 12 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {499.200 499.200 748.800 748.800} 13 of 25
VERIFY DRC ..... Sub-Area : 13 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {748.800 499.200 998.400 748.800} 14 of 25
VERIFY DRC ..... Sub-Area : 14 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {998.400 499.200 1241.860 748.800} 15 of 25
VERIFY DRC ..... Sub-Area : 15 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 748.800 249.600 998.400} 16 of 25
VERIFY DRC ..... Sub-Area : 16 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {249.600 748.800 499.200 998.400} 17 of 25
VERIFY DRC ..... Sub-Area : 17 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {499.200 748.800 748.800 998.400} 18 of 25
VERIFY DRC ..... Sub-Area : 18 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {748.800 748.800 998.400 998.400} 19 of 25
VERIFY DRC ..... Sub-Area : 19 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {998.400 748.800 1241.860 998.400} 20 of 25
VERIFY DRC ..... Sub-Area : 20 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 998.400 249.600 1229.880} 21 of 25
VERIFY DRC ..... Sub-Area : 21 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {249.600 998.400 499.200 1229.880} 22 of 25
VERIFY DRC ..... Sub-Area : 22 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {499.200 998.400 748.800 1229.880} 23 of 25
VERIFY DRC ..... Sub-Area : 23 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {748.800 998.400 998.400 1229.880} 24 of 25
VERIFY DRC ..... Sub-Area : 24 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {998.400 998.400 1241.860 1229.880} 25 of 25
VERIFY DRC ..... Sub-Area : 25 complete 0 Viols.
Verification Complete : 0 Viols.
*** End Verify DRC (CPU: 0:00:01.4 ELAPSED TIME: 1.00 MEM: 72.0M) ***
innovus 1> VERIFY_CONNECTIVITY use new engine.
******** Start: VERIFY CONNECTIVITY ********
Start Time: Wed May 29 23:27:54 2024
Design Name: CHIP
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (1241.8600, 1229.8800)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 23:27:54 **** Processed 5000 nets.
Begin Summary
Found no problems or warnings.
End Summary
End Time: Wed May 29 23:27:54 2024
Time Elapsed: 0:00:00.0
******** End: VERIFY CONNECTIVITY ********
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.3 MEM: 0.000M)
innovus 1>
Remote monitoring
Follow terminal folder
UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: https://mobaxterm.mobatek.net


Violation Browser — ee23
Violation Type:
Violation:
LOCATION
Description:
Find:
Save Report
Drc File: CHIP.viols.drc
Report File: CHIP.viols.rpt
Save
Load
Favorite
Instance
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
Bump
Grid
Miscellaneous

8. Post Layout simulation result :



9. Power result :



10. IR Drop Results :

To address this problem, I distributed the power pads evenly in the middle of all four sides, ensuring balanced power distribution and providing even power supply at a minimum level.