u-boot satrtup sequence start.s start armboot main loop() run command() (arch/arm/cpu/hi3536/start.s) (common/main.c) (common/main.c) Command table reset main loop() (run_command() U-boot.lds specifles the start.o will be firstly link start.o,so bootm the entry of start.s is the u-boot entry. (arch/arm/cpu/hi3536/u-boot.lds) arch_cpu_init decjpg timer_init getinfo board_init install_auto_comple help interrupt_init i2c get_clocks parse_line() arse command, find toke loady env_init loadb and extract argumen init baudrate mtest CONFIG_BOOT_RETRY_TIMI loop init_sequence array one serial init nit_cmd_timeout() tendif base /* copy u-boot.bin from spi no flash to ddr */ console_init_f crc32 display_banner cmp print_cpuinfo ср mw checkboard u boot cmd end whitcl b copy_to_ddr /* r0 stores __reset offset fro where we get started. */ nm init_func_i2c mm Jsing macro U_BOOT_CMD to add a command into the dram_init md ext sect.*/ mii stopkey_confir arm_pci_init ping spi_flash_probe rarpboot retum 0 . Set the cpu to SVC32 mode tftp Disable irq and fiq Invalidate L1 I/D Invalidate L1 D-cache copy the u-boot.bin to ddr,if bootp he source address and the arget address is equal, it will be kip. */ setenv printenv end argc, argv) '* call function to do the saveenv BSS version * we just aNalysis the signel on the signel of the signel _bss_start Processing. run_command setvobg U-boot Image stopvl TEXT_BASE **SDRAM** (_armboot_start) startvl stopgx CFG_MALLOC_LEN Address startgx not repeatable, interrupte commands are always considered not repeatable stopvo GBL_DATA_SIZE gd points to globel startvo partinfo * jump to do_clr_remap */ *boot from bootrom,we copy ne uboot.bin to ram structure of gd t increase direction unrecognized, bootd recursion or too many args) If cmd is NULL or "" or long L. Set up the stack 2. Clear bss IRQ&FIQ Stack erasemtd /* Defined in User stack top bootlogo board/svr2730, ery important * nan CONFIG_SYS_CBSIZE-1 considered unrecognized) nbootm User Stack misc_init_r() appupdate SDRAM BASE conf0 sysupdate .. Do clear remap ..Set SMP bit ACTLR register to nable I cache and D cache for firmwareupdate bootupdate /* @ jump to C code, start_armboot difined in arch/ arm/lib/board.c +285*/ app0 7 and A17 ublupdate B. ddr_init I. init_registers /* init PLL/DDRC Flash ios0 allupdate pinfo envargs sysidx env defenv console 0x0000 0000 hiupdate Figure 1 U-boot memory layout hwinfo