



1. Description

1.1. Project

Project Name	bmsbq431R
Board Name	custom
Generated with:	STM32CubeMX 6.1.1
Date	02/06/2021

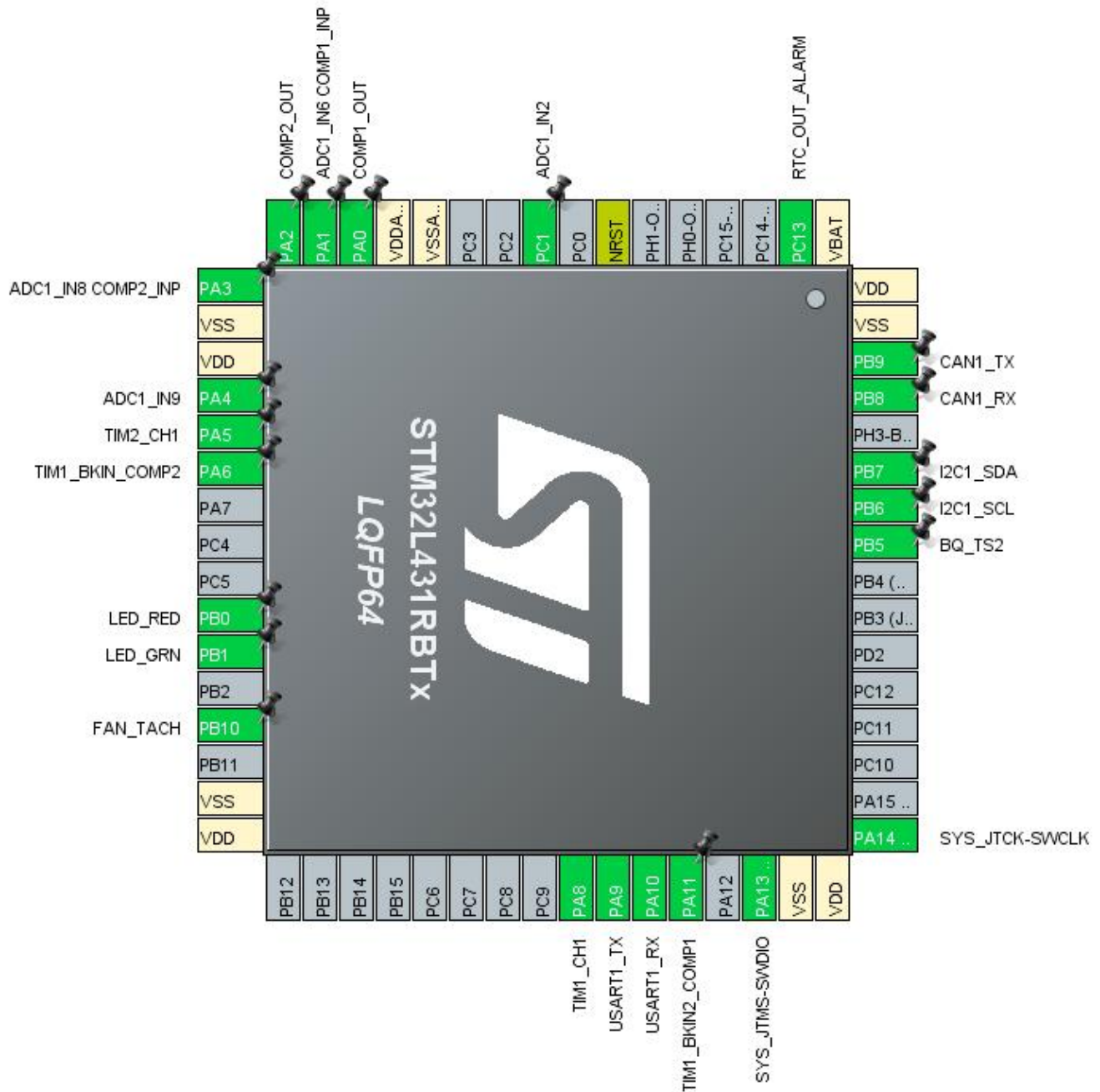
1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x1
MCU name	STM32L431RBTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4
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2. Pinout Configuration



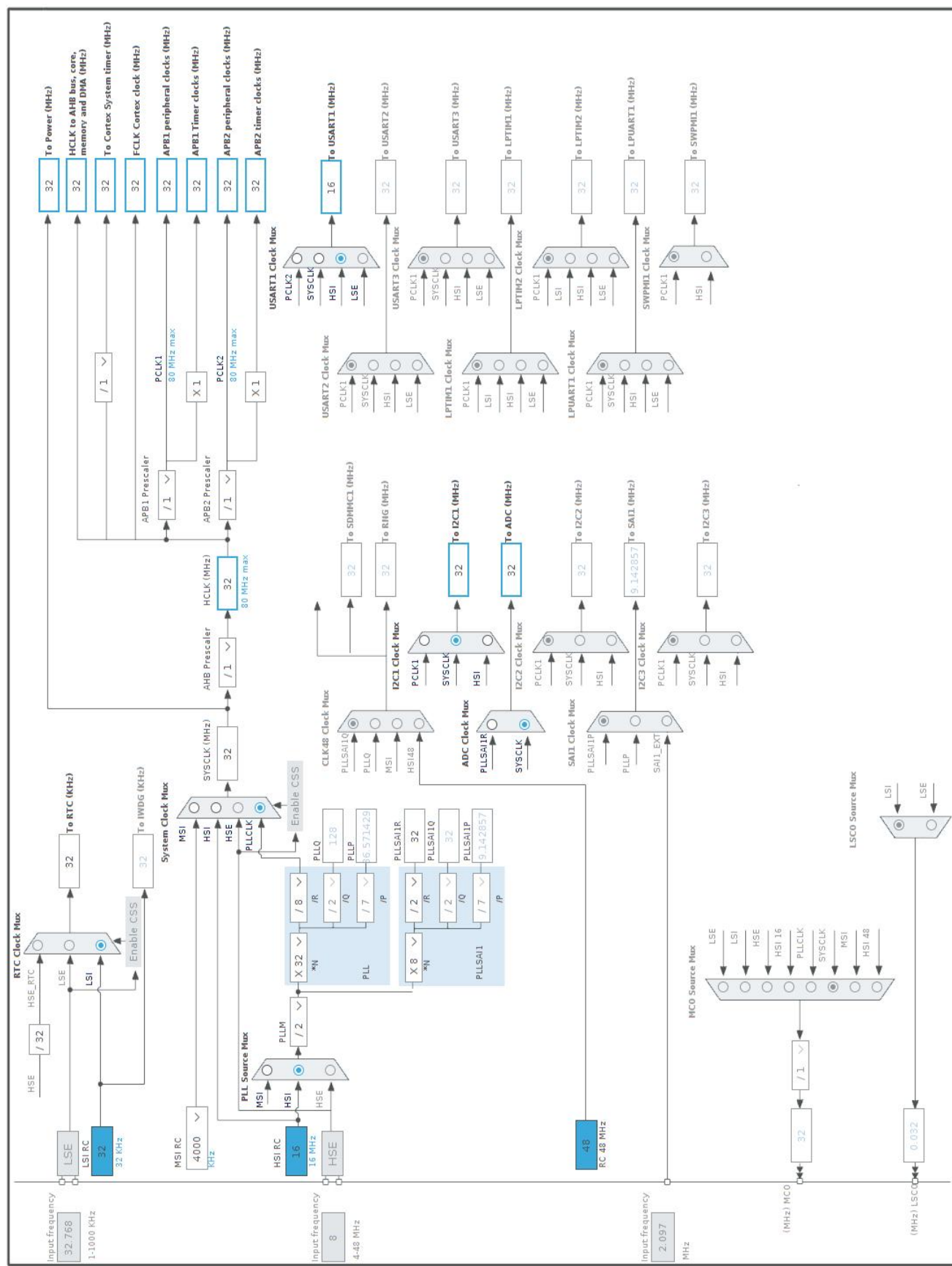
(Rotated +90°)

3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	RTC_OUT_ALARM	
7	NRST	Reset		
9	PC1	I/O	ADC1_IN2	
12	VSSA/VREF-	Power		
13	VDDA/VREF+	Power		
14	PA0	I/O	COMP1_OUT	
15	PA1	I/O	ADC1_IN6, COMP1_INP	
16	PA2	I/O	COMP2_OUT	
17	PA3	I/O	ADC1_IN8, COMP2_INP	
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	ADC1_IN9	
21	PA5	I/O	TIM2_CH1	
22	PA6	I/O	TIM1_BKIN_COMP2	
26	PB0 *	I/O	GPIO_Output	LED_RED
27	PB1 *	I/O	GPIO_Output	LED_GRN
29	PB10	I/O	TIM2_CH3	FAN_TACH
31	VSS	Power		
32	VDD	Power		
41	PA8	I/O	TIM1_CH1	
42	PA9	I/O	USART1_TX	
43	PA10	I/O	USART1_RX	
44	PA11	I/O	TIM1_BKIN2_COMP1	
46	PA13 (JTMS-SWDIO)	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDD	Power		
49	PA14 (JTCK-SWCLK)	I/O	SYS_JTCK-SWCLK	
57	PB5 *	I/O	GPIO_Analog	BQ_TS2
58	PB6	I/O	I2C1_SCL	
59	PB7	I/O	I2C1_SDA	
61	PB8	I/O	CAN1_RX	
62	PB9	I/O	CAN1_TX	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	bmsbq431R
Project Folder	/home/deh/GliderWinchItems/BMS/bmsbq431R
Toolchain / IDE	EWARM V8.32
Firmware Package Name and Version	STM32Cube FW_L4 V1.16.0
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_ADC1_Init	ADC1
5	MX_CAN1_Init	CAN1
6	MX_I2C1_Init	I2C1
7	MX_RTC_Init	RTC
8	MX_TIM2_Init	TIM2
9	MX_USART1_UART_Init	USART1
10	MX_COMP1_Init	COMP1
11	MX_COMP2_Init	COMP2

Rank	Function Name	Peripheral Instance Name
12	MX_DAC1_Init	DAC1
13	MX_TIM1_Init	TIM1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x1
MCU	STM32L431RBTx
Datasheet	DS11453_Rev1

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

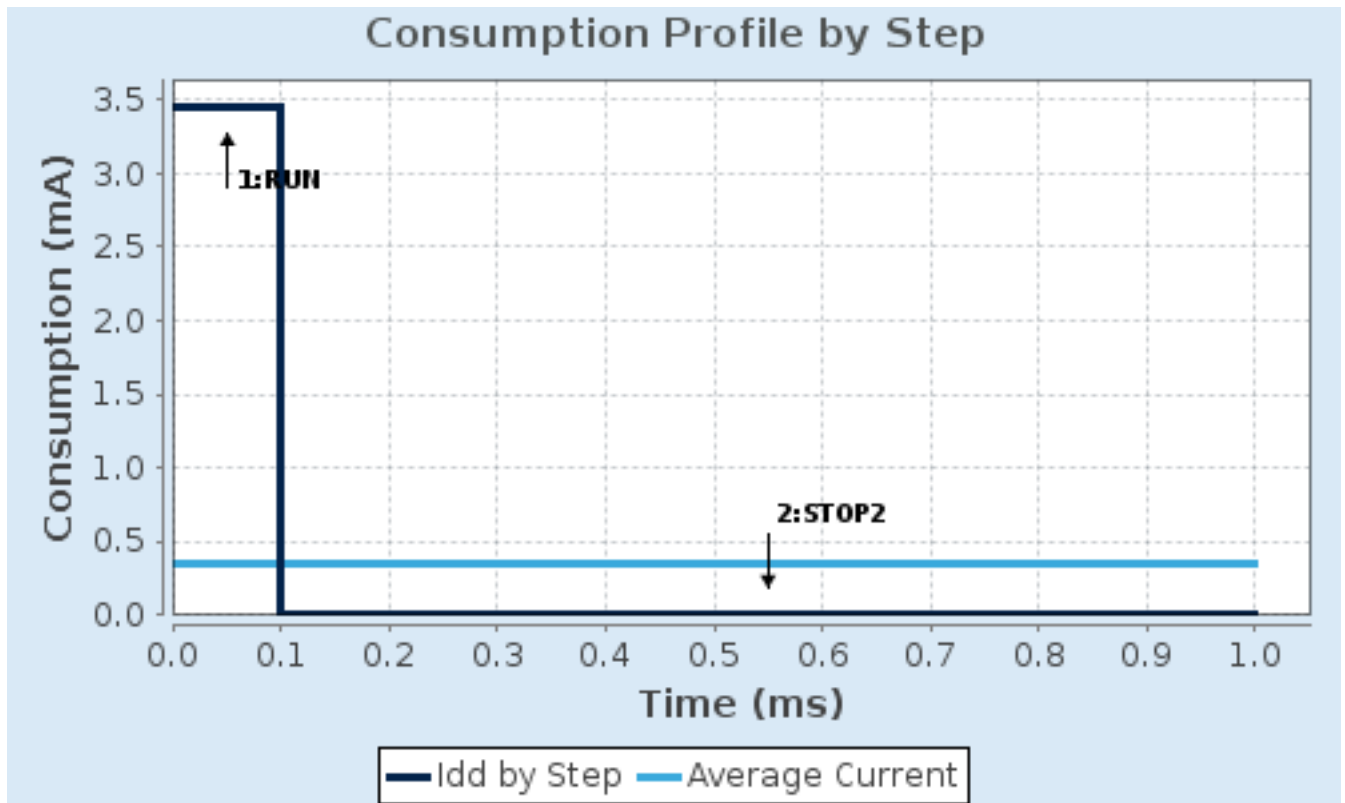
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	FLASH	n/a
CPU Frequency	32 MHz	0 Hz
Clock Configuration	HSE BYP ART	ALL CLOCKS OFF
Clock Source Frequency	32 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	3.46 mA	1.06 μ A
Duration	0.1 ms	0.9 ms
DMIPS	40.0	0.0
Ta Max	104.53	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	346.95 μ A
Battery Life	1 year, 1 month, 8 days, 12 hours	Average DMIPS	40.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1

IN2: IN2 Single-ended

IN9: IN9 Single-ended

mode: Vrefint Channel

7.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
<u>Rank</u>	1
Channel	Channel Vrefint *
Sampling Time	2.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable
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Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false
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Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false
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Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false
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7.2. CAN1

mode: Activated

7.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	16
Time Quantum	500.0 *
Time Quanta in Bit Segment 1	1 Time
Time Quanta in Bit Segment 2	1 Time
Time for one Bit	1500.00 *
Baud Rate	666666 *
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal
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7.3. COMP1

mode: Input [+]

Input [-]: DAC OUT1

mode: ExternalOutput

mode: External Output to TIM1 BKIN2

7.3.1. Parameter Settings:

Basic Parameters:

Speed / Power Mode	High Speed
Trigger Mode	None
Hysteresis Level	None

Output Configuration:

Blanking Source	None
Output Pol	COMP output on GPIO isn't inverted

7.4. COMP2

Input [+]: INP

Input [-]: DAC OUT2

mode: ExternalOutput

mode: External Output to TIM1 BKIN

7.4.1. Parameter Settings:

Basic Parameters:

Speed / Power Mode	High Speed
Trigger Mode	None
Hysteresis Level	None

Output Configuration:

Blanking Source	None
Output Pol	COMP output on GPIO isn't inverted

7.5. DAC1

OUT1 mode: Connected to on chip-peripherals only

OUT2 mode: Connected to on chip-peripherals only

7.5.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Disable
Trigger	None
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

DAC Out2 Settings:

Output Buffer	Disable
Trigger	None
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

7.6. I2C1

I2C: I2C

7.6.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Fast Mode *
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x00300F38 *

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.7. RCC

7.7.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	1 WS (2 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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7.8. RTC

mode: Activate Clock Source

mode: Activate Calendar

Alarm A: Routed to OUT

7.8.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255
Output Polarity	Output Polarity High
Output Type	Output Type Opendrain

Calendar Time:

Data Format	BCD data format
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	Monday
Month	January
Date	1
Year	0

Alarm A:

Hours	0
Minutes	0
Seconds	0
Sub Seconds	0
Alarm Mask Date Week day	Disable
Alarm Mask Hours	Disable
Alarm Mask Minutes	Disable
Alarm Mask Seconds	Disable
Alarm Sub Second Mask	All Alarm SS fields are masked.
Alarm Date Week Day Sel	Date
Alarm Date	1

7.9. SYS

Debug: Serial Wire

Timebase Source: TIM15

7.10. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable
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PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.11. TIM2

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel3: Input Capture direct mode

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable
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PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

Input Capture Channel 3:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.12. USART1

Mode: Asynchronous

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	8 Samples *
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC1	ADC1_IN2	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA1	ADC1_IN6	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA3	ADC1_IN8	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA4	ADC1_IN9	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
CAN1	PB8	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB9	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
COMP1	PA0	COMP1_OUT	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	COMP1_INP	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA11	TIM1_BKIN2_COMP1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
COMP2	PA2	COMP2_OUT	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	COMP2_INP	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA6	TIM1_BKIN_COMP2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	Very High *	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	Very High *	
RTC	PC13	RTC_OUT_ALARM	n/a	n/a	n/a	
SYS	PA13 (JTMS-SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK-SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA5	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	TIM2_CH3	Alternate Function Push Pull	Pull-up *	Low	FAN_TACH
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
GPIO	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_RED
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_GRN
	PB5	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	BQ_TS2

8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA1_Channel5	Peripheral To Memory	Low
USART1_TX	DMA1_Channel4	Memory To Peripheral	Low

USART1_RX: DMA1_Channel5 DMA request Settings:

Mode: **Circular ***
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

USART1_TX: DMA1_Channel4 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel4 global interrupt	true	0	0
DMA1 channel5 global interrupt	true	0	0
TIM1 break interrupt and TIM15 global interrupt	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 global interrupt	unused		
CAN1 TX interrupt	unused		
CAN1 RX0 interrupt	unused		
CAN1 RX1 interrupt	unused		
CAN1 SCE interrupt	unused		
TIM1 update interrupt and TIM16 global interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
USART1 global interrupt	unused		
RTC alarm interrupt through EXTI line 18	unused		
TIM6 global interrupt, DAC channel1 and channel2 underrun error interrupts	unused		
COMP1 and COMP2 interrupts through EXTI lines 21 and 22	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
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Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 channel4 global interrupt	false	true	true
DMA1 channel5 global interrupt	false	true	true
TIM1 break interrupt and TIM15 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware						
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA ✓	ADC1 ✓	RTC ✓	CAN1 ✓			
GPIO ✓	COMP1 ✓	TIM1 ✓	I2C1 ✓			
NVIC ✓	COMP2 ✓	TIM2 ✓	USART1 ✓			
RCC ✓	DAC1 ✓					
SYS ✓						

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00257211.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00151940.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00218224.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00085385.pdf
Application note	http://www.st.com/resource/en/application_note/DM00087593.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00156964.pdf
Application note	http://www.st.com/resource/en/application_note/DM00150423.pdf
Application note	http://www.st.com/resource/en/application_note/DM00209748.pdf

Application note http://www.st.com/resource/en/application_note/DM00125306.pdf

Application note http://www.st.com/resource/en/application_note/DM00141025.pdf

Application note http://www.st.com/resource/en/application_note/DM00144612.pdf

Application note http://www.st.com/resource/en/application_note/DM00148033.pdf

Application note http://www.st.com/resource/en/application_note/DM00209768.pdf

Application note http://www.st.com/resource/en/application_note/DM00216518.pdf

Application note http://www.st.com/resource/en/application_note/DM00220769.pdf

Application note http://www.st.com/resource/en/application_note/DM00227538.pdf

Application note http://www.st.com/resource/en/application_note/DM00257177.pdf

Application note http://www.st.com/resource/en/application_note/DM00269143.pdf

Application note http://www.st.com/resource/en/application_note/DM00272912.pdf

Application note http://www.st.com/resource/en/application_note/DM00226326.pdf

Application note http://www.st.com/resource/en/application_note/DM00236305.pdf

Application note http://www.st.com/resource/en/application_note/DM00260952.pdf

Application note http://www.st.com/resource/en/application_note/DM00263732.pdf

Application note http://www.st.com/resource/en/application_note/DM00269146.pdf

Application note http://www.st.com/resource/en/application_note/DM00327191.pdf

Application note http://www.st.com/resource/en/application_note/DM00355687.pdf

Application note http://www.st.com/resource/en/application_note/DM00311483.pdf

Application note http://www.st.com/resource/en/application_note/DM00354244.pdf

Application note http://www.st.com/resource/en/application_note/DM00367673.pdf

Application note http://www.st.com/resource/en/application_note/DM00315319.pdf

Application note http://www.st.com/resource/en/application_note/DM00380469.pdf

Application note http://www.st.com/resource/en/application_note/DM00354333.pdf

Application note http://www.st.com/resource/en/application_note/DM00395696.pdf

Application note http://www.st.com/resource/en/application_note/DM00445657.pdf

Application note http://www.st.com/resource/en/application_note/DM00493651.pdf

Application note http://www.st.com/resource/en/application_note/DM00536349.pdf

Application note http://www.st.com/resource/en/application_note/DM00209772.pdf

Application note http://www.st.com/resource/en/application_note/DM00476869.pdf

Application note http://www.st.com/resource/en/application_note/DM00660597.pdf

Application note http://www.st.com/resource/en/application_note/DM00725181.pdf