**A. Overview**

Two boards are used to monitor, charge, and balance a battery module of up to 18 cells. One board carries a low current charger, power isolation, and CAN interfacing. The second board carries STM32F4 processor and LCT6813-1 BMS chips. The two boards stack and are connected with two 1x30 headers at each edge.

The top of the top board carries the headers for the more frequently changed external board connections. The I2C header is on the bottom of the bottom board.

Each cell of the battery module is connected to the charger (top) board via 20 pin ribbon cable to an IDC type connector. (18 cell wires plus two wires to battery module ground).

A bus with 12v nominal, ground, and CAN signals connects to each battery module unit. A 10 pin ribbon cable connects the connectors on the battery box (9 pin D) to the charger board.

There are provisions for other features--

- FET drive for a resistor to by-pass current across the entire battery module.

- UART header for debugging (FTDI, JP4).

- Header for STLink program loading/debugging (SWD) (JP5) .

- Two FET driven, external LEDs, JP8.

- Three thermistors, JP10

- One Hall-effect (or 5v sensor) (JP7)

The two pcbs are 140x45mm and designed fit in the space between the batterys and front of the battery box. The 20 pin ribbon cable splits with one half going to the top of the battery array, and the other to the bottom half.

**B. Power chain: bmschgrR.sch (top board) & bmsbmsR.sch (bottom board)**

The main power for the unit is from the CAN bus +12v (nominal) and this references to “system” or CAN bus ground. This battery module electronics is isolated from the CAN bus ground.

The following is the chain (more detail follows)--

CAN bus +12 main input drives

1) linear 5v for CAN bus side CAN interface

2) dc-dc converter (12→15v) with isolation drives,

a) dc-dc (15v→75v) low current charger

b) dc-dc (15v→7v) drives,

(1) bms/transistor regulator

(2) linear 5v

(3) dc-dc (7v→3.3v) processor

**CAN bus ground referenced (AGND on top board schematic)**

Referring to the schematic, the +12 (nominal) from the CAN bus is reverse polarity checked by the FET U$1. The 0.1 ohm (R33) resistor in series is provides a test point for measuring current .

The +12v drives a 7805L linear regulator (IC2) to provide +5v for the CAN bus side of the unit. The +5v drives the CAN bus side of the CAN interface (ISO1050) and logic for fan control. There are several configurations of fans that can be accommodated, with the common feature that the FET driving the fans is at CAN bus side ground and the control is isolated and driven from the processor at battery module ground.

+12 drives a dc-dc converter CUI, Inc, PYBJ6-D12-S15 (U$2) that isolates the +12v on the CAN bus side from +15v on the battery module side. U$2 regulates as well as isolates.

+12v drives LED2 to indicate that 12v is present on the CAN bus side.

**Battery module ground referenced (GND on schematic)**

+15v is converted to lower voltages for the BMS and processor circuits. There are two sources for the +15v. One is the dc-dc converter from the top board which isolates the CAN bus +12 power. The other source is from the battery module itself (more detail described later.)

The +15v diode OR’ed from the top board (CAN bus) or battery module powers the following features--

- 7805L linear regulator (IC1) which provides +5v for the battery module side of the CAN interface (ISO1050).

- DC-DC boost driver (MCP1401|1416) and FET U$12 to produce the a high voltage for lower current charging the entire battery module.

- Power to the bottom board (bmsbmsR.sch) where the +15v is converted to lower voltages for the processor and bms chips (via pin 1 on JP2 on the bottom edge 1x30 header).

– A dc-dc converter reduces the +15v to +7v. The board layout provides three options for this dc-dc converter. The least expensive, but largest footprint, is based on a LM2596.

- The +7 drives a LM7805L. The +5 output goes to the Hall-effect header, I2C bus, thermistor sensors and pin 25 of the top 1x30 header (connecting to +5 on the top board). (Note: there is a redundancy with LM7805Ls on both the top an bottom boards. Better would be to drive the I2C +5 from the top board via pin 25 and have the analog Hall effect, and thermistor +5 from the bottom board LM7805L.)

- The +7v goes to the collector of a NPN transistor (Q3) that forms part of the LTC6813-1 5v regulator.

- The +7v drives a dc-dc converter to produce 3.3v for the processor. Provisions is for two dc-dc converter modules. One is the LM2596 based module. The other is the minibuck.

More detail--

- Header for I2C bus which could be used for a LCD display, or port extension for pushbuttons and LEDs.

**C. BMS board bmsbmsR.sch (bottom board) features**

**C.1 Power supply chain voltage measurements**

The processor ADC is used to monitor power supply voltages.

a. +15 Or’ed voltage (drives dc-dc boost charger and rest of chain)

R47/R48 PC3

b. +7

R49/F51 PC5

c. +5

R44/R45 PC2

d. Total battery module

Depending on the parts fitted, the battery module total voltage can be measured with the following, however the external dump resistor control is not possible. Furthermore, the total battery module voltage can be generated by totaling the individual cell readings.

(R37+R56)/R38 PA1

**C.2 BMS GPIO**

Usage of the nine available bms gpio pins (16b ADC)--

The measurement of the 5v supply is used in conjunction with the thermistors and Hall-effect to make the measurements ratiometric with respect to the 5v supply.

gpio1 – 5v supply to thermistors and 5v sensor (e.g. Hall-effect)

R25/R50

gpio2 – thermistor #1

R26

gpio3 – thermistor #2

R27

gpio4- thermistor #3

R28

gpio5 – Hall-effect

R29

The following are for future possibilities--

gpio6 – thru-hole pad R33→gnd

gpio7 – thru-hole pad R53/R34

gpio8 – thru-hole pad R35 →gnd

gpio9 – thru-hole pad R36 → gnd

**C.3 I2C bus**

The I2C bus, I2C2, is brought out to 1x4 header JP3 pins--

1) gnd

2) +5

3) PB8 SDA with pullup, R23

4) PB9 SCK with pullup, R24

**C.4 Processor—STM32F405RxT6 or STM32F446RxT6**

Pinouts are “mostly the same” between the two processors. The differences are in the on-chip power pin by-passing.

PB11 connects to 4.7u cap, CP2, for F446 and is open and available as i/o pin for F405.

Capacitor pads for CP1 and CP3 are zero ohm for F405 and 4.7u for F446.

**C.5 BMS LTC6813-1**

Regulated 5v for internal chip derives from NPN transistor (Q3), with +7v on the collector and the base driven by the internal feedback. The transistor base provides 5v for the bms. R19/C6 provides filtering of the 7v, as recommended in the datasheet.

Communication of the processor with bms is via spi and other control lines--

PA2 – BMS WDT

PA4 – SPI1 NSS BMS CSB/IMA

PA5 – SPI1 SCLK

PA6 – SPI1-MOSI (?) BMS SDO with R46 4.7K pullup

PA7 – SPI1-MISO (?) BMS SDI

Cell connections--

R1 – R18 and CC1 through CC18 provide ADC sense filtering with the time-constant recommended in the datasheet. (Note: by-pass current limiting resistors and external fets reside on the top board.)

**C.6 Battery dump**

Provision is made for an external power resistor for by-passing current across the total battery. Several configurations can be implemented depending on the parts fitted.

For a straight turn-on/turn-off via FET, Q10, R38, 1M, will hold assure the FET is off when the processor is not powered. PA1 will drive the FET, but the FET needs a low g-s turn-on voltage since the PA1 will only rise to about 3v. R57 is fitted with zero ohms to ground the FET source. The FET drain on JP2 pin 3 would go to the dump resistor, and the other side of the resistor to the battery module plus directly (not via the ribbon cable). Pin 4 on JP3 would go to the battery module minus (GND).

Modification of the foregoing to provide current sensing can be made by fitting R57 with a small resistance. Via R31, PA3 can measure the voltage drop across for R57 to measure current, however the voltage drop will be small so the resolution will be poor.

As mentioned earlier, the total battery module voltage can be measured by other fittings of the parts. Alternately, the +15 from the top board, i.e. before OR’ing, can be measured.

**C.7 Battery module powering**

The provision for powering the bms from the battery module allows slow discharge for long term storage without the need for a 12v CAN power bus. A pushbutton on the module box is pressed while the unit is powered from the CAN bus. The program then maintains the bms board (no charger of course) until the discharge has completed at which time a FET connecting the battery to the bms is turned off. Once off, the external pushbutton will not activate the unit.

Thru-hole pads U$13,14,15 allow selection of 3 or 4 battery cells. The NFET/PFET pair, QQ100, is acts as a power switch to connect the cells to the power chain and diode OR’s with the +15v from the dc-dc converter. PA0 drives the NFET of the QQ100 pair, and is pulled to GND with R32. Pressing the external pushbutton connected to JP11 signals the processor as well as turns on the QQ100 FET switch.

Since the pushbutton is a pull-up, Vcc must be present. Therefore, the bms has to be powered from the CAN bus for the switch to present. Once the switch is active the program must configure PA0 for output and hold it high until the discharge is complete. When the program drops PA0 the power drops and the bms is dead. Pressing the pushbutton in this state will not start the program since there will be no Vcc for the pushbutton pullup.

**C.8 Misc**

**Onboard LED--**

Shows Vcc present: LED1 – R59-Vcc

**Heat sinking--**

A large via is located under the LTC6813-1. This allows soldering to the heat sink pad on the bottom of the part. When the LTC6913-1 internal FETs are used for balancing substantial heat is generated from the relatively high FET Rdon resistance. The bottom of the board is mostly clear so that a piece of copper can be soldered to that via for addition heat sinking.

**D. Charger board: bmschgrR.sch (top board) features**

The charger board provides the some of the power chain (covered in the foregoing), and cell balancing resistors and fets, plus some misc provisions.

**D.1 DC-DC charger**

The +15v from the dc-dc converter that isolates from the CAN bus ground drives a dc-dc boost to generate a charging current. The program controls the switching of FET, U$12, which switches the inductor, U$4, to produce a high voltage via diode U$7. Zener, U$10, limits the voltage should the battery module cable not be connected. Capacitors C8, C9, provide a small amount of filtering for the open circuit situation. Resistor R31 and JP11 provide a means for test and calibration of the current. The gate driver MCP1401|1416 via gate resistor R1 drives the FET.

The processor drives the gate driver and monitors the +15 voltage and and high voltage generated. If the power drain exceeds the CAN bus dc-dc isolation converter (U$2) power limit the dc-dc converter will drop the +15v and the program can back off. If the high voltage exceeds the maximum battery module voltage, it is assumed the battery cable is not connected and the switching terminated. Program development and test will determine if these features are needed.

Resistor R29 assures that the gate driver will not turn on the FET, thus shorting the +15v via the inductor if the bottom board is not plugged in, or the program is not operating.

R5|R6 divides the +15v from the dc-dc converter (before OR’ing on the bms board), and passes that to pin 11, on the (bottom) 1x30 header, JP2, to the bms board (bottom) PC0 for measurement of the dc-dc converter output voltage.

R28|R27 divides the charger boost voltage. The divider passes that to pin 12 on the (bottom) 1x30 header, JP2, to the bms board (bottom) PC1 for measurement.

**D.2 Balancing by-pass resistors and FETS**

The LTC68123-1 on the bmsbmsR board (bottom) passes the “sense” and cell lines up to the bmschgrR board via the two 1x30 headers. The resistors for by-passing the current on a cell are on the bmschrgR board. Provision is to either use a low current balancing with the internal FETs in the LTC6813-1 or higher current using external FETs on mounted on the bmschgrR board.

The board layout allows for external or internal FET by-passing. For internal FET by-passing it implements the circuit shown in Fig 38 (a) in the LTC6813-1 datasheet. For external FET by-passing it implements the circuit shown in Fig 35 (a). The RC values are on the bmsbmsR board (bottom) and the by-passing resistors and FETs are on the bmschgrR board (top).

To minimize board space the by-passing resistor, e.g. R$2, was given a footprint with three pins. The resistor mounts vertically for better cooling, and one lead of the resistor can go to either of two holes on the pc board. E.g. for external FET by-passing R$2 has one lead common to external or internal FET by-passing connected to the 10 ohm resistor that goes to C1 (cell #1). The other R$2 lead connects to the source of F$2. For internal by-passing that lead would connected to S1 instead of the drain on FET F$2. The FET gate resistor is not needed for internal by-pass mode.

**D.x Misc**

**Master reset--**

A CAN bus line, pin 6, in 2x5 IDC connector, is for a master reset. The intention is that pulling this line to ground will reset all the processors on the CAN bus. This line connects to the CAN bus +12v and via R30 energizes opt-isolator, U$13, which via the 1x30 header resets the processor on the bms (bottom) board. Diode, D3, protects the opto-isolator from reverse voltages on the CAN bus line.

**LEDs--**

JP8 provides for two external leds, driven by two FETs

Pin 1 Q2, R2, 1x30 header (bottom) pin 6 (PC11)

Pin 2 Q3, R4, 1x30 header (bottom) pin 7 (PC10)

Pin3 +5v

Onboard LED1 is also driven from the 1x30 header pin 7 (PC10), via resistor R7.

**UART/FTDI--**

JP4 presents USART1 for a USB-serial cable.

Warning: this is not isolated from the battery module.