**A. Overview**

**directory: GliderWinchItems/BMS/docs/description**

**file: bmsbmsBQ\_TI\_BQ76952\_description.docx**

**eagle directory: GliderWinchItems/BMS/hw/eagle/bmsbmsBQ**

**file: bmsbq.sch,brd**

The following provides a description and some of the thinking in the pcb design. The design intends to provide a number of hardware configuration options. Some of these are to facilitate testing and program development and would not be needed in a later refined design. Provisions have been included a number of places for implementing the same function using alternate parts that have differing footprints, e.g. a 8 pin and 16 pin isolated CAN driver packages.

This bms connects to a 16 series cell battery module. Multiple battery modules (e.g. six or seven) are connected in series to make a battery string. Hence, a battery string would use six or seven of these bms boards. The boards communicate and get their power via a CAN bus cable, though there is an option for running off the battery module power, which might be required for discharging for storage. This CAN bus cable carries the two CAN signals, “system” ground and system 12v (nominal), plus a signal line for a master reset. In addition to the CAN bus nodes for the battery module bmses there will be a CAN node that is the “energy management controller” (EMC), though some other node might provide the EMC functions for the early implementations.

Since the battery string is not grounded to the system and floats, or is lightly biased via very large resistors, all of the battery modules and therefore the bmses are isolated from the system ground. The bms board processor and bms ic ground is at battery module minus level and isolated from system ground. The CAN drive, FAN control, master reset, dc-dc power, are at system ground. More detail on this later.

This board can accommodate a STM32F405RxT6, STM32F446RxT6, or STM32L431RxT6 processors. These are all 64 pin LPFQ packages. There small differences in the power pins so there is provision of the pcb for zero ohm or capacitors in several locations. The main target processor is the ‘L431. This processor has comparator and op-amp features that are not available in the ‘F405 or ‘F446, and is somewhat lower power as well, but less sram. The pcb layout allows the comparators and op-amp in th ‘L431 to be used for controlling the on-board charger.

The BMS controller is the Texas Instruments BQ76952, in a 48 pin LPFQ package. There are no alternatives and the design revolves around this part.

The main features of this bms design are--

- Low current battery module charger (approximately 80 ma)

- Cell-by-cell voltage measurement

- Cell-by-cell discharging

- Thermistors (at least three planned)

- FET to discharge entire module at low current via a resistor

- FET to turn on battery module heater (high current)

- FAN controller (on/off/pwm)

- FET (spare) to turn on/off something external.

- Headers for external pcb for external FET cell-by-cell discharging

- Header for I2C bus (3.3v)

- Header for spare I2C bus (5.0v)

- Header for two external processor controlled LEDs

- Header for SWD (ST’s Single Wire Debugger, non-isolated!)

- Header for UART (non-isolated!)

The files for this project are on github repository--

https://github.com/GliderWinchItems/BMS

The files of interest for the board design described here, within the repository, can be found at

hw/eagle/bmsbmsBQ/bmsbq.sch and ‘.brd.

The general board layout has three ground plane sections. The leftmost (as viewed in eagle .brd) is the system ground (and 12v, etc.). The middle section is processor ground (which is at battery module minus level) and the right section the BQ76952 bms wiring (which is also at battery module minus level). The processor ground and BQ ground are connected at one point to reduce the effect of digital noise from the processor with the BQ adc measurements.

**Note:** The eagle file was renumbered with the prefix “100” for parts on the underside layer.Later part additions retain the top/bottom “100” prefix but may not correspond to the location strategy the eagle renumbering script uses whereby the part numbers start at a board corner and work up and across.

**Note:** The term “shutdown” can have a number of meanings. For the processor it can be a low power mode where everything, except the RTC domain, is stopped (and Vcc is present). Another use of the term could be when the processor Vcc is not present. For the BQ76952, shutdown is a low power mode where most features are turned off, and though connected to the battery module, the current drain is less than 1 ua.

**Note:** Values of resistors, capacitors are tentative and subject to change during development.

**B. CAN bus cable connections**

A 10-pin ribbon with IDC type plug plugs into the bms board with a 2x5 keyed header. At the other end it is crimped into a 9-pin female D connector and a short distance onward to a male D connector. These 9 pin D connectors are mounted on the battery module box. CAN bus cables daisy-chain the battery modules together. Having the chain form a ring allows cutting the current drop in the power carrying wires in half. To reduce voltage drop in the ribbon cable the plus and minus wires are tripled.

The following ribbon pin assignments (should!) correspond to the 9-pin D connector and attempts to match the typical CAN assignments for 9-pin connectors. The header on the pcb is JP6--

1 – system +12V

2 – system ground

3 – CAN L2

4 – CAN H2

5 – system ground

6 – master reset

7 - system +12V

8 - system +12V

9 - system ground

10 - unused

**12v polarity protection--**

Reverse polarity protection on the 12v system power is provide by a pfet (FET103). The FET blocks if the +12v and system ground are reversed.

**Input current measurement--**

For development and test purposes, a thru-hole 0.1 ohm series resistor (R5) allows for measuring the current input.

**Master reset--**

The master reset line is used to reset the processors on the CAN nodes, i.e. reboot. This might be used to reset for program re-loading over CAN, or simply restart during development.

The master reset line in the CAN bus cable drives a H11L1S opto-coupler (OPT101). Pulling the master reset line to system ground turns on the opto-coupler and pulls the NRST (reset) line on the processor to ground. The 3.3K, R121 resistor on the opto input limits the current on the input, and the 10K, R8, pull-up resistor holds the NRST line normally high. The pushbutton allows manually resetting the processor. Diode D5 on the opto input protects against reverse polarity.

**LED-12V power--**

LED1, 6.8K, R2 indicates that 12V power (of correct polarity) is present.

**CAN 5v supply (5V/2)--**

From the 12v power, the AP7380Y (REG1) linear regulator supplies 5v to the system side of the isolated CAN driver (ISO1042); eagle net designation 5V/2. C121, 4.7u, and C108, 4.7u, provide the necessary input/output capacitors for the regulator.

**FAN 12v supply--**

Given that the cooling fan(s) are spec’d at 12v +/- 10%, but the system 12v will at times be 13.8v or even higher, a regulator is provided to limit the voltage to the FAN(s). There are two regulator options. One is the LDK320 (REG3A) which is a SOT-89 package, which has a low quiescent current, but may not be available. The other is the venerable LM7812T (REG3B) which is a TO-220 package, but has an 8 ma quiescent draw. The regulator uses C1, 1u for the output, and shares C3 (1u), C122 (4.7u), C121 (4.7u) on the +12 protected line.

The regulated FAN 12 goes to a 4 pin header (JP5)--

1 – system ground

2 – FAN regulated +12v

3 – FAN tachometer

4 – FAN on/off/pwm

The fan on/off/pwm signal is zero for off; open circuit (fan has a weak fan pull-up) or 5v for full on; or pwm 0-5v. To assure the FAN does not run when the processor is off, or not controlling the i/o pin, a 74LVC1G14 inverter (P$1) with its input pulled up with the 10K R107 resistor holds the FAN off when the opto-isolator (OPT100) is not active. The R107 pull-up to 5V/2, system ground 5 volt supply, is also needed for the open drain OPT100.

To control the FAN the processor pin PA5 drives a NFET (FET102). Pull down resistor R127 assures a floating PA5 does not energize the FAN. The opto input current is set by the 1.8K R105 resistor and 5V/1, 5 volt processor ground side supply.

**C. Power supply chain**

**DC-DC 12 to 15v converter**

The +12v from the CAN bus cable is isolated and stepped up to 15v from the +12v protected line. There are two converter options. PYBJ6-D12-S15 (IC1A) and AMG1215SNZ (IC1B). These produce a regulated 15v output with an input voltage in the 9-18v range. They are both rated at 6W. The PYJ6 is the preferred part and will sustain the 15v to a current output of about 1.4x the rating, which at 15v is about 560 ma. The output voltage regulation holds up to the overload cutoff limit then drops very rapidly, i.e. a sharp knee.

The 15v supplies the power to the processor and bms ground domain. The battery module trickle charger is the main consumption of the power. Stepping up the 12v input to 15v helps the efficiency of the charger switching to boost to the module voltage, which with 16 cells is a maximum voltage, ~56 (LiFe) or ~67v (LiPo).

**5 volt processor (5V/1)**

AP7380Y (REG100), with C111, 4.7u, and C123, 4.7u, supplies 5v for the processor side. It drives the following--

74HC00 (IC1) FET gate drive logic (to drive dump and heater FETs)

I2C2 bus (spare I2C, e.g. 5v LCD displays)

**Vcc (3.3v)**

Vcc (REG1A or REG1B) supplies 3.3v--

Processor

I2C1 bus

pull-ups (R14) (R11)

BQ76952

Sub-board: external FET discharge

CAN driver processor side

FAN tach opto-isolator pull-up (R17)

NRST (hard reset) pull-up (R8) for pushbutton and opto-isolator

LED2 and LED3 (R15) (R16) 3.3K current limits, JP13 external LED provision

Vdd (analog voltage) is connected to Vcc via a ferrite bead and by-passed with C105 (0.1u) to reduce Vcc digital noise.

Two Vcc regulator options are provided. If the processor is run at a low sysclk rate, the linear regulator, AP7380Y, (REG1), is the most efficient approach for regulation. For larger currents, a TO-220 footprint is provided that will handle a VOX7803-500 switcher, or linear LD1117-V33. Input/output caps: C119 4.7u, C120 100n and C124 4.7u. The values might vary depending on the regulator chosen.

The input to the Vcc regulator is via a diode OR which allows powering the processor from three sources. One source is the 15v described above, via diode D1.

Another input, via D2, is from the BQ REG2 output. The BQ76952 has provision for two regulators, fed from an external NPN transistor follower which drops from the plus of the battery module to supply the internal regulators. The BQ registers allow selecting the internal regulator voltages--1.8, 3.0, 3.3, 5.0v. Using the 5.0v for the diode OR avoids OR’ing the output of the Vcc regulator. The program controls the configuration of BQ REG2 and whether the BQ REG2 is on/off.

The third input to the OR, via D3, is from a P-FET, N-FET combination to switch directly to cell #3 of the battery module. Cell #3 provides a voltage that is less than the 15v dc-dc converter and greater than 5v, so if the P/N switch is on and the CAN bus 12v is present, the drain on the battery is limited to FET leakage.

FET1, and FET104 form the P/N switch. N-FET, FET1, pulls down the gate of the P-FET to turn it on. An external switch via JP1 can also turn on the P-FET. Processor pin, PC13, can turn on the N-FET. Resistors R4, and R125 assure the FETs are off when the external power is off.

A number of powering scenarios can be implemented with this arrangement. Being able to discharge the battery module to a voltage for long-term storage might require operating the bms without power from the CAN bus. In this case the processor must be powered from the battery module.

The RTC can wake up the processor from a complete shutdown by using the RTC and PC13 to turn on the P/N switch. PC13 is in the RTC domain and powered by VBAT even when the main power, VCC, is off. The LSE (low speed external osc, i.e. xtal) can run and a time setting signal an “alarm” in the RTC. The alarm routes to PC13 to turn on the P/N switch at which point the processor executes a power-on-reset and restarts.

**VBAT**

The processor VBAT supplies the RTC (Real Time Clock) domain in the processors. When Vcc is off, VBAT will maintain the RTC and associated sram registers. The RTC domain provides a means for saving some data when the processor is in shutdown mode with VBAT present.

It requires a minimum of 1.7v and draws less than 1 ua with the 32 Khz clock running. There are two alternatives for powering VBAT. One is with the BQ76952 regulator REG1. This can be set to 1.8v. A zero ohm resistor, R12, connects REG1 to the VBAT processor pin1 and C118.

An alternative is to install the MCP1810 linear regulator (REG101). This is a low quiescent current regulator powered from battery cell #1. The current drain, though continuous on the cell, is less than 1 ua so the unbalancing that cell from the others is negligible. R123 and C118 give some protection for hot-plugging the battery module to the board. R123 and the MCP1810 would not be installed if the BQ (REG1) is used for VBAT.

Note: The processor internally connects VBAT to Vcc when Vcc exceeds the VBAT pin voltage.

**D. Charger**  
  
A low current charger boosts the 15v dc-dc isolated converter to the voltage of the battery module by switching an inductor with a FET. The FET turns on and the inductor current increases. The FET turns off and the inductor “flyback” dumps the energy into the battery pack. The strategy is to set a pwm rate and on/off ratio such that the current drops to zero during FET off time, and the current build-up during the on time results in delivering the power available from the dc-dc converter; usually called a discontinuous conduction mode (DCM). Using this mode, the average output current can be set without feedback, i.e., open-loop.

If the parameters are such that the current does not drop back to zero during the FET off time the current level increases each cycle and unless there is some mechanism for limiting the peak current eventually the something fails. If the build up is slow enough the dc-dc converter will eventually shutdown in overload mode. If the build-up is fast the output capacitance of the dc-dc converter may be sufficient to destroy the FET before the overload limit begins lowering the voltage.

Drive to the charger is from processor PA8, timer TIM1CH1. This drives the MCP1416 (or MCP1401) FET gate driver (IC102). The gate drive is supplied with 15v from the dc-dc converter. In addition to the output capacitance on the dc-dc converter module, pads are provided for C113, C114, C115, (4.7u, 0.1u, 10n). R118 is a small series resistor between the driver and FET gate, shown as 6.8 ohms on the schematic. It is expected that values of around 15 ohms might be optimum, but the FET and other factors will be involved. A test point, TP1, provides convenient access to monitoring the FET gate signal.

The size and type of inductor for the charger (L1) will be selected after some experimenting. The Coilcraft RFB1010 series, 47 uH, is expected to be a reasonable mid-point for the inductances. The pcb footprint is arranged with alternate hole spacings for various size thru-hole inductors and rectangular areas without solder mask for various smd mounting inductors.

The PMV280ENEA switching fet (FET3) was chosen for its small output capacitance. The 1.1a current rating is sufficient to handle the peak currents. The SI2324A has a larger output capacitance and somewhat higher current rating. The output capacitance factors into ringing when the FET turns off, and the period of the ringing can affect the current at the beginning of the next fet on duration.

The switch fet drain and inductor connect to diode (U$3) that reverse biases during the FET on duration and directs the energy to the battery when the FET turns off.

LTSpice simulation files may be found in repository LTSpice directory.

Several features are present to deal with the open circuit situation. If the voltage of the inductor/FET-drain is not limited in some manner, when the FET turns off there is nothing to limit the voltage and the FET will have to absorb the energy in the avalanche mode. To prevent FET damage a capacitor plus zener is used to limit the voltage, and several schemes using the ‘L431 comparators with DAC, and/or ADC are used to shutdown the FET switching quickly.

In the open circuit situation, capacitor C5 (thru-hole) or C112 (smd), [1u@100v](mailto:1u@100v), will start at 15v, and with each pwm cycle of the FET increase the voltage. When the voltage reaches the zener voltage the zener will limit further increases. There is a thru-hole and smd alternative for the zeners (D4 and D6). 82V is the expected value.

Since the charger can generate close to 5.5W of power and the zeners are rated at 0.5W or less, a means of detecting the over-voltage and turning off the pwm is needed. Several methods are possible.

A simplified circuit sketch, config\_02202100.PDF, in the repo directory docs/description, shows the pins and internal switches for the various configurations that use the internal op-amp and two comparators in the ‘L431. Reference to this sketch may be helpful in following the following.

One method of shutting down the pwm is to measure the voltage at the capacitor/zener junction. R115 and R119 form a voltage divider for input to the processor. Several variations are possible. One is to use a high value resistors that draw very little current from the output, e.g. 4M|210K. That divider impedance is too large for the processor ADC; 50K is about the amount where variable leakages begin to affect the ADC readings. Provision to deal with this is the inclusion of an op-amp follower, a TLV521 (IC101). The op-amp output feeds PA7 and PB2. PB2 can be configured for comparator 1 input (COMP1\_INP). PA7 [‘L431-ADC1\_IN12] for the ADC measurement. DAC1 can be configured to connect to the comparator minus (COMP1\_INM). The comparator output can be configured to internally activate the break-input (BKIN2) to timer TIM1 and immediately turn off the timer output pin driving the FET. If the comparator is not used, or not available in the case of using the ‘F405 or ‘F446 processors, the program must rely upon the ADC measurement and turn off the FET. This of course is not immediate and until the software detects the over-voltage and turns off the FET, the zener must dissipate the power. The comparator scheme is hardware and not software dependent, and in fact, it might be possible to eliminate the zener.

Another variation is a second output diode, PMEG10020 (D109). This isolates the battery module from the voltage divider. With the voltage divider isolated, the divider is no longer a continuous drain on the battery module. Smaller resistors can be used for the R115|R119 voltage divider and the op-amp follower eliminated, e.g. 64K|3.3K. However, the voltage measured by the divider is higher than the battery module voltage due to the diode drop. But, the bms BQ can measure the total battery module voltage, but the measurement take much longer (but is 16b adc rather than 12b).

For FET current monitoring a 0.1 ohm resistor, R6, is placed in the FET (FET3) source. Test point, TP1, provides a place for a ‘scope. The voltage across the 0.1 ohm sense resistor is connected to PB4 and a zero ohm bridge to PA0. In the L431 this PB4 can be configured for comparator 2 input (COMP2\_INP); DAC2 can be configured for internal connection to COMP2\_INM. The output of the comparator can be configured as a break signal to timer TIM1 and turn the FET drive off whenever the current sense voltage exceeds the DAC setting. This scheme is a hardware means for preventing the FET current from exceeding its rating.

A possible enhancement is to install the zero ohm bridge R23 which connects the sense 0.1 ohm resistor R6 to PA0, and configure the ‘L431 op-amp (OPAMP\_INP). The op-amp can be configured for gain (requiring PA1, OPAMP\_INM, be connected to ground). PA3 is the op-amp output, and comparator 2 input (COMP2\_INP) can be configured to connect to PA3. The comparator minus, and output are then configured as in the foregoing with DAC2 and timer 1 break. This arrangement allows limiting the current, but with gain the sensing of the sense resistor voltage.

The output of the 0.1 ohm sense resistor R6 is passed through a RC filter for average current monitoring: R7-C6, 1.5K-0.1u. PC1 connects to this filter output and ADC measurement [‘L431-ADC1-IN5]. For the ‘L431, PA0 can be connect to the RC output via zero ohm R9. PA0 can be configured for OPAMP use as previously described, however the output can be configured to internally connect to ADC-IN8. For the ‘F405 or ‘F446 one has to be content with PC1 ADC and/or PA0 configured for ADC input. With the ‘L431 and this configuration the smoothed FET current waveform can be measured with op-amp gain.

Another feature that might be of use is the facility in the ‘L431 for blanking a comparator with a timer to avoid an unintended comparator output for a short spike such as when a FET turns on. Comparator 2, COMP2, can be linked with TIM15CH1 so that TIM15CH1 can blank the comparator. Similarly, comparator 1, COMP1, can be linked with TIM1CH5 so that TIM1CH5 can blank the comparator.

For software control of the charging there are a number of strategies that can be employed to make use of the above measurement techniques. Using the L431 processor and comparators gives the most flexibility, as well as providing protection of the fet during software development.

Header JP3, R120 (1 ohm) provides a test point for measuring output current.

Test points--

TP1 – FET102 gate

TP2 – PA0 OPAMP\_INP

TP3 – PA2 COMP2\_OUT

TP3A – FET CURRENT SENSE RESISTOR

TP4 – PA3 OPAMP OUTPUT

TP5 – PA6 TIM1\_BKIN\_COMP2

TP6 – PA11 TIM1\_BKIN2\_COMP1

**NOTE: The above test points are at battery module ground, not system ground.**

**E. BMS**

**Battery cabling**

The battery module is connected to the bms board with a 20 wire ribbon cable. On the bms board end of the ribbon an IDC 2x10 plug mates with the 2x10 (keyed) header (JP9). 1X10 headers JP8, and JP10, mount on the underside and provide a means of extending the ribbon cable connections to a sub-board that would use fets for cell balancing discharging at rates higher than supported by the BQ76952 using its internal fets.

The ribbon cable wire assignments have the cable split into a group that goes to the top of the battery module, and another group that goes to the bottom. The ends of the ribbon connect to cells on the module, and peel off in sequence as the cable goes down the battery module. Pictures of the battery module (18 positions, 16 cells installed) can be found in the repo directory docs/pictures.

The pcb layout is based on the following pin assignments--

col 1: 2x10 header pin number

col 2: 20 pin ribbon color

col 3: module cell number

col 4: additional description

---------TOP SPLIT-------------

1 BLK - PGND/SRN (BATTERY MODULE MINUS)

2 WHT - SRP (CURRENT SENSE POS)

3 GRY - VSS (CURRENT SENSE NEG)P

4 PUR - C0 (CELL #1 MINUS)

5 BLU - C2 (CELL #2 PLUS)

6 GRN - C4

7 YEL - C6

8 ORG - C8

9 RED - C10

10 BRN - C12

11 BLK - C14

12 WHT - C16 (CELL #16 PLUS) (BATTERY MODULE PLUS)

----------BOTTOM SPLIT ---------

13 GRY - C1 (CELL #1 PLUS)

14 PUR - C3

15 BLU - C5

16 GRN - C7

17 YEL - C9

18 ORG - C11

19 RED - C13

20 BRN - C15

The individual cell connections go through a 20 ohm series resistor (schematic labels RC101-RC116) to the BQ76952 input pin, and each pin has a 0.1u by-pass capacitor (CR101-CR116). The discharge resistance is a combination of the series resistor, in conjunction with the internal fet resistance (15 ohm typical). (Note: when adjacent cells are being discharge they share a common series resistor with the result that the discharge current for the cells may not be the same.)

Ribbon cable wires are present for current sensing (SRP, SRN). R116, R122, and CF116, CF111 are input filtering.

**I2C communication**

The processor I2C1, PB6 (SCL) and PB7 (SDA), connects to the BQ76952 and two 4 pin headers, JP10, JP11. JP10 is mounted on the bottom of the pcb for mating with a sub-board if external FET cell balancing discharging is used. JP11 mounts on the top for possible connection to external 3.3v I2C devices.

Header pin assignment--

1 – ground

2 – +3.3v (VCC)

3 – PB7 – I2C1 SDA w 3.3K (R11) pull-up to Vcc

4 – PB6 – I2C1 SCL w 3.3K (R14) pull-up to Vcc

The BQ76952, unless preprogrammed, boots up in I2C “fast” (400KHz) mode.

The regulator for VCC can receive power from three sources. VCC is required for processor communication with the BQ76952. However without communication the BQ can still perform operations.

**Control**

**ALERT** connects to PB3. The error detection in the BQ76952 can to cause an interrupt in the processor via the ALERT pin. Enabling the internal pull-up on the processor is necessary. An external pull-up on the pcb is not provided. The ALERT pin is active low, i.e. normally high and pulls low when the BQ detects a fault.

**RST\_SHUT** connects to PB5. PB5 configured for push-pull output. Asserting RST\_SHUT for greater than one second will cause the bms to enter SHUTDOWN mode. For less than one second it causes exiting SLEEP and DEEPSLEEP modes.

**TS2** is not connected and floats. When the BQ enters into shutdown mode TS2 is connected to a high impedance (~4.5M) to approximately 5v. If TS2 is pulled low BQ exits shutdown mode. If TS2 is low before the BQ command to enter shutdown mode, e.g. TS2 connected to a thermistor, then BQ enters a “soft shutdown” condition, but cannot enter a full shutdown. Hence, TS2 is left float and not used.

**LD** is connected to PD2. Control of LD might have some use in controlling the entry and exit from shutdown, and is more of a jic provision.

**Regulators**

REG18 is by-passed to ground with C110, 2.2u, per the datasheet.

NPN transistor, Q1, drops the battery module voltage, (PACK), via resistor RT1, into the input REGIN. BREG drives the base of the NPN. C9, 1u, and RT1, add filtering. C8, 22n by-passes the emitter (per datasheet). The power dissipation requires consideration as the total REG1 and REG2 the transistor plus resistor must dissipate the battery voltage minus about 5v at the total current. Hence, RT1 is a thru-laid out as hole vertically mounted resistor which can handle ½ w.

REG1 can be used to power VBAT using the 1.8v or 3.0v voltage selection.

REG2 can be used to power the 3.3v Vcc by using the 5v, which diode ORs (D2) with other inputs to the 3.3v linear regulator (REG1A or REG1B). Enabling REG2 is necessary for turning on the Dump and Heater fets.

**Thermistors**

BQ pins TS1, TS3, and DCHG connect to 2 pin headers JP2, JP4, JP5. 10nF capacitors across the thermistors help noise (per datasheet). The bms register initialization will accommodate either 10K or 100K thermistors with internal pull-ups.

TS1, TS3, and DCHG can also be configured as ADC inputs.

DSG and CHG connect to 2 pin headers for two additional jic thermistor (or ADC) inputs.

**F. Misc**

**Dump**

For discharging the entire battery module FET (FET100) can switch in a 10W resistor mounted on the board, or a resistor connected to the two pin header JP17. Thru-hole pads are positioned on the board so that a 10W resistor can be mounted on the bottom side of the board. The resistor is not shown on the schematic. For an off board resistor, the header pin connected to the fet drain is expected to be connected to the resistor, and the other end of the resistor to battery module plus. The header pin for the fet source would be connected to the battery module minus. The minus connection avoid the resistor current passing through the board traces and battery module ribbon cable. R101 holds the fet off. R102 makes the fet act as a source-follower if the external minus connection is missing.

To prevent inadvertently turning on the dump fet the processor must set one I/o pin high (PC10) and another pin (PC8) low. IC1 gates invert and AND, as well as increase the voltage from the 3.3v processor to 5v, for driving the dump FET. R18, 470K, assures the gate input does not drift high if the i/o pin is not configured for output.

Configuring the BQ REG2 for 5v (5V/3) is required for powering IC1 which supplies the gate drive for the FET100 and FET2.

Item: When the battery module is not connected the BQ chip will only be powered if the charger is active, i.e. the 1u@100v capacitor C112 with zener or software over-voltage control powers the BQ.

**Heater**

At times it may be necessary to warm the battery module before the first launch. A FET, FET2, for switching on a high wattage resistance is provided. A TO-220 footprint for FET2 provides for a high current fet. The same logic as above for “Dump” is used. In this case it is PC12 high and PC11 low that enables the FET. Two spade terminals are provide beside the FET for the external connections to the heater. The same as for “Dump,” R126 limits current should the external battery minus be missing. R124 assures FET off when the processor is not powered. R104 assures the FET would not turn on if PC12 is floating.

**Dump2**

This provision might be used for some external load, e.g. a relay. Board space allowed adding this jic. FET101 is driven by PC6. Two pin header JP16 connects to the fet drain and source. R103 and R100 provide the protection in the manner described above.

The FET101 gate is driven directly from the processor i/o pin and does not depend on the 5v source as does Dump and Heater.

**Spare thermistors**

Header JP12 can be used to connect to thermistors. PC4 and PC5 can be configured for ADC.   
R10 and R13 are pull-ups to Vcc.

**HSE**

Provision is made for the High Speed External oscillator, i.e. xtal control. Xtal, Q100, loading capacitors, C107, C109 (15p), startup resistor R112, 1M. Processor pins PD0, PD1.

**LSE: 32 Khz oscillator**

A crystal (X101) provides for 32 Khz LSE (Low Speed External) oscillator implementation. C100, C101 (22p) are the xtal loading capacitors. The LSE uses processor pins PC14, PC15.

In the processor shutdown mode the RTC internal 32 Khz osc (LSI) is shut down as it is not part of the RTC domain. However with the xtal it will run in the LSE mode. In the other current low power modes the RTC LSI osc runs.

**Spark gap**

Since the battery module ground is isolated and floating with respect to the system ground, provision for limiting a voltage built up that might breakdown one of the isolation barriers (dc-dc converter transformer, opto-isolators, or CAN driver). A pcb spark gap is made with pad PD1. R3 can be a resistor for limiting sparkover current or fusing in more catastrophic situations.

Thru-hole pads are located near the pcb spark gap for mounting a gas discharge type spark gap.

**I2C2 bus**

Header JP21 provides a I2C bus with 5v. This purpose of this bus is for a possible LCD display which would require 5v. The I2C1 bus described above is for newer 3.3v parts.

This is the only load on net 5V/1, AP7380Y, linear regulator, (REG100), the regulator and capacitors C111, C123 can be omitted of this I2C bus is not implemented.

Header JP21 pin assignment--

1 – ground

2 – +5.0v (5V/1)

3 – PB14 – I2C1 SDA w 3.3K (R11) pull-up to 5V/1

4 – PB13 – I2C1 SCL w 3.3K (R14) pull-up to 5V/1

**LEDs**

LED1 (R2) 6.8K – CAN bus cable +12v protected

LED2 (R15) 3.3K – GRN – PB0 also pin2 JP13

LED3 (R16) 3.3K – RED – PB1 also pin 3 JP13

Provision for LED2 and 3 on-board and three pin JP13 header for (low current) external LEDs.

JP13 pin1 – 3.3v (VCC). PB0 and PB1 pull down, i.e. set to 0 turns the LED on; 1 is off.