**Overview**

Note: an early version is out on github i(GliderWinchItems) n the BMS repo with directories for bmsbms and bmschgr. These were abandoned and a major revision with the suffix ‘R’ suffix added. (The revision having to do with the main parts on the top rather bottom sides of the boards). The following refers to the files in the bmsbmsR and bmschgrR directories.

Two boards communicate via 1x30 headers on the top (top as seen in the eagle layout) and bottom edges of the card. The top board is the “charger” board, and the bottom board the “bms” board. The headers on the top board 1x30 are on the board underside and the bottom board 1x30 header are on the topside.

Headers on the topside of the top board are for features requiring easy access, such as SWD for flashing programs, FTDI for monitoring/debugging, and battery cable.

Headers on the bottom side of the bottom board are for connectors that are not expected to be accessed after assembly, e.g. I2C header for LCD.

The top board has the following main features--

- Isolated dc-dc converter (CAN cable 12v to 15v bms power, 6w)

- Isolated CAN driver (with two LM78L05 to power both sides)

- Isolated FAN pwm drive

- Isolated FAN tach sensor

- Isolated Master reset

- Battery charging boost circuit

- BMS discharge resistors

- BMS external discharge FETs

- Header isolated (topside of board)

. Board-to-CAN cable (2x5) (U$6)

- Headers NOT isolated (topside of board)

. Battery cable, (U$5) (2x10) IDC connector male

. SWD (STLink single wire debugger)

. FTDI (JP4) (usart1 for PC monitoring/debugging)

. Two fet driven LEDs (red & green) (JP8)

. 12V fan (JP9)

. Three thermistors (JP10)

. Hall-effect current sensor (JP7)

. Charger current test-point resistor (JP11)

The bottom board has the following main features--

- STM32F405/446R processor

- LTC6813-1 bms

- 15v to 7v dc-dc switcher (provision for three types) [powers: LTC6813 regulator and 7v switcher]

- 7v to 3.3v dc-dc switcher (provision for two types) [powers: STM32F405/446R processor]

- LM78L05 for +5 needs.

- BMS RC filter for each cell

- PFET/NFET switch to power 15v switcher from battery cell tap (PA0 pushbutton control)

- Headers (bottom side)

. Pushbutton (JP11) (PA0 wakeup pin, pullup)

. Battery dump (JP12) (onboard FET, or external FET, RC, and current sense)

. I2C1 bus: (JP3), LCD or non-fet drive bi-color LED

. Pushbuttons (JP10) two pushbuttons, or ADC inputs.

. On-board LED. Driven from same I/o pin as two color leds on bmschgr board.

**LTC6813-1**

The LTC6813 “C” inputs have a RC in series to the 1x30 pin header. The “S” pins pass directly to the bmschgr board. The datasheet recommends a time constant using 100 ohm and 100n capacitor RC, but mentions 10 ohms when using internal fet discharging; hence 100 ohms and 0.1u is used if the external fet discharging is not implemented.

The discharge resistors are on the bmschgr board. The resistors are mounted up-right, on the underside of the board (for air circulation). The layout uses a three pin resistor footprint which allows the resistor to be connected for either external fet discharge control, or internal fet control. When the internal fet switches the discharge resistor the resistor is inserted to connect C(n) to S(n). For external fet control the resistor is inserted to connect C(n) to FET(n+1) drain.

For external fet discharge control the fet gate resistors are present as shown in the datasheet, but their presence appear to provide no benefit.

The processor communicates with the LTC6813 with SPI1

PA4 SPI1-NSS <-> CSB

PA5 SPI1-SCK <-> SCK

PA6 SPI1-MISO <-> SDO (4.7K pullup to VCC)

PA7 SPI1-MOSI <-> SDI

LTC6813 power is via a NPN transistor driven from the LTC6813 internals.

Base LTC6813 DRIVE

Collector 7v switcher via 100 ohm|0.1u filter. (datasheet recommendation)

Emitter VREG

The pcb has a large via in the center of the LTC6813 for hand-soldering the heat sink pad. The part mounts on the top side of the board. A copper foil additional heat-sinking could be soldered to the bottom side and the area to the right of the LTC6813 on the bottom side is free of parts.

**Ground plane**

On the top board the topside and bottom sides are mostly copper-pour with ground. The ground planes are split to isolate the digital and analog currents. The 1x30 top header has two ground pins (#30 & #19) which carry the ground splits between the boards. On each board the digital ground connects to the analog ground at one small area near the center. Hopefully(!) this will help the noise in the analog readings.

**STM32F405R, STM32F446R compatibility**

Either f405R or f446 processors can be used, however there are a few hardware configuration differences with the power pin grounding and by-passing. The following three pins differ between the two processors. The rest of the pins are identical.

Pin 30 capacitor CP2

f405 = PB11

f446 = VCAP\_1 = 2.2u by-pass cap

Pin 31 capacitor CP3

f405 = VCAP\_1 = 2.2u by-pass cap

f446 = VSS = zero ohm

Pin 47 capacitor CP1

f405 = VCAP\_2 = 2.2 u by-pass cap

f446 = VSS = zero ohm

Thinking of possible uses of the board PB11 is not available on the f446. Therefore if I2C2 were to used in the future, the I2C2-SDA for the header would have to come from the alternate on PC12. However, PC12 is also used for the SD card interface, so SD card and I2C2 could not be used together. Either both are unlikely.

Note—the implemented I2C bus header on the bmsbms board is I2C1, not I2C2.

**I2C bus - Header JP3**

This header is on the bottom side of the bottom board--

Pin1- gnd

Pin2 - +5

Pin3 – PB8 I2C1-SDA with 3.3K pullup

Pin4 – PB9 I2C1-SCL with 3.3K pullup

**Power supply chain**

On the bmschgr board, protection for polarity reversal of the system 12v power is provided by a P-FET, U$1. A 1 ohm (or less) resistor is in series for testing input current.

On the bmschgr board, the 12v power from the CAN cable drives the FAN and dc-dc isolated converter. On the isolated battery side, a 6 watt dc-dc converter output drives the bmsbms board and dc-dc boost switcher to charge the battery.

On the bmsbms board the first switcher in the chain converts the input to 7v for the LTC6813 regulator transistor and switcher for generating 3.3v for the processor, as well as a 5v LM78L05 regulator.

The first switcher receives its power via a diode “OR” to the bmschgr board with the isolated dc-dc switcher, or a P-FET/N-FET pair that can turn on a three or four cell tap on the battery. The tap selection is made with a hard-wired jumper to thr-hole solder pads on the bmsbms board (top edge, right of center). The N-FET is turned on by a pushbutton which pulls up PA0 (which can also be a RTC wake-up pin). There are several possibilities for use of this arrangement.

One possibility is using the battery to maintain the processor during a calibration sequence for the dc-dc boost battery charger. The sequence increases the pwm, and hence charging current until the overload on the isolated dc-dc converter trips. At this point the dc-dc isolated converter voltage drops to zero. The battery maintains the processor which then uses the last pwm value for computing a safe pwm max.

Another possibility is to run the processor and LTC6813 for discharging the batteries to a storage level when external power is not available. The discharge requires a long duration and external power in the form a 12v automotive battery is marginal. When the discharge level is reached the NFET is switched off, and if CAN cable power is not present the processor shuts down.

Bringing up the processor if it is in a shutdown condition (which also means no external power is present) can be implemented with the pushbutton. The pushbutton is a pull-up, and the pin in the powered down state is open drain. The pullup turns on the N\_FET and the P-FET connects the battery to the first switcher and it all comes up. The processor must then set PA0 to output and high to maintain the power before the pushbutton is released.

When the processor is brought up via the CAN cable power being applied it will sense PA0 (pushbutton input) and see that it is not high. When the program startup sees PA0 high the sw can assume a discharge is might be requested and to preclude an accidental triggering of the discharge several subsequent pushes could be require before going into the discharge sequence. LED flashing & colors would give the hapless Op clues as to what is going on.

**BMSBMS switcher options**

Three types of dc-dc switchers can be used. One type is the inexpensive modules based on the LM2596. Removing the voltage setting pot is essential as these become intermittent in a matter of days. The pot is replaced with a fixed resistor to achieve the desired output, in this case 7v. The main disadvantage of this module is the size and board space required.

Vo ~= 1.23 \* R1/(R1+10K)

A second option that uses much less board space is the very inexpensive modules based on the MP2307. Some measurements show that these are slightly less efficient than the LM2596 modules at the power levels being used here.

<https://www.ebay.com/itm/114195655451?ul_noapp=true>

These also require the very tiny pot to be removed and replaced with a fixed resistor

Vo ~= 0.925 \* R1/(R1+100K)

A third option requiring even less space, but somewhat more expensive, is the LM78xx replacement switchers, e.g. a 3.3v output version--

<https://www.digikey.com/product-detail/en/VXO7803-500/102-4248-ND/7350287>

All three of these can be fitted on the bmsbms board.

**LM78L05 supply**

These are cheap--$0.25--and have tolerate a wide range of input voltages. They are used for supplying both sides of the CAN driver on the bmschgr board, and 5v analog sensors on the bmsbms board. The 5v (VREG) for the LTC6813 is via the NPN transistor, driven from the LTC6813 input feedback.

**VBAT**

The VBAT pin is powered via diode from VCC. When VCC is not present, i.e. the processor is not powered, there is provision for a low quiescent linear regulator (AP7380) that will power VBAT from the first battery cell.

If the P-FET/N-FET scheme described above is used, then there is less reason to implement the battery maintained VBAT.

**Power supply voltage sensing and ADC inputs**

The isolated dc-dc converter output and battery voltage dividers are on the bmschgr board. The other dividers are on the bmsbms board.

PC0 ADC123-IN10 - Isolated dc-dc switcher output

PC1 ADC123-IN11– Battery voltage

PC2 ADC123-IN12 - 5v bmsbms LM78L05

PC3 ADC123-IN13 – 15v diode-ORed

PC5 ADC123-IN14– 15→7v switcher

PA3 ADC123-IN3 - Dump current sense

**CAN cable header**

A 2x5 male header (keyed) receives an IDC 10 pin ribbon cable connector. The IDC connector plugs into the bmschgr board and the ribbon routes through one DE-9 connector and on to a second DE-9 connector close-by. The two closely spaced DC-9 connectors allow daisy-chain of the CAN cable. Locating them close together minimizes the amount of ribbon cable (small wire) in the chain. The 12v and ground in the CAN cable three pins, each, paralleled, i.e. six of the nine pins on the DE-9 connector. The CAN H and CAN L signal lines take two pins. The remaining pin in the DE-9 connector is for the master reset line. The tenth wire in the ribbon is not used.

The master reset line is pulled to (system) ground to activate the master reset. Each battery module has a H11L1 opto-isolator with a 3.3K resistor to the 12v CAN cable power. The output of the opto-isolator battery pulls down the NRST (not-reset) line on the processor from 5v to battery module ground, thus causing a hard-reset.

Provision for a smd pushbutton on the bottom side of the bmsbms board allows for manual resets during test & debugging.

**Battery charger**

The bmschgr board holds a fet driver, fet, inductor, high voltage diode, zener, and capacitor for generating a current for charging the battery module. Approximately 5 watts is available from the 6 watt dc-dc isolation converter for charging, leaving about 1 watt for running the processor, LTC6813, and other 5v loads.

The MPC1416 fet driver is driven by a pwm signal from the bmsbms board (PC7-TIM8CH2). The voltage boost is done in discontinuous mode. The inductor current “discharging” into the battery reaches zero, before being “charged” by turning the fet back on. As the pwm increases the average current increases. At some point either the dc-dc isolation converter load becomes too large, at which point the overload protection in it does a fold-back and the voltage collapses to zero. Header (1x2) JP11 across a small resistor (e.g. 1ohm, R31) allows calibration & test.

The 82v zener and 1u capacitor in the output to the battery serves to limit the voltage across the fet should the charger be active and the battery connection is open.

The voltage of the charger output (pin 13 on the bottom 1x30 header) is monitored via R27 & R28 resistor divider, on pin 12 of the bottom 1x30 header, into PC1-ADC-IN11. Measuring the charger output voltage with the processor 12b ADC is much faster than using the 16b LTC6813 measurement and allows the program to shutdown the charger for the open-circuit situation.

**LTC6813 GPIO auxiliary pins**

The nine auxiliary pins can be used for 16b ADC measurements. Five of the nine have designated uses, and the other four have thru-hole solder pads for possible uses.

G1 – Measures the 5v LM78L05 output used for Hall-effect sensor. The LTC6813 5v (VREG) has marginal drive and the Hall-effect sensor will affect the voltage, so an external 5v is used and the voltage measured so as to make the measurement ratiometric.

G2 – Thermistor #1, 10K, 2x3 header (JP10) on bmschgr , R26 10K pullup

G3 – Thermistor #2, 10K, 2x3 header (JP10) on bmschgr, R27 10K pullup

G4 – Thermistor #3, 10K, 2x3 header (JP10) on bmschgr, R28 10K pullup

G5 – Hall effect sensor, 1x3 header (JP7) on bmschgr, R22|R29 divider

G6 - Solder pad U$1, R33 to gnd, on bmsbms

G7 - Solder pad U$8, R34 to gnd, R53 to pad U$12, on bmsbms

G8 - Solder pad U$9, R35 to gnd, on bmsbms

G9 - Solder pad U$10,R36 to gnd, on bmsbms

G1-G5 are planned usage with headers on the bmschgr board.

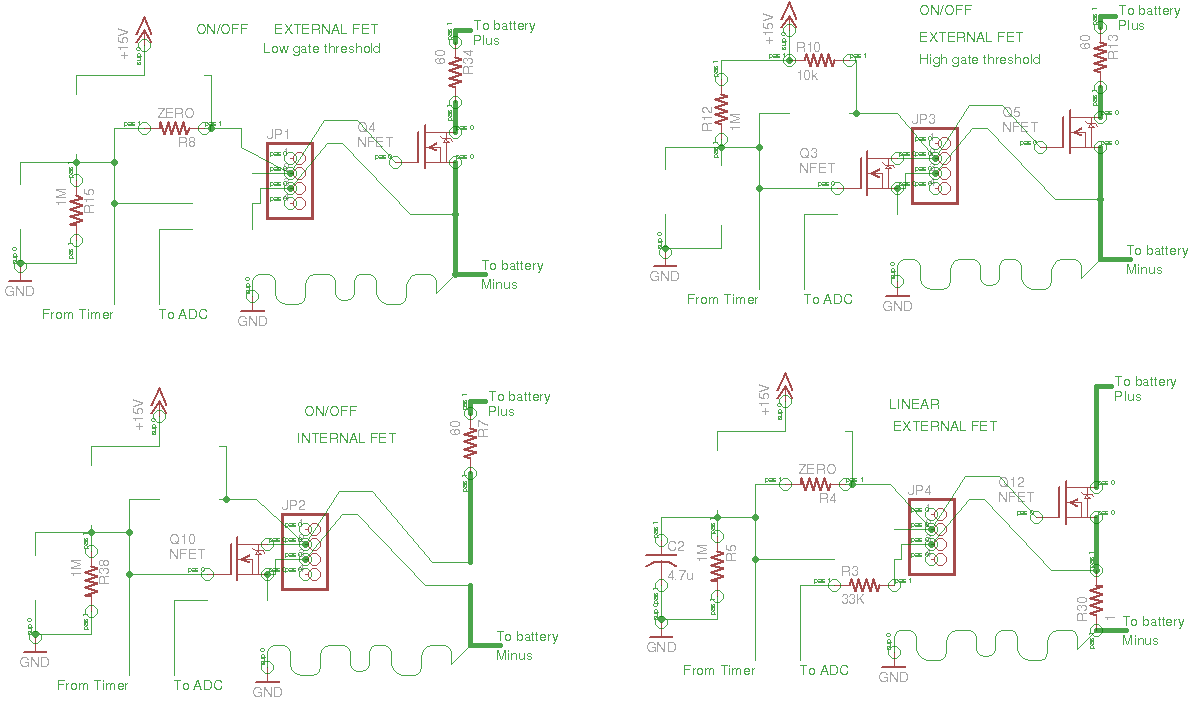
G6-G9 are spare inputs for late additions. Thru-hole solderpad provide access. The resistors R33-R36, and R53 are to-be-determined.

**Battery Dump**

Two situations where a load on the battery is needed are battery dump and battery pre-heat. The battery dump is for placing a load across the battery to discharge it to the long term storage level. Using the individual bms fets with resistors is one way to do a discharge, but the current load on each cell may vary due to resistor and fet variations. A single resistor across the whole battery module pass the same current through each cell.

The pre-heating applies a large load to the battery and uses the heat generated to raise the temperature of a very cold module.

Provision is made for several ways of implementing a load.



The above schematic depicts a number of ways the parts for the dump can be implemented. (The undulating ground line is a reminder the ground-loop path from the battery minus via the battery cable ribbon, bmschgr board, 1x30 header, bmsbms board to the header.) Various parts pn the bmsbms board are fitted or omitted to construct the different circuits. These parts are located in a space on the topside of the bmsbms board that was available, so there was no need to make a hard decision for the specific circuit to be used.

Note that the external load grounding connects directly to the battery minus and not through the pcbs and bmschgr-to-battery cable.

The bottom left circuit shows is a simple switching of an external resistor with an on-board fet. The 1M gate resistor to ground assures the fet is off until software configures and sets the i/o pin. The footprint is for a SOT-23 package and 100v 2a fets are inexpensive.

The top left circuit shows an external fet. The external fet requires a low gate threshold as the gate drive is directly from the processor i/o pin, and hence a bit less than the 3.3v VCC when it is high. This limits the range of external fets available. The fet, RFP12N10L, is a candidate.

The top right circuit provides for an external fet and uses the internal fet to increase the gate drive voltage. The 1M gate resistor on the internal fet assures that it is on during the time the board powers up and the processor program configures the i/o pin. The drain resistor to +15v pulls up the external fet gate.

PWM with the foregoing on/off circuits is limited in speed, but sufficient for low speed switching. To provide for fast switching the header includes pcb ground as well as +15. That allows an external fet driver and fet to be driven at higher rates. The choices for voltages greater than VCC (3.3v) was +5, +7, and +15. Since many fets reach minimum Rds with gate voltages of +10, the +15v was selected. Most fets allow +/-20v as the max source-gate, and most fet drivers are +18v or higher.

The lower right circuit shows the configuration for using a fet in a linear mode. A fet with heat-sink could be used for a load. A load resistor in the external fet drain could be added to off-load some of the heat generation from the fet, but TO-220 package type fets are capable of 50+ watts of dissipation. The resistor in the external fet is used to sense the current. The RC for the gate smooths a timer pwm for controlling the source-gate voltage. The program raises the pwm until the sensed current level is reached. This scheme avoids noise generated by switching relatively large currents.

**LEDs**

On-board leds are mainly for test & debugging.

External leds we expected to be bi-color (e.g. red & green) and panel mounted to show status.

**On-board leds: bmschgr--**

- Power on: driven by 12v on the polarity protected side.

- Program controlled: i/o pin driver from pin #6 bottom 1x30 (PC11), drive to FET Q3 gate

**External leds: bmschgr**

- program: header JP8-1 (PC10), FET Q2 drain in series with 470 ohm pulls down 5V(B)

- program: header JP8-2 (PC11), FET Q3 drain in series with 470 ohm pulls down 5V(B)

Note PC11 drives the FET for header JP8-2, as well as on-board LED.

**On-board leds: bmsbms--**

- program: PC13 pulldown 330 ohm to VCC

**External leds: bmsbms--**

- PC10, PC11 to bmschgr board JP8-1,2

- JP3-3 PB8 (alternative to I2C bus usage)

- JP3-4, PB9 (alternative to I2C bus usage)

LEDs on the I2C bus header is an alternative to using the I2C bus for the LCD. Note that one of those cheap bus extender modules based on the PCF8574T could be used to drive multiple LEDs as well as read pushbuttons, and coexist on the I2C bus along with LCD displays. The cheap modules support jumpers for setting 8 addresses.

**SWD (Single Wire Debugger)**

Header JP5 on bmschgr provides easy access to the SWD on bmsbms via the 1x30 header JP1--

JP5 JP1

1 GND

2 #28 PA14 JTCK

3 #29 PA13 JTMS

4 NC

The JP5 pin sequence is the same as for the “Blue Pill” STM32F103 module. Pin #4 is designated as 3.3v power, so in this case it is no-connection.

**JIC: Alternate MCP1416 w header**

Just-in case: bmschgr, JP13, A 1x4 header with the same pin sequence as JP9 for the gnd and +12 for the 12v fan. A H11L1 opto-isolator provides the isolation and is driven by PC6 on the bms side. The H11L1 system side can be configured a number of ways by the components fitted.

- Direct output of the H11L1 (5v signal)

- Output of the H11L1 via fet Q4 with or without pullup resistor to 12v

- Output of a MCP1416 fet driver via a series resistor (generally to prevent ringing).

PC6, TIM8CH1 can be used for pwm if needed.

PC6 also supports USART6-TX, making that a possible isolated uart output. Since the H11L1 inverts the signal the fet can be used to correct the inversion.

There is no provision for a fly-back diode.

This is output-only. No provision for incoming signals.

**JIC SD card**

Just-in case: thru-hole solder pads are available for driving an external SD card. However, the two LEDs on the header of bmschgr share two pins.

