**Discontinuous Conduction Mode Current Output Boost Converter**

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This analysis was undertaken in support of the development of a simple low current/power boost converter used to provide a trickle charge for topping off and balancing a battery string on the order of 65 volts. The input voltage to this converter is on the order of 12-15 volts and the maximum charging current on the order of 75 mA. So roughly a 5 W converter. Operation in Discontinuous Conduction Mode (DCM) avoids the need for high bandwidth current sensing for feedback operation. The output current comes in short, relatively high current (around 1 A) triangular pulses but the batteries only really care about the average current in this application. The output control accuracy required for this application is not believed critical.

The following analysis assumes an idealized lossless boost converter boosting fromtooperating in Discontinuous Conduction Mode (DCM). If a synchronous rectifier was used for the output diode to eliminate its voltage drop, the primary errors would be associated with the inductor losses. (When using a diode, the analysis can be approximately modified to correct for it by simply adding the forward diode drop to the design output voltage.)  
  
The analysis covers three main topics. The first addresses covering the maximum inductance that can be employed for a given set of input and output voltages and a desired PWM frequency. (The selected PWM frequency may be refined during prototype development to be that which balances coil losses and switching loss for best efficiency.) The second portion covers the transfer function from duty cycle to output current and considers the sensitivity to input and output voltage deviations from the nominal. The third section addresses an observed oscillatory resonance that is excited as the inductor current returns and undershoots through 0. The resonance frequency and amplitude are developed along with the implications to the output current settability. If the resulting settability should be deemed insufficient, a simple scheme to mitigate this issue is proposed that seems imminently applicable for this application.

Inductor Sizing

The inductor charges up to a peak currentduring the FET on period  as given by



Similarly, the inductor discharges back to 0 current during off period governed by the equation



For DCM operation, these may be equated yielding



Let



Then



Hence,



At the boundary between DCM and CCM operation, the PWM period is given by



The boundary PWM frequency is thus given by



so the inductance for a specified PWM frequency may be found from



This is actually an upper bound on *L*. If *L* is any larger, the system would exit DCM for that PWM frequency. If an inductor were out of tolerance and too large, the PWM frequency may be reduced to accommodate this. In fact, we might consider adjusting the PWM frequency to compensate for inductor size in general. More on this following Equation .

The boundary duty cycle (and the maximum duty cycle) is given by

   
  
The output power is the output voltage times the maximum desired (average) output current. The output power is also the energy transferred per cycle times the PWM frequency. Setting these equal (lossless) yields,



Solving for ,



Output Current Adjustment and Parameter Sensitivities

Now the behavior when solidly in DCM mode, i.e., when the duty cycle is less thanis considered. Now that the inductance, PWM frequency, and boundary value for duty cyclehave been established, solving for the transfer function from duty cycle to current is relatively straightforward. Assume the values for inductance and PWM frequency are fixed. Then the inductor current at the end of a charging period of duty cycle  is



where is the actual input voltage andis the duty cycle. (Note the boundary duty cycle for DCM is actually only when  and  .) The discharge time back to zero current is then given by



This is a triangular waveform so the charge transferred to the output is easily computed as



The average output current is just this charge per cycle times the PWM frequency,



So the system is square law with duty cycle, quadratically sensitive to input voltage variations, inversely sensitive to the inductance value, and approximately inversely sensitive to the output voltage (if it is large compared to ). If the (effective) inductance is measured during calibration and the input and output voltages are measured during operation, the duty cycle for a desired output current may be solved for as



Something to note here is the product in the numerator. Calibration for inductor tolerance might involve effectively making this product a constant by adjusting the PWM frequency.

Off-State LC Resonance  
  
Very lightly damped oscillations in the inductor current after it has returned through 0 have been observed in simulations, are reasonably understood, and are expected to occur in practice. The oscillation frequency is primarily set by the inductor resonating with the drain-source capacitance of the FET. This resonance is excited by the inductor current returning to 0 and then undershooting. This undershoot is associated with the charging of the output diode’s capacitance. The resonance frequency and amplitude are developed next. Then the implications of this resonance on output current settability are developed. Finally, a simple scheme to mitigate these issues is proposed should better settability accuracy be desired.  
  
The resonance frequency is primarily determined by a parallel LC tank formed between the main inductor and the FET’s drain-source output capacitance. The resonant frequency is thus approximately given by the well-known relation



The amplitude of the current can be approximately estimated using the observed behavior of its excitation. The discharging inductor current discharges through 0 and continues while the output diode’s junction capacitance charges as it cuts off current flow to the output. The drain voltage during this period has been clamped to about -0.6 volts by the FET’s body diode. As such the inductor starts charging back towards 0 current with the applied voltage equal to  where  is this diode drop. Hence the rate of change of the current here is simply given by

   
This results in the inductor current ramping at a rate similar to the normal charging rate when the FET turns on. As this current passes through 0 and begins the first cycle of its oscillation, it was observed that the slope as it passed through 0 was continuous and established the zero-crossing slope of subsequent resonance. The slope of a sinusoidal as it passes through 0 is found by evaluating its derivative at this zero-crossing point. When this is done, the zero-crossing slope is found to be



Hence the amplitude may be approximated by setting these slopes equal and solving for A. This yields



As is discussed next, there is value in minimizing this amplitude. That suggests selecting the switching FET for low output capacitance is desirable. It also suggests using larger inductors. Inductor size is inversely related to the PWM frequency so that suggests some value to lower PWM frequencies. So in addition to trying to balance switching losses with inductor ac losses, here is something else to consider in choosing the nominal operating frequency.

Depending on their amplitude and where they are in their cycle at the start of the next PWM cycle, the inductor current does not start at 0 and hence the final peak current will generally be offset by this initial value. In the steady state, this is generally repeatable. But where in the cycle this will be when the FET turns on is not readily predictable. This results in the transfer function from duty cycle to output current to generally follow Equation but with a stairstep like progression due to the initial condition of the inductor current being walked through. (It has not been investigated but it might not necessarily even be monotonic depending on the oscillatory current’s amplitude.) The effect of the initial condition on the output can be seen by modifying Equation above slightly.



where is the erroneous initial current of approximate range from Equation above. The  term may be neglected so long as it is small in comparison which is generally the case. Multiplying this charge by the PWM frequency gives the output current



The first term is the same as for Equation as would be expected. Normalizing by this value yields



So the fractional error is seen to depend on the value of the erroneous initial condition to the average output current modified by the leading scaling factor.  is generally in the range of 0.5 to 0.7 and  for the working numbers given at the paper’s beginning is around 3.33. So roughly this scaling factor is on the order of ¼. In some simulations the observed value of was around 25 mA which is about 1/3rd the nominal value of the output current. In that case we could be looking at errors on the order of ±8%. That is significant but not intolerable in my estimation.  
  
But there is appears simple was this issue maybe substantially mitigated for this application. If the PWM period was randomly or periodically modulated over a range that spanned several resonance periods, the longer-term average of the output current would be much closer to the desired value. Balancing is a relatively slow process so this appears to be a very applicable mitigation. If this is employed, then some additional margin to the DCM-CCM boundary would be needed to avoid entry into CCM operation. Ideally, the PWM period would be changed every cycle but that is not critical given the time frame for balancing expected. It appears there are likely enough processor cycles available for a random number generator to be executed out of an interrupt routing triggered by the completion of a cylcle. Note that the FET on time (counts) does not get changed here, only the duration of the current PWM cycle. But another variation would be to keep the PWM period fixed and modulate the duty cycle. Given the square law nature of output current to duty cycle, the former scheme would probably be preferred to the later.