



## 1. Description

### 1.1. Project

Project Name	BMScableL431
Board Name	custom
Generated with:	STM32CubeMX 6.3.0
Date	08/01/2021

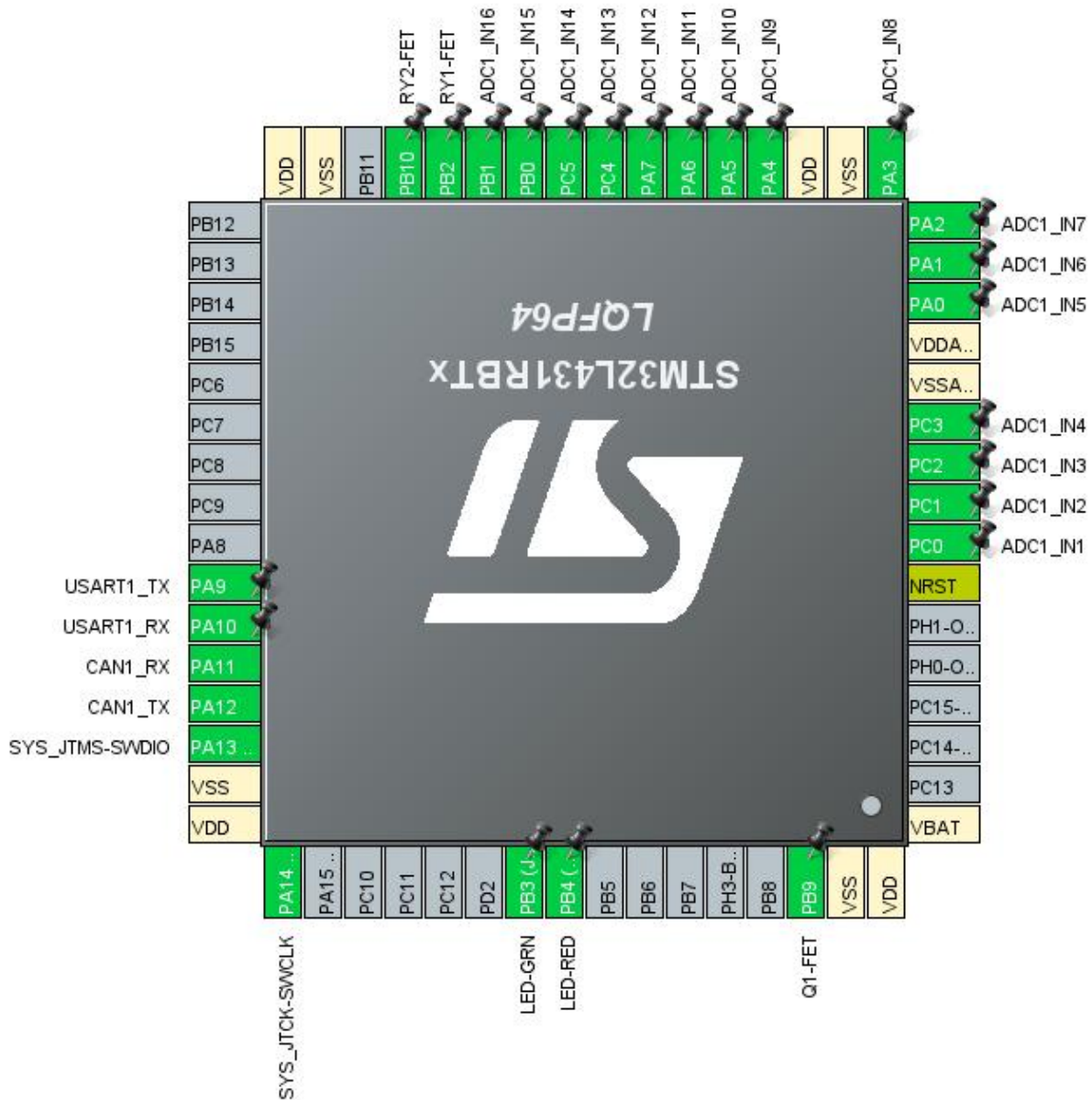
### 1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x1
MCU name	STM32L431RBTx
MCU Package	LQFP64
MCU Pin number	64

### 1.3. Core(s) information

Core(s)	Arm Cortex-M4
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## 2. Pinout Configuration



(Rotated +180°)

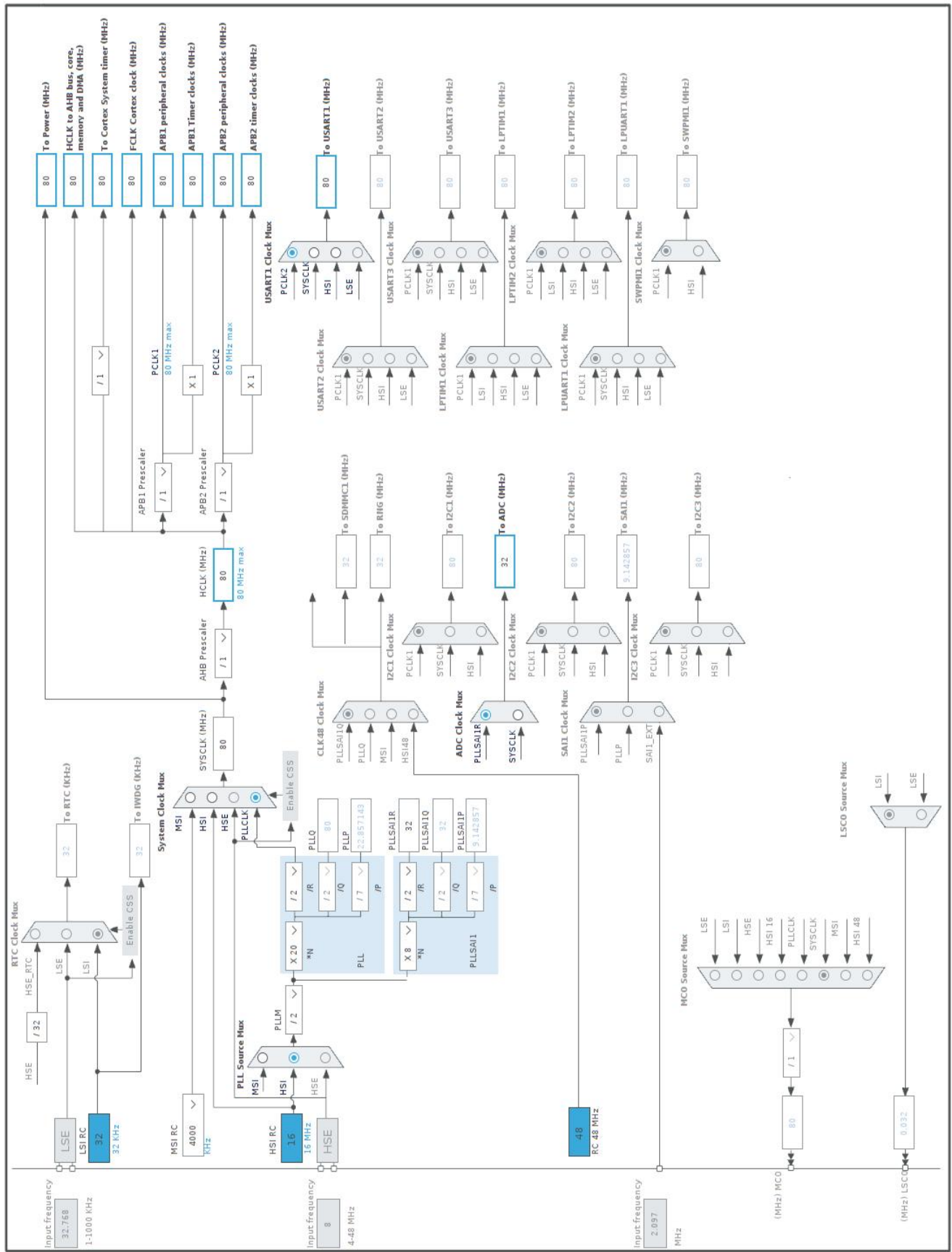
### 3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
7	NRST	Reset		
8	PC0	I/O	ADC1_IN1	
9	PC1	I/O	ADC1_IN2	
10	PC2	I/O	ADC1_IN3	
11	PC3	I/O	ADC1_IN4	
12	VSSA/VREF-	Power		
13	VDDA/VREF+	Power		
14	PA0	I/O	ADC1_IN5	
15	PA1	I/O	ADC1_IN6	
16	PA2	I/O	ADC1_IN7	
17	PA3	I/O	ADC1_IN8	
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	ADC1_IN9	
21	PA5	I/O	ADC1_IN10	
22	PA6	I/O	ADC1_IN11	
23	PA7	I/O	ADC1_IN12	
24	PC4	I/O	ADC1_IN13	
25	PC5	I/O	ADC1_IN14	
26	PB0	I/O	ADC1_IN15	
27	PB1	I/O	ADC1_IN16	
28	PB2 *	I/O	GPIO_Output	RY1-FET
29	PB10 *	I/O	GPIO_Output	RY2-FET
31	VSS	Power		
32	VDD	Power		
42	PA9	I/O	USART1_TX	
43	PA10	I/O	USART1_RX	
44	PA11	I/O	CAN1_RX	
45	PA12	I/O	CAN1_TX	
46	PA13 (JTMS-SWDIO)	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDD	Power		
49	PA14 (JTCK-SWCLK)	I/O	SYS_JTCK-SWCLK	
55	PB3 (JTDO-TRACESWO) *	I/O	GPIO_Output	LED-GRN
56	PB4 (NJTRST) *	I/O	GPIO_Output	LED-RED

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
62	PB9 *	I/O	GPIO_Output	Q1-FET
63	VSS	Power		
64	VDD	Power		

\* The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 5. Software Project

### 5.1. Project Settings

Name	Value
Project Name	BMScableL431
Project Folder	/home/deh/GliderWinchItems/BMScable/pcb/BMScableL431
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_L4 V1.17.0
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_ADC1_Init	ADC1
5	MX_USART1_UART_Init	USART1
6	MX_CAN1_Init	CAN1

## 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x1
MCU	STM32L431RBTx
Datasheet	DS11453_Rev1

### 6.2. Parameter Selection

Temperature	25
Vdd	3.0

### 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1



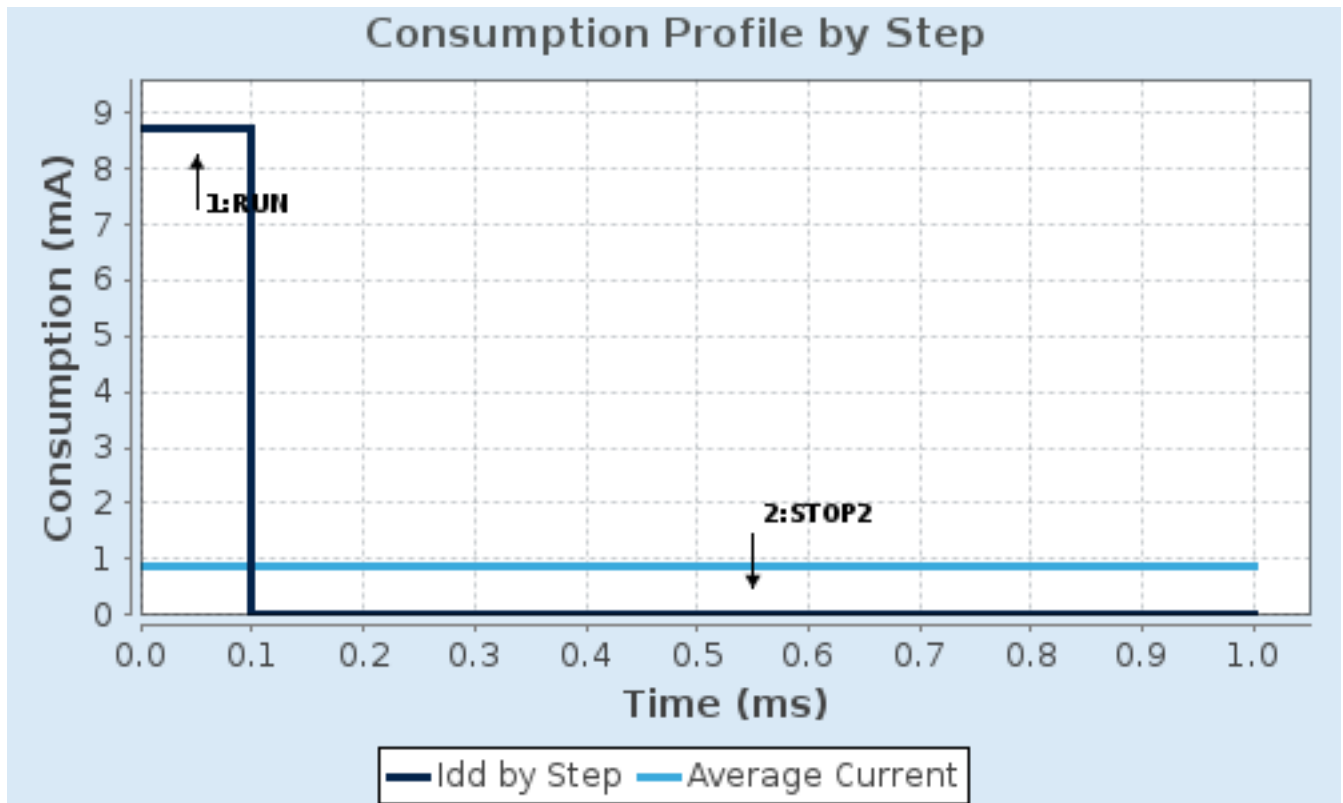
#### 6.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP2
<b>Vdd</b>	3.0	3.0
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	Range1-High	NoRange
<b>Fetch Type</b>	SRAM2	n/a
<b>CPU Frequency</b>	80 MHz	0 Hz
<b>Clock Configuration</b>	HSE BYP PLL	ALL CLOCKS OFF
<b>Clock Source Frequency</b>	4 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	8.71 mA	1.06 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	100.0	0.0
<b>Ta Max</b>	103.82	105
<b>Category</b>	In DS Table	In DS Table

#### 6.5. Results

Sequence Time	1 ms	Average Current	871.95 $\mu$ A
Battery Life	5 months, 9 days, 16 hours	Average DMIPS	100.0 DMIPS

#### 6.6. Chart



## 7. Peripherals and Middlewares Configuration

### 7.1. ADC1

IN1: IN1 Single-ended

IN2: IN2 Single-ended

IN3: IN3 Single-ended

IN4: IN4 Single-ended

IN5: IN5 Single-ended

IN6: IN6 Single-ended

IN7: IN7 Single-ended

IN8: IN8 Single-ended

IN9: IN9 Single-ended

IN10: IN10 Single-ended

IN11: IN11 Single-ended

IN12: IN12 Single-ended

IN13: IN13 Single-ended

IN14: IN14 Single-ended

IN15: IN15 Single-ended

mode: IN16 Single-ended

IN17: Temperature Sensor Channel

mode: Vrefint Channel

#### 7.1.1. Parameter Settings:

##### ADC\_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	<b>Enabled *</b>
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled

##### ADC\_Regular\_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	<b>16 *</b>

External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
<u>Rank</u>	1
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
<u>Rank</u>	<b>2 *</b>
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
<u>Rank</u>	<b>3 *</b>
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
<u>Rank</u>	<b>4 *</b>
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
<u>Rank</u>	<b>5 *</b>
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
<u>Rank</u>	<b>6 *</b>
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
<u>Rank</u>	<b>7 *</b>
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
<u>Rank</u>	<b>8 *</b>
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
<u>Rank</u>	<b>9 *</b>
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
<u>Rank</u>	<b>10 *</b>
Channel	Channel 1
Sampling Time	2.5 Cycles

Offset Number	No offset
<u>Rank</u>	<b>11 *</b>
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
<u>Rank</u>	<b>12 *</b>
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
<u>Rank</u>	<b>13 *</b>
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
<u>Rank</u>	<b>14 *</b>
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
<u>Rank</u>	<b>15 *</b>
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
<u>Rank</u>	<b>16 *</b>
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
<b>ADC_Injected_ConversionMode:</b>	
Enable Injected Conversions	<b>Enable *</b>
Enable Injected Oversampling	Disable
Number Of Conversions	<b>2 *</b>
External Trigger Source	Injected Conversion launched by software
External Trigger Conversion Edge	None
Injected Conversion Mode	None
Injected Queue	Injected Queue Disable
<u>Rank</u>	1
Channel	<b>Channel Vrefint *</b>
Sampling Time	<b>640.5 Cycles *</b>
Offset Number	No offset
Monitored by	None
<u>Rank</u>	<b>2 *</b>
Channel	<b>Channel Vrefint *</b>

Sampling Time	<b>640.5 Cycles *</b>
Offset Number	No offset
Monitored by	None
<b>Analog Watchdog 1:</b>	
Enable Analog WatchDog1 Mode	false
<b>Analog Watchdog 2:</b>	
Enable Analog WatchDog2 Mode	false
<b>Analog Watchdog 3:</b>	
Enable Analog WatchDog3 Mode	false

## 7.2. CAN1

**mode: Activated**

### 7.2.1. Parameter Settings:

#### **Bit Timings Parameters:**

Prescaler (for Time Quantum)	<b>20 *</b>
Time Quantum	<b>250.0 *</b>
Time Quanta in Bit Segment 1	<b>2 Times *</b>
Time Quanta in Bit Segment 2	<b>5 Times *</b>
Time for one Bit	<b>2000.00 *</b>
Baud Rate	<b>500000 *</b>
ReSynchronization Jump Width	1 Time

#### **Basic Parameters:**

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	<b>Enable *</b>

#### **Advanced Parameters:**

Operating Mode	Normal
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## 7.3. RCC

### 7.3.1. Parameter Settings:

#### **System Parameters:**

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

**RCC Parameters:**

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

**Power Parameters:**

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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## 7.4. SYS

### Debug: Serial Wire

Timebase Source: TIM15

## 7.5. USART1

### Mode: Asynchronous

#### 7.5.1. Parameter Settings:

**Basic Parameters:**

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

**Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

**Advanced Features:**

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable

MSB First Disable

## 7.6. FREERTOS

### Interface: CMSIS\_V2

#### 7.6.1. Config parameters:

##### API:

FreeRTOS API CMSIS v2

##### Versions:

FreeRTOS version 10.3.1

CMSIS-RTOS version 2.00

##### MPU/FPU:

ENABLE\_MPU Disabled

ENABLE\_FPU Disabled

##### Kernel settings:

USE\_PREEMPTION Enabled

CPU\_CLOCK\_HZ SystemCoreClock

TICK\_RATE\_HZ 1000

MAX\_PRIORITIES 56

MINIMAL\_STACK\_SIZE 128

MAX\_TASK\_NAME\_LEN 16

USE\_16\_BIT\_TICKS Disabled

IDLE\_SHOULD\_YIELD Enabled

USE\_MUTEXES Enabled

USE\_RECURSIVE\_MUTEXES Enabled

USE\_COUNTING\_SEMAPHORES Enabled

QUEUE\_REGISTRY\_SIZE 8

USE\_APPLICATION\_TASK\_TAG Disabled

ENABLE\_BACKWARD\_COMPATIBILITY Enabled

USE\_PORT\_OPTIMISED\_TASK\_SELECTION Disabled

USE\_TICKLESS\_IDLE Disabled

USE\_TASK\_NOTIFICATIONS Enabled

RECORD\_STACK\_HIGH\_ADDRESS Disabled

##### Memory management settings:

Memory Allocation Dynamic / Static

TOTAL\_HEAP\_SIZE 3000

Memory Management scheme heap\_4

##### Hook function related definitions:

USE\_IDLE\_HOOK Disabled

USE\_TICK\_HOOK Disabled



USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

**Run time and task stats gathering related definitions:**

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

**Co-routine related definitions:**

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

**Software timer definitions:**

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

**Interrupt nesting behaviour configuration:**

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

**Added with 10.2.1 support:**

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

**CMSIS-RTOS V2 flags:**

USE_OS2_THREAD_SUSPEND_RESUME	Enabled
USE_OS2_THREAD_ENUMERATE	Enabled
USE_OS2_EVENTFLAGS_FROM_ISR	Enabled
USE_OS2_THREAD_FLAGS	Enabled
USE_OS2_TIMER	Enabled
USE_OS2_MUTEX	Enabled

7.6.2. Include parameters:

**Include definitions:**

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled

xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Enabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

### 7.6.3. Advanced settings:

#### **Newlib settings (see parameter description first):**

USE\_NEWLIB\_REENTRANT                      Disabled

#### **Project settings (see parameter description first):**

Use FW pack heap file                      Enabled

**\* User modified value**

## 8. System Configuration

### 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN1	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PC1	ADC1_IN2	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PC2	ADC1_IN3	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PC3	ADC1_IN4	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA0	ADC1_IN5	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA1	ADC1_IN6	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA2	ADC1_IN7	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA3	ADC1_IN8	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA4	ADC1_IN9	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA5	ADC1_IN10	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA6	ADC1_IN11	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA7	ADC1_IN12	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PC4	ADC1_IN13	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PC5	ADC1_IN14	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PB0	ADC1_IN15	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PB1	ADC1_IN16	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
CAN1	PA11	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA12	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SYS	PA13 (JTMS-SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA14 (JTCK-SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
GPIO	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RY1-FET
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RY2-FET
	PB3 (JTDO-TRACESWO)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED-GRN
	PB4 (NJTRST)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED-RED
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Q1-FET

## 8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low
USART1_RX	DMA1_Channel5	Peripheral To Memory	Low
USART1_TX	DMA1_Channel4	Memory To Peripheral	Low

### ADC1: DMA1\_Channel1 DMA request Settings:

Mode: Normal  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Half Word  
Memory Data Width: Half Word

### USART1\_RX: DMA1\_Channel5 DMA request Settings:

Mode: Normal  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

### USART1\_TX: DMA1\_Channel4 DMA request Settings:

Mode: **Circular \***  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

### 8.3. NVIC configuration

#### 8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 channel1 global interrupt	true	5	0
DMA1 channel4 global interrupt	true	5	0
DMA1 channel5 global interrupt	true	5	0
TIM1 break interrupt and TIM15 global interrupt	true	15	0
USART1 global interrupt	true	5	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 global interrupt	unused		
CAN1 TX interrupt	unused		
CAN1 RX0 interrupt	unused		
CAN1 RX1 interrupt	unused		
CAN1 SCE interrupt	unused		
FPU global interrupt	unused		

#### 8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
DMA1 channel1 global interrupt	false	true	true
DMA1 channel4 global interrupt	false	true	true
DMA1 channel5 global interrupt	false	true	true
TIM1 break interrupt and TIM15 global interrupt	false	true	true
USART1 global interrupt	false	true	true

\* User modified value

## 9. System Views

### 9.1. Category view

#### 9.1.1. Current

#### Middleware

FREERTOS ✓

#### System Core

DMA ✓

GPIO ✓

NVIC ✓

RCC ✓

SYS ✓

#### Analog

ADC1 ✓

#### Timers

#### Connectivity

CAN1 ✓

USART1 ✓

#### Multimedia

#### Security

#### Computing



## 10. Docs & Resources

Type	Link
Datasheet	<a href="http://www.st.com/resource/en/datasheet/DM00257211.pdf">http://www.st.com/resource/en/datasheet/DM00257211.pdf</a>
Reference manual	<a href="http://www.st.com/resource/en/reference_manual/DM00151940.pdf">http://www.st.com/resource/en/reference_manual/DM00151940.pdf</a>
Programming manual	<a href="http://www.st.com/resource/en/programming_manual/DM00046982.pdf">http://www.st.com/resource/en/programming_manual/DM00046982.pdf</a>
Errata sheet	<a href="http://www.st.com/resource/en/errata_sheet/DM00218224.pdf">http://www.st.com/resource/en/errata_sheet/DM00218224.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00160362.pdf">http://www.st.com/resource/en/application_note/CD00160362.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00167594.pdf">http://www.st.com/resource/en/application_note/CD00167594.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00211314.pdf">http://www.st.com/resource/en/application_note/CD00211314.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00259245.pdf">http://www.st.com/resource/en/application_note/CD00259245.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264321.pdf">http://www.st.com/resource/en/application_note/CD00264321.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264342.pdf">http://www.st.com/resource/en/application_note/CD00264342.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264379.pdf">http://www.st.com/resource/en/application_note/CD00264379.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00042534.pdf">http://www.st.com/resource/en/application_note/DM00042534.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00072315.pdf">http://www.st.com/resource/en/application_note/DM00072315.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00073742.pdf">http://www.st.com/resource/en/application_note/DM00073742.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00073853.pdf">http://www.st.com/resource/en/application_note/DM00073853.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00080497.pdf">http://www.st.com/resource/en/application_note/DM00080497.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00081379.pdf">http://www.st.com/resource/en/application_note/DM00081379.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00085385.pdf">http://www.st.com/resource/en/application_note/DM00085385.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00087593.pdf">http://www.st.com/resource/en/application_note/DM00087593.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00125306.pdf">http://www.st.com/resource/en/application_note/DM00125306.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00129215.pdf">http://www.st.com/resource/en/application_note/DM00129215.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00141025.pdf">http://www.st.com/resource/en/application_note/DM00141025.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00144612.pdf">http://www.st.com/resource/en/application_note/DM00144612.pdf</a>
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