**A. Overview**

The following is a description of the design and layout of the pcb for testing the ribbon cable connections to the BMS battery module before plugging it into the BMS board.

The files may be found in the github repository--

**GliderWinchItems/BMScable**

The description is based on the files in **../pcb/BMScableL431/eagleNucleo**

The basic problem is that if the ribbon cable wires to the battery module cells are in the wrong sequence the bms chip on the bms board may be damaged due to polarity reversal or over-voltage. The cable IDC connector is plugged into this cable tester after wiring to the battery module and it checks that the wiring is correct.

There are several possible problems--

1. Wire is open (not connected)

2. Cell sequence is incorrect (wires reversed, ect.)

3. Ribbon crimped upside down (negative voltages)

Each wire from the ribbon cable, except (expected) ground goes though a resistor divider with large series resistor (e.g. 680K) and smaller value to ground, (e.g. 33K). Under normal circumstances this divider measures the voltage of each wire with the ADC on the processor. The voltages would range from one cell at low charge producing a voltage of approximately 3.0v to 16 cells at max giving approximately 67v (4.2 LiPo cells). The measured voltages of the 16 cells should be in the correct sequence.

Open wires would give an adc reading of approximately zero voltage.

If the ribbon is flipped-over and crimped “backwards” the voltages will be negative. To avoid problems Schottky diodes protect the adc input pins. A non-processor/software check is a pair of green/red LEDs with a large series resistor (e.g. 100K) across the battery module plus and minus. RED would indicate a reversed ribbon. The software will (likely) see this situation as “all zero” which could be mean either the cable is not plugged or negative voltages. The LEDs visually resolve these two possible situations.

The TI BQ76952 bms IC includes Kelvin sensing of a current sense resistor in the minus end of the battery module. Those wires will be essentially at ground as far as this tester’s ADC is concerned. To check for open circuit on these wires a large resistor (e.g. 680K) is added and connected to +5v. This should provide sufficient offset voltage so that an open wire will show a small voltage, whereas connected to ground will be zero, and yet a miswiring to the top of the battery module does not exceed the ADC max input voltage.

The board design was made to either plug into a Nucleo 446R board, or have a STM32L431RxT6, STM32F405RxT6, or STM32F446RxT6 processor on-board and avoid the need the for the Nucleo board. Part of this approach was to test the PCBCart.com proto-service which is inexpensive, but does not place solder-mask between smd pads. Should that be a problem, then boards can be used by using the header with Nucleo board.

Another incentive for doing this board was to avoid re-wiring a perf-board with headers that plugs into a Nucleo 446R that was wired for the 18 cell LTC-6813-1 bms IC which is either not available or has a lead-time measured in years.

**B. More detail**

**Relays**

The processors provide 16 ADC external inputs. The header for the ribbon cable is keyed 2x10, i.e. twenty wires. One of the wires is ground. The other 19 are fair-game for connection. This means there are three more than ADC inputs. To handle this, three SPDT contacts of two DPDT relays are used to switch three ADC inputs between ribbon cable wires.

The NC contacts on the relays are chosen so that these are cell voltages and the NO contacts are for testing the current sense wires and C0 (bottom cell ground). With this arrangement the board could be used for a low resolution battery cell monitoring, by using the provision for an isolated CAN driver feature (described later), and no relay operation would be required. (Or, simply omit the relay and jumper the COM and NC pads.)

RY1 – FET101 – PB10 drive

NC COM NO

C2 PB1 SRP

RY2 – FET100 -PB2 drive

NC COM NO

C4 PB0 SRN

C8 PB0 C0

**JP4 keyed 2x10 header and ribbon wiring**

The following table lists the header pin number versus ‘L431 processor ADC pin, ribbon cable color and battery module cell number (plus current sense wires).

The header-to-processor ADC pcb traces connect header pins to selected ADC pins without crossovers. The corresponding Nucleo header pins results in many crossovers, but spacing is not a problem.

col 1: 2x10 header pin number

col 2: battery module cell number

col 3: ADC number (note 1)

col 4: ADC i/o port-pin (and relay)

col 5: 20 pin ribbon color

col 6: battery module cell number

col 7: additional description

---------TOP SPLIT-------------

1 SRN : IN-16 : PB1 RY1-ON : BLK - \_\_\_ (BATTERY MODULE MINUS)

2 SRP : IN-15 : PB0 RY2-ON : WHT - SRP (CURRENT SENSE POS)

3 GND : –---- : GND : GRY - VSS (CURRENT SENSE NEG)P

4 C0 : IN-14 : PC5 RY2-ON : PUR - C0 (CELL #1 MINUS)

5 C2 : IN-16 : PB1 RY1-OFF: BLU - C2 ( CELL #2 PLUS)

6 C4 : IN-15 : PB0 RY2-OFF: GRN - C4

7 C6 : IN-13 : PC4 : YEL - C6

8 C8 : IN-14 : PC5 RY2-OFF: ORG - C8

9 C10 : IN-11 : PA6 : RED - C10

10 C12 : IN-12 : PA7 : BRN - C12

11 C14 : IN-9 : PA4 : BLK - C14

12 C16 : IN-10 : PA5 : WHT - C16 (CELL #16 PLUS) (BATTERY MODULE PLUS)

----------BOTTOM SPLIT ---------

13 C1 : IN-7 : PA2 : GRY - C1 (CELL #1 PLUS)

14 C3 : IN-8 : PA3 : PUR - C3

15 C5 : IN-5 : PA0 : BLU - C5

16 C7 : IN-6 : PA1 : GRN - C7

17 C9 : IN-3 : PC2 : YEL - C9

18 C11 : IN-4 : PC3 : ORG - C11

19 C13 : IN-1 : PC0 : RED - C13

20 C15 : IN-2 : PC1 : BRN – C15

(note 1) - L431 ADC numbers are listed. For the same i/o port-pin numbers, the F405 and F446 ADC numbering is different (e.g. IN-15 is ‘L431 PB0 and ‘F405 PC5. ‘L431 is IN-1 thru IN-16, whereas ‘F405 is IN-0 thru IN-15). This mapping can be handled by ADC register setup for the ADC scan sequence (e.g. in STM32CubeMX), or later mapping in software.

**Serial-USB**

Provision is present for a five pin FTDI header (JP5) and/or on-board FTDI knock-off module. These connect to PA9 and PA10, for USART1 communication.

The FTDI knock-off module provides an option for powering the board with 5v from the USB to power via diode D7 and jumper on JP1/JP2

**LEDs**

col1 – LED .sch number

col2 – color

col3 – PCB processor pin

col4 – Nucleo header pin

col5 – description

LED1 GRN PB3 PA13 Processor controlled (pulldown = on)

LED2 RED PB4 PA14 Processor controlled (pulldown = on)

LED3 RED GND-C16 Wired-reverse polarity = on

LED4 GRN C16-GND Wired-correct polarity = on

**CAN driver**

An isolated CAN driver (8-pin versions of ISO-1042, ISO-1044) could be fitted with header JP8 and connected to an existing sub-board configured without the driver. The sub-board has provision for an ISO-1050 which is more expensive.

For non-isolated CAN, header JP3 could wired to the sub-board with the MCP-2551 or equivalent.

An option for powering the board via the CAN and sub-board is via D6 and a JP1/JP2 jumper.

**XTAL HSE**

A JIC feature is the the High Speed External oscillator can be fitted with crystal (XTAL1) should more accurate control of the system clock be needed.

**Spare jic FET**

Spare Fet for external FET Q1, with gate drive PB8.

Header JP9:

1 – gnd

2 – FET drain

3 – FET drain diode cathode