STM32
CubeMX

# 1. Description

## 1.1. Project

| | |
|---|---|
| Project Name | F446 |
| Board Name | custom |
| Generated with: | STM32CubeMX 6.3.0 |
| Date | 10/30/2023 |

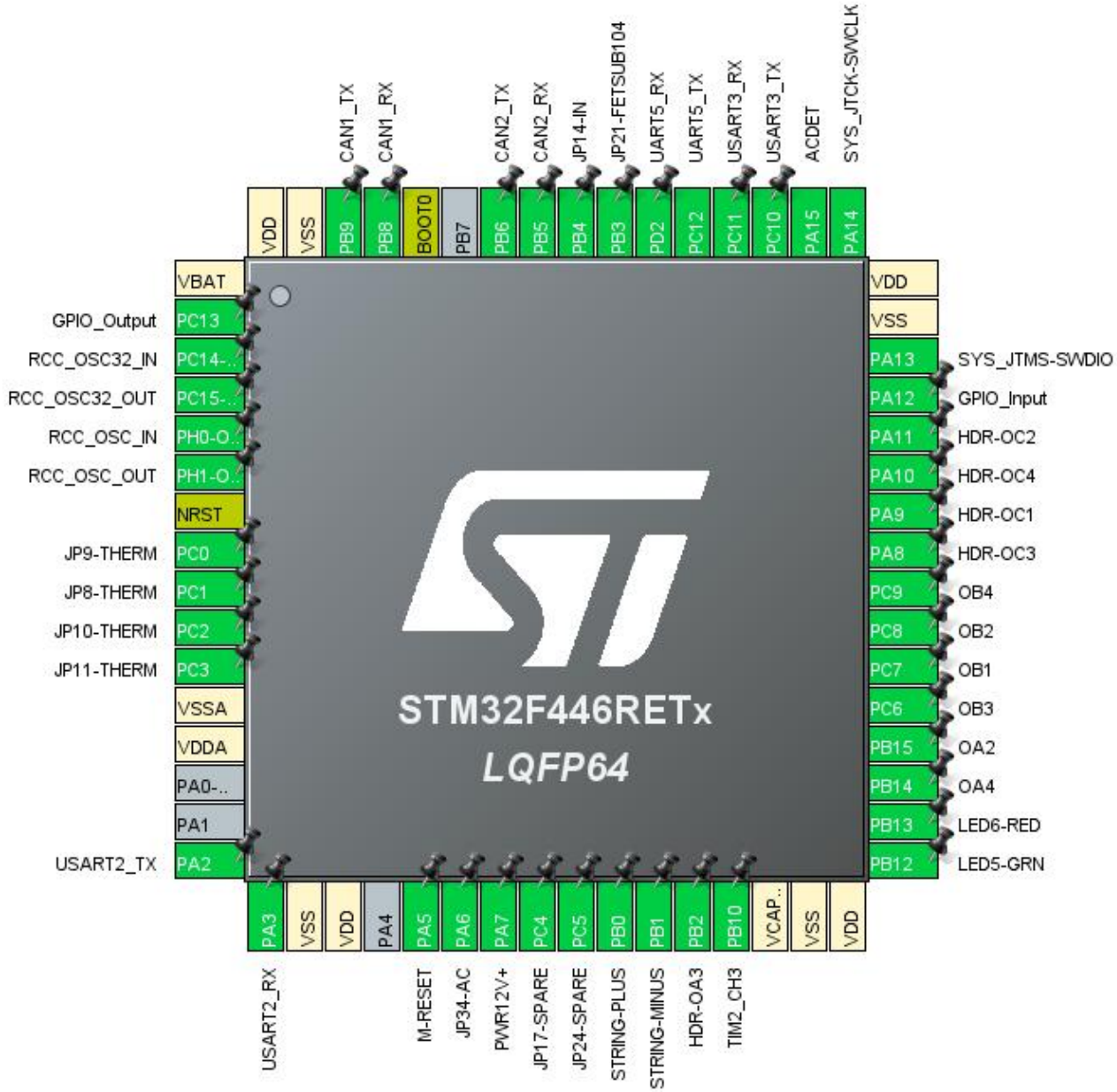
## 1.2. MCU

| | |
|---|---|
| MCU Series | STM32F4 |
| MCU Line | STM32F446 |
| MCU name | STM32F446RETx |
| MCU Package | LQFP64 |
| MCU Pin number | 64 |

## 1.3. Core(s) information

| | |
|---|---|
| Core(s) | Arm Cortex-M4 |

## 2. Pinout Configuration



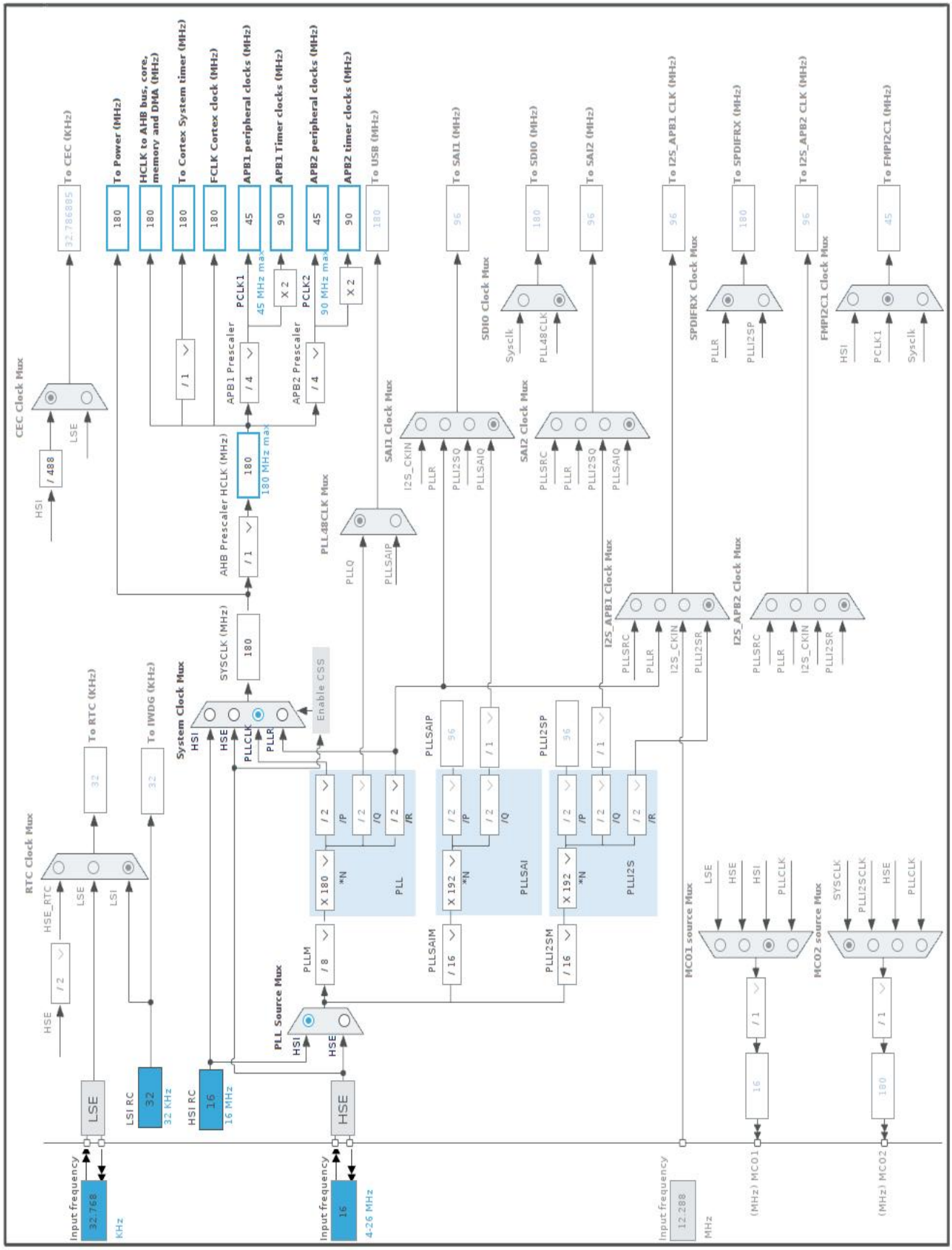
# 3. Pins Configuration

| Pin Number LQFP64 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 1 | VBAT | Power | | |
| 2 | PC13 * | I/O | GPIO_Output | |
| 3 | PC14-OSC32_IN | I/O | RCC_OSC32_IN | |
| 4 | PC15-OSC32_OUT | I/O | RCC_OSC32_OUT | |
| 5 | PH0-OSC_IN | I/O | RCC_OSC_IN | |
| 6 | PH1-OSC_OUT | I/O | RCC_OSC_OUT | |
| 7 | NRST | Reset | | |
| 8 | PC0 | I/O | ADC2_IN10, ADC3_IN10, ADC1_IN10 | JP9-THERM |
| 9 | PC1 | I/O | ADC2_IN11, ADC3_IN11, ADC1_IN11 | JP8-THERM |
| 10 | PC2 | I/O | ADC2_IN12, ADC3_IN12, ADC1_IN12 | JP10-THERM |
| 11 | PC3 | I/O | ADC2_IN13, ADC3_IN13, ADC1_IN13 | JP11-THERM |
| 12 | VSSA | Power | | |
| 13 | VDDA | Power | | |
| 16 | PA2 | I/O | USART2_TX | |
| 17 | PA3 | I/O | USART2_RX | |
| 18 | VSS | Power | | |
| 19 | VDD | Power | | |
| 21 | PA5 * | I/O | GPIO_Output | M-RESET |
| 22 | PA6 | I/O | ADC1_IN6 | JP34-AC |
| 23 | PA7 | I/O | ADC1_IN7 | PWR12V+ |
| 24 | PC4 | I/O | ADC1_IN14 | JP17-SPARE |
| 25 | PC5 | I/O | ADC1_IN15 | JP24-SPARE |
| 26 | PB0 | I/O | ADC1_IN8 | STRING-PLUS |
| 27 | PB1 | I/O | ADC1_IN9 | STRING-MINUS |
| 28 | PB2 | I/O | TIM2_CH4 | HDR-OA3 |
| 29 | PB10 | I/O | TIM2_CH3 | |
| 30 | VCAP_1 | Power | | |
| 31 | VSS | Power | | |
| 32 | VDD | Power | | |
| 33 | PB12 * | I/O | GPIO_Output | LED5-GRN |
| 34 | PB13 * | I/O | GPIO_Output | LED6-RED |
| 35 | PB14 | I/O | TIM12_CH1 | OA4 |

| Pin Number LQFP64 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 36 | PB15 | I/O | TIM12_CH2 | OA2 |
| 37 | PC6 | I/O | TIM3_CH1 | OB3 |
| 38 | PC7 | I/O | TIM3_CH2 | OB1 |
| 39 | PC8 | I/O | TIM3_CH3 | OB2 |
| 40 | PC9 | I/O | TIM3_CH4 | OB4 |
| 41 | PA8 | I/O | TIM1_CH1 | HDR-OC3 |
| 42 | PA9 | I/O | TIM1_CH2 | HDR-OC1 |
| 43 | PA10 | I/O | TIM1_CH3 | HDR-OC4 |
| 44 | PA11 | I/O | TIM1_CH4 | HDR-OC2 |
| 45 | PA12 * | I/O | GPIO_Input | |
| 46 | PA13 | I/O | SYS_JTMS-SWDIO | |
| 47 | VSS | Power | | |
| 48 | VDD | Power | | |
| 49 | PA14 | I/O | SYS_JTCK-SWCLK | |
| 50 | PA15 | I/O | TIM2_CH1 | ACDET |
| 51 | PC10 | I/O | USART3_TX | |
| 52 | PC11 | I/O | USART3_RX | |
| 53 | PC12 | I/O | UART5_TX | |
| 54 | PD2 | I/O | UART5_RX | |
| 55 | PB3 | I/O | TIM2_CH2 | JP21-FETSUB104 |
| 56 | PB4 * | I/O | GPIO_Input | JP14-IN |
| 57 | PB5 | I/O | CAN2_RX | |
| 58 | PB6 | I/O | CAN2_TX | |
| 60 | BOOT0 | Boot | | |
| 61 | PB8 | I/O | CAN1_RX | |
| 62 | PB9 | I/O | CAN1_TX | |
| 63 | VSS | Power | | |
| 64 | VDD | Power | | |

* The pin is affected with an I/O function

# 4. Clock Tree Configuration



# 5. Software Project

## 5.1. Project Settings

| Name | Value |
|---|---|
| Project Name | F446 |
| Project Folder | /home/deh/GliderWinchItems/bmsmot/emcmmc/F446 |
| Toolchain / IDE | Makefile |
| Firmware Package Name and Version | STM32Cube FW_F4 V1.26.2 |
| Application Structure | Advanced |
| Generate Under Root | No |
| Do not generate the main() | No |
| Minimum Heap Size | 0x200 |
| Minimum Stack Size | 0x400 |

## 5.2. Code Generation Settings

| Name | Value |
|---|---|
| STM32Cube MCU packages and embedded software | Copy all used libraries into the project folder |
| Generate peripheral initialization as a pair of '.c/.h' files | No |
| Backup previously generated files when re-generating | No |
| Keep User Code when re-generating | Yes |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |
| Enable Full Assert | No |

## 5.3. Advanced Settings - Generated Function Calls

| Rank | Function Name | Peripheral Instance Name |
|---|---|---|
| 1 | SystemClock_Config | RCC |
| 2 | MX_GPIO_Init | GPIO |
| 3 | MX_DMA_Init | DMA |
| 4 | MX_CAN1_Init | CAN1 |
| 5 | MX_CAN2_Init | CAN2 |
| 6 | MX_UART5_Init | UART5 |
| 7 | MX_USART2_UART_Init | USART2 |
| 8 | MX_USART3_UART_Init | USART3 |
| 9 | MX_TIM1_Init | TIM1 |
| 10 | MX_TIM2_Init | TIM2 |
| 11 | MX_ADC1_Init | ADC1 |

| Rank | Function Name | Peripheral Instance Name |
|---|---|---|
| 12 | MX_TIM3_Init | TIM3 |
| 13 | MX_TIM12_Init | TIM12 |
| 14 | MX_TIM5_Init | TIM5 |
| 15 | MX_TIM13_Init | TIM13 |
| 16 | MX_TIM9_Init | TIM9 |

# 6. Power Consumption Calculator report

## 6.1. Microcontroller Selection

| | |
|---|---|
| Series | STM32F4 |
| Line | STM32F446 |
| MCU | STM32F446RETx |
| Datasheet | DS10693_Rev6 |

## 6.2. Parameter Selection

| | |
|---|---|
| Temperature | 25 |
| Vdd | 3.3 |

## 6.3. Battery Selection

| | |
|---|---|
| Battery | Li-SOCL2(A3400) |
| Capacity | 3400.0 mAh |
| Self Discharge | 0.08 %/month |
| Nominal Voltage | 3.6 V |
| Max Cont Current | 100.0 mA |
| Max Pulse Current | 200.0 mA |
| Cells in series | 1 |
| Cells in parallel | 1 |

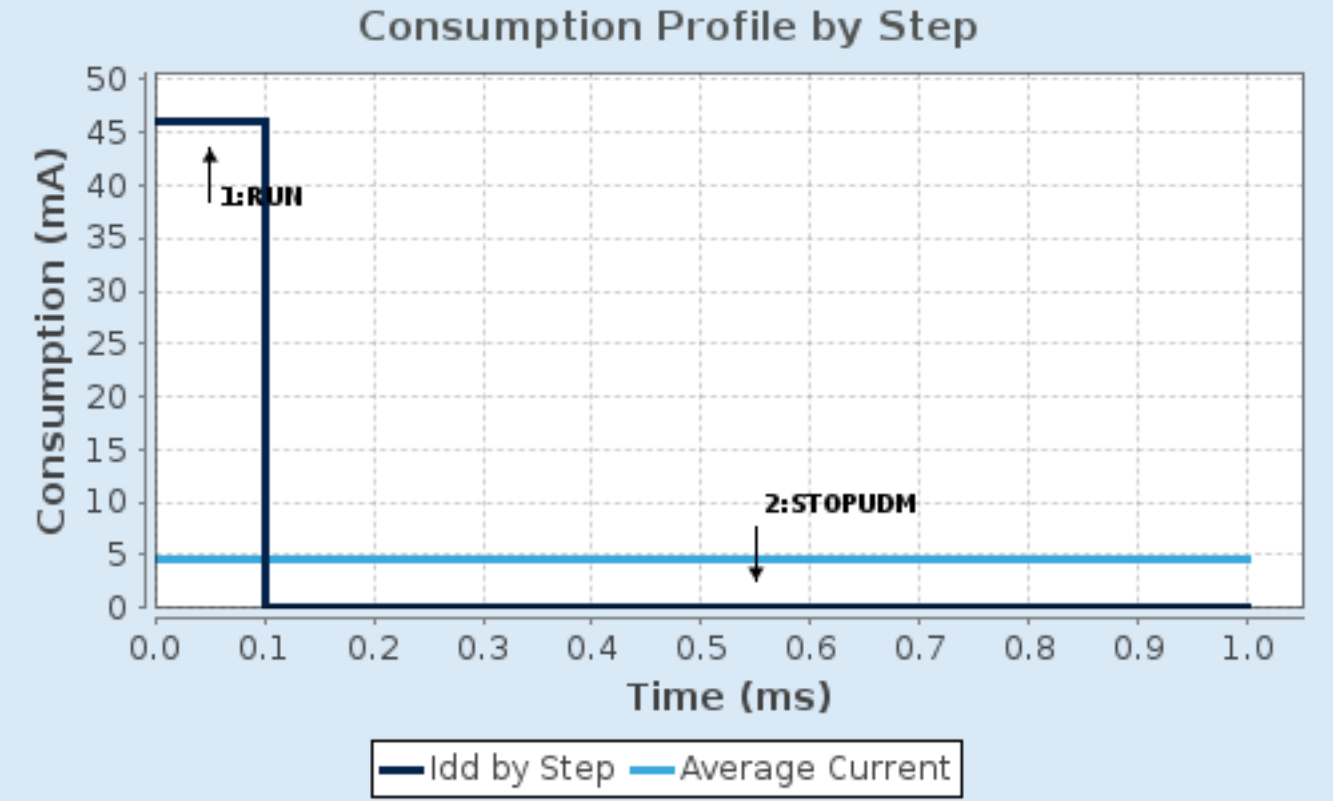
## 6.4. Sequence

| ***Step*** | Step1 | Step2 |
|---|---|---|
| ***Mode*** | RUN | STOP_UDM (Under Drive) |
| ***Vdd*** | 3.3 | 3.3 |
| ***Voltage Source*** | Battery | Battery |
| ***Range*** | Scale1-High | No Scale |
| ***Fetch Type*** | RAM/FLASH/REGON/ART/PREFETCH | n/a |
| ***CPU Frequency*** | 180 MHz | 0 Hz |
| ***Clock Configuration*** | HSE PLL | Regulator_LP Flash-PwrDwn |
| ***Clock Source Frequency*** | 4 MHz | 0 Hz |
| ***Peripherals*** | | |
| ***Additional Cons.*** | 0 mA | 0 mA |
| ***Average Current*** | 46 mA | 55 µA |
| ***Duration*** | 0.1 ms | 0.9 ms |
| ***DMIPS*** | 225.0 | 0.0 |
| ***Ta Max*** | 98.02 | 104.99 |
| ***Category*** | In DS Table | In DS Table |

## 6.5. Results

| | | | |
|---|---|---|---|
| Sequence Time | 1 ms | Average Current | 4.65 mA |
| Battery Life | 1 month | Average DMIPS | 225.0 DMIPS |

## 6.6. Chart


Consumption Profile by Step
Consumption (mA)
50
45
40
35
30
25
20
15
10
5
0
1:RUN
2:STOPUDM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

# 7. Peripherals and Middlewares Configuration

## 7.1. ADC1

**mode: IN6**

**mode: IN7**

**mode: IN8**

**mode: IN9**

**mode: IN10**

**mode: IN11**

**mode: IN12**

**mode: IN13**

**mode: IN14**

**mode: IN15**

**mode: Vrefint Channel**

**mode: Vbat Channel**

### 7.1.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | PCLK2 divided by 2 |
| Resolution | 12 bits (15 ADC Clock cycles) |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Enabled |
| Continuous Conversion Mode | **Enabled *** |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | **Enabled *** |
| End Of Conversion Selection | EOC flag at the end of single channel conversion |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Number Of Conversion | **12 *** |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | **Channel 10 *** |
| Sampling Time | **56 Cycles *** |
| Rank | **2 *** |
| Channel | **Channel 11 *** |
| Sampling Time | **56 Cycles *** |

| | |
|---|---|
| Rank | **3 *** |
| Channel | **Channel 12 *** |
| Sampling Time | **56 Cycles *** |
| Rank | **4 *** |
| Channel | **Channel 13 *** |
| Sampling Time | **56 Cycles *** |
| Rank | **5 *** |
| Channel | **Channel 14 *** |
| Sampling Time | **56 Cycles *** |
| Rank | **6 *** |
| Channel | **Channel 15 *** |
| Sampling Time | **56 Cycles *** |
| Rank | **7 *** |
| Channel | **Channel 7 *** |
| Sampling Time | **144 Cycles *** |
| Rank | **8 *** |
| Channel | **Channel 8 *** |
| Sampling Time | **56 Cycles *** |
| Rank | **9 *** |
| Channel | **Channel 9 *** |
| Sampling Time | **56 Cycles *** |
| Rank | **10 *** |
| Channel | Channel 6 |
| Sampling Time | **480 Cycles *** |
| Rank | **11 *** |
| Channel | **Channel Vbat *** |
| Sampling Time | **480 Cycles *** |
| Rank | **12 *** |
| Channel | **Channel Vrefint *** |
| Sampling Time | **480 Cycles *** |

### ADC_Injected_ConversionMode:

| | |
|---|---|
| Number Of Conversions | 0 |

### WatchDog:

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## 7.2. CAN1

## mode: Activated

### 7.2.1. Parameter Settings:

**Bit Timings Parameters:**

| | |
|---|---|
| Prescaler (for Time Quantum) | **10 *** |
| Time Quantum | **222.22222222222223 *** |
| Time Quanta in Bit Segment 1 | **6 Times *** |
| Time Quanta in Bit Segment 2 | **2 Times *** |
| Time for one Bit | **1999.99 *** |
| Baud Rate | **500000 *** |
| ReSynchronization Jump Width | 1 Time |

**Basic Parameters:**

| | |
|---|---|
| Time Triggered Communication Mode | Disable |
| Automatic Bus-Off Management | Disable |
| Automatic Wake-Up Mode | Disable |
| Automatic Retransmission | **Enable *** |
| Receive Fifo Locked Mode | Disable |
| Transmit Fifo Priority | Disable |

**Advanced Parameters:**

| | |
|---|---|
| Operating Mode | Normal |

## 7.3. CAN2

## mode: Activated

### 7.3.1. Parameter Settings:

**Bit Timings Parameters:**

| | |
|---|---|
| Prescaler (for Time Quantum) | **10 *** |
| Time Quantum | **222.22222222222223 *** |
| Time Quanta in Bit Segment 1 | **6 Times *** |
| Time Quanta in Bit Segment 2 | **2 Times *** |
| Time for one Bit | **1999.99 *** |
| Baud Rate | **500000 *** |
| ReSynchronization Jump Width | **2 Times *** |

**Basic Parameters:**

| | |
|---|---|
| Time Triggered Communication Mode | Disable |
| Automatic Bus-Off Management | Disable |
| Automatic Wake-Up Mode | Disable |
| Automatic Retransmission | **Enable *** |
| Receive Fifo Locked Mode | Disable |
| Transmit Fifo Priority | Disable |

**Advanced Parameters:**

| | |
|---|---|
| Operating Mode | Normal |

## 7.4. RCC

**High Speed Clock (HSE): Crystal/Ceramic Resonator**

**Low Speed Clock (LSE) : Crystal/Ceramic Resonator**

### 7.4.1. Parameter Settings:

**System Parameters:**

| | |
|---|---|
| VDD voltage (V) | 3.3 |
| Instruction Cache | Enabled |
| Prefetch Buffer | Enabled |
| Data Cache | Enabled |
| Flash Latency(WS) | 5 WS (6 CPU cycle) |

**RCC Parameters:**

| | |
|---|---|
| HSI Calibration Value | 16 |
| TIM Prescaler Selection | Disabled |
| HSE Startup Timout Value (ms) | 100 |
| LSE Startup Timout Value (ms) | 5000 |

**Power Parameters:**

| | |
|---|---|
| Power Regulator Voltage Scale | Power Regulator Voltage Scale 1 |
| Power Over Drive | Enabled |

## 7.5. SYS

**Debug: Serial Wire**

**Timebase Source: TIM14**

## 7.6. TIM1

**Clock Source : Internal Clock**

**Channel1: Output Compare CH1**

## Channel2: PWM Generation CH2
## Channel3: PWM Generation CH3
## Channel4: PWM Generation CH4

### 7.6.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **36000 *** |
| Internal Clock Division (CKD) | No Division |
| Repetition Counter (RCR - 8 bits value) | 0 |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

**Break And Dead Time management - BRK Configuration:**

| | |
|---|---|
| BRK State | Disable |
| BRK Polarity | High |

**Break And Dead Time management - Output Configuration:**

| | |
|---|---|
| Automatic Output State | Disable |
| Off State Selection for Run Mode (OSSR) | Disable |
| Off State Selection for Idle Mode (OSSI) | Disable |
| Lock Configuration | Off |

**Output Compare Channel 1:**

| | |
|---|---|
| Mode | Frozen (used for Timing base) |
| Pulse (16 bits value) | 0 |
| Output compare preload | Disable |
| CH Polarity | High |
| CH Idle State | Reset |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |
| CH Idle State | Reset |

**PWM Generation Channel 3:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |

| | |
|---|---|
| Fast Mode | Disable |
| CH Polarity | High |
| CH Idle State | Reset |

**PWM Generation Channel 4:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |
| CH Idle State | Reset |

## 7.7. TIM2

**Clock Source : Internal Clock**

**Channel1: Input Capture direct mode**

**Channel2: PWM Generation CH2**

**Channel3: PWM Generation CH3**

**Channel4: PWM Generation CH4**

### 7.7.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **2 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 32 bits value ) | **36000 *** |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

**Input Capture Channel 1:**

| | |
|---|---|
| Polarity Selection | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter (4 bits value) | 0 |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 3:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 4:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

## 7.8. TIM3

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

**Channel3: PWM Generation CH3**

**Channel4: PWM Generation CH4**

### 7.8.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **36000 *** |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |

| | |
|---|---|
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 3:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 4:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

## 7.9. TIM5

## mode: Clock Source

## Channel1: Output Compare No Output

### 7.9.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **9000 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 32 bits value ) | 4294967295 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

**Output Compare No Output Channel 1:**

| | |
|---|---|
| Mode | Frozen (used for Timing base) |
| Pulse (32 bits value) | 0 |
| Output compare preload | Disable |
| CH Polarity | High |

## 7.10. TIM9

**mode: Clock Source**

**mode: One Pulse Mode**

7.10.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **9000 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | 65535 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

## 7.11. TIM12

**mode: Clock Source**

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

7.11.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **36000 *** |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

## 7.12. TIM13

### mode: Activated

### Channel1: Output Compare No Output

#### 7.12.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **9000 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | 65535 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Output Compare No Output Channel 1:**

| | |
|---|---|
| Mode | Frozen (used for Timing base) |
| Pulse (16 bits value) | 0 |
| Output compare preload | Disable |
| CH Polarity | High |

## 7.13. UART5

### Mode: Asynchronous

#### 7.13.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | **Receive Only *** |
| Over Sampling | 16 Samples |

## 7.14. USART2

### Mode: Asynchronous

#### 7.14.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |

| | |
|---|---|
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |

## 7.15. USART3

## Mode: Asynchronous

### 7.15.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |

## 7.16. FREERTOS

## Interface: CMSIS_V1

### 7.16.1. Config parameters:

**API:**

| | |
|---|---|
| FreeRTOS API | CMSIS v1 |

**Versions:**

| | |
|---|---|
| FreeRTOS version | 10.3.1 |
| CMSIS-RTOS version | 1.02 |

**MPU/FPU:**

| | |
|---|---|
| ENABLE_MPU | Disabled |
| ENABLE_FPU | Disabled |

**Kernel settings:**

| | |
|---|---|
| USE_PREEMPTION | Enabled |
| CPU_CLOCK_HZ | SystemCoreClock |
| TICK_RATE_HZ | 1000 |
| MAX_PRIORITIES | 7 |

| | |
|---|---|
| MINIMAL_STACK_SIZE | 128 |
| MAX_TASK_NAME_LEN | 16 |
| USE_16_BIT_TICKS | Disabled |
| IDLE_SHOULD_YIELD | Enabled |
| USE_MUTEXES | Enabled |
| USE_RECURSIVE_MUTEXES | Disabled |
| USE_COUNTING_SEMAPHORES | Disabled |
| QUEUE_REGISTRY_SIZE | 8 |
| USE_APPLICATION_TASK_TAG | Disabled |
| ENABLE_BACKWARD_COMPATIBILITY | Enabled |
| USE_PORT_OPTIMISED_TASK_SELECTION | Enabled |
| USE_TICKLESS_IDLE | Disabled |
| USE_TASK_NOTIFICATIONS | Enabled |
| RECORD_STACK_HIGH_ADDRESS | Disabled |

### Memory management settings:

| | |
|---|---|
| Memory Allocation | Dynamic / Static |
| TOTAL_HEAP_SIZE | 15360 |
| Memory Management scheme | heap_4 |

### Hook function related definitions:

| | |
|---|---|
| USE_IDLE_HOOK | Disabled |
| USE_TICK_HOOK | Disabled |
| USE_MALLOC_FAILED_HOOK | Disabled |
| USE_DAEMON_TASK_STARTUP_HOOK | Disabled |
| CHECK_FOR_STACK_OVERFLOW | Disabled |

### Run time and task stats gathering related definitions:

| | |
|---|---|
| GENERATE_RUN_TIME_STATS | Disabled |
| USE_TRACE_FACILITY | Disabled |
| USE_STATS_FORMATTING_FUNCTIONS | Disabled |

### Co-routine related definitions:

| | |
|---|---|
| USE_CO_ROUTINES | Disabled |
| MAX_CO_ROUTINE_PRIORITIES | 2 |

### Software timer definitions:

| | |
|---|---|
| USE_TIMERS | Disabled |

### Interrupt nesting behaviour configuration:

| | |
|---|---|
| LIBRARY_LOWEST_INTERRUPT_PRIORITY | 15 |
| LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY | 5 |

### Added with 10.2.1 support:

| | |
|---|---|
| MESSAGE_BUFFER_LENGTH_TYPE | size_t |
| USE_POSIX_ERRNO | Disabled |

## 7.16.2. Include parameters:

**Include definitions:**

| | |
|---|---|
| vTaskPrioritySet | Enabled |
| uxTaskPriorityGet | Enabled |
| vTaskDelete | Enabled |
| vTaskCleanUpResources | Disabled |
| vTaskSuspend | Enabled |
| vTaskDelayUntil | Disabled |
| vTaskDelay | Enabled |
| xTaskGetSchedulerState | Enabled |
| xTaskResumeFromISR | Enabled |
| xQueueGetMutexHolder | Disabled |
| xSemaphoreGetMutexHolder | Disabled |
| pcTaskGetTaskName | Disabled |
| uxTaskGetStackHighWaterMark | Disabled |
| xTaskGetCurrentTaskHandle | Disabled |
| eTaskGetState | Disabled |
| xEventGroupSetBitFromISR | Disabled |
| xTimerPendFunctionCall | Disabled |
| xTaskAbortDelay | Disabled |
| xTaskGetHandle | Disabled |
| uxTaskGetStackHighWaterMark2 | Disabled |

## 7.16.3. Advanced settings:

**Newlib settings (see parameter description first):**

| | |
|---|---|
| USE_NEWLIB_REENTRANT | Disabled |

**Project settings (see parameter description first):**

| | |
|---|---|
| Use FW pack heap file | Enabled |

*** User modified value**

# 8. System Configuration

## 8.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| ADC1 | PC0 | ADC1_IN10 | Analog mode | No pull-up and no pull-down | n/a | JP9-THERM |
| | PC1 | ADC1_IN11 | Analog mode | No pull-up and no pull-down | n/a | JP8-THERM |
| | PC2 | ADC1_IN12 | Analog mode | No pull-up and no pull-down | n/a | JP10-THERM |
| | PC3 | ADC1_IN13 | Analog mode | No pull-up and no pull-down | n/a | JP11-THERM |
| | PA6 | ADC1_IN6 | Analog mode | No pull-up and no pull-down | n/a | JP34-AC |
| | PA7 | ADC1_IN7 | Analog mode | No pull-up and no pull-down | n/a | PWR12V+ |
| | PC4 | ADC1_IN14 | Analog mode | No pull-up and no pull-down | n/a | JP17-SPARE |
| | PC5 | ADC1_IN15 | Analog mode | No pull-up and no pull-down | n/a | JP24-SPARE |
| | PB0 | ADC1_IN8 | Analog mode | No pull-up and no pull-down | n/a | STRING-PLUS |
| | PB1 | ADC1_IN9 | Analog mode | No pull-up and no pull-down | n/a | STRING-MINUS |
| CAN1 | PB8 | CAN1_RX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PB9 | CAN1_TX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| CAN2 | PB5 | CAN2_RX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PB6 | CAN2_TX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| RCC | PC14-OSC32_IN | RCC_OSC32_IN | n/a | n/a | n/a | |
| | PC15-OSC32_OUT | RCC_OSC32_OUT | n/a | n/a | n/a | |
| | PH0-OSC_IN | RCC_OSC_IN | n/a | n/a | n/a | |
| | PH1-OSC_OUT | RCC_OSC_OUT | n/a | n/a | n/a | |
| SYS | PA13 | SYS_JTMS-SWDIO | n/a | n/a | n/a | |
| | PA14 | SYS_JTCK-SWCLK | n/a | n/a | n/a | |
| TIM1 | PA8 | TIM1_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | HDR-OC3 |
| | PA9 | TIM1_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | HDR-OC1 |
| | PA10 | TIM1_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | HDR-OC4 |
| | PA11 | TIM1_CH4 | Alternate Function Push Pull | No pull-up and no pull-down | Low | HDR-OC2 |
| TIM2 | PB2 | TIM2_CH4 | Alternate Function Push Pull | No pull-up and no pull-down | Low | HDR-OA3 |
| | PB10 | TIM2_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| | PA15 | TIM2_CH1 | **Alternate Function Open Drain *** | No pull-up and no pull-down | Low | ACDET |
| | PB3 | TIM2_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | JP21-FETSUB104 |
| TIM3 | PC6 | TIM3_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | OB3 |
| | PC7 | TIM3_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | OB1 |
| | PC8 | TIM3_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | OB2 |
| | PC9 | TIM3_CH4 | Alternate Function Push Pull | No pull-up and no pull-down | Low | OB4 |
| TIM12 | PB14 | TIM12_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | OA4 |
| | PB15 | TIM12_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | OA2 |
| UART5 | PC12 | UART5_TX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PD2 | UART5_RX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| USART2 | PA2 | USART2_TX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PA3 | USART2_RX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| USART3 | PC10 | USART3_TX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PC11 | USART3_RX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| GPIO | PC13 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PA5 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | M-RESET |
| | PB12 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | LED5-GRN |
| | PB13 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | LED6-RED |
| | PA12 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | |
| | PB4 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | JP14-IN |

## 8.2. DMA configuration

| DMA request | Stream | Direction | Priority |
|---|---|---|---|
| UART5_RX | DMA1_Stream0 | Peripheral To Memory | Low |
| USART2_TX | DMA1_Stream6 | Memory To Peripheral | Low |
| USART3_RX | DMA1_Stream1 | Peripheral To Memory | Low |
| USART3_TX | DMA1_Stream3 | Memory To Peripheral | Low |
| ADC1 | DMA2_Stream0 | Peripheral To Memory | Low |
| USART2_RX | DMA1_Stream5 | Peripheral To Memory | Low |

*UART5_RX: DMA1_Stream0 DMA request Settings:*

| | |
|---|---|
| Mode: | **Circular *** |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

*USART2_TX: DMA1_Stream6 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

*USART3_RX: DMA1_Stream1 DMA request Settings:*

| | |
|---|---|
| Mode: | **Circular *** |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

*USART3_TX: DMA1_Stream3 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### *ADC1: DMA2_Stream0 DMA request Settings:*

| | |
|---|---|
| Mode: | **Circular *** |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Half Word |
| Memory Data Width: | Half Word |

### *USART2_RX: DMA1_Stream5 DMA request Settings:*

| | |
|---|---|
| Mode: | **Circular *** |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

## 8.3. NVIC configuration

### 8.3.1. NVIC

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Pre-fetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 15 | 0 |
| System tick timer | true | 15 | 0 |
| DMA1 stream0 global interrupt | true | 5 | 0 |
| DMA1 stream1 global interrupt | true | 5 | 0 |
| DMA1 stream3 global interrupt | true | 5 | 0 |
| DMA1 stream5 global interrupt | true | 5 | 0 |
| DMA1 stream6 global interrupt | true | 5 | 0 |
| CAN1 TX interrupt | true | 5 | 0 |
| CAN1 RX0 interrupt | true | 5 | 0 |
| CAN1 RX1 interrupt | true | 5 | 0 |
| TIM1 break interrupt and TIM9 global interrupt | true | 8 | 0 |
| USART2 global interrupt | true | 5 | 0 |
| USART3 global interrupt | true | 5 | 0 |
| TIM8 update interrupt and TIM13 global interrupt | true | 8 | 0 |
| TIM8 trigger and commutation interrupts and TIM14 global interrupt | true | 15 | 0 |
| TIM5 global interrupt | true | 8 | 0 |
| UART5 global interrupt | true | 5 | 0 |
| DMA2 stream0 global interrupt | true | 5 | 0 |
| CAN2 TX interrupt | true | 5 | 0 |
| CAN2 RX0 interrupt | true | 5 | 0 |
| CAN2 RX1 interrupt | true | 5 | 0 |
| PVD interrupt through EXTI line 16 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| ADC1, ADC2 and ADC3 interrupts | unused | | |
| CAN1 SCE interrupt | unused | | |
| TIM1 update interrupt and TIM10 global interrupt | unused | | |
| TIM1 trigger and commutation interrupts and TIM11 global interrupt | unused | | |

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| TIM1 capture compare interrupt | unused | | |
| TIM2 global interrupt | unused | | |
| TIM3 global interrupt | unused | | |
| TIM8 break interrupt and TIM12 global interrupt | unused | | |
| CAN2 SCE interrupt | unused | | |
| FPU global interrupt | unused | | |

### 8.3.2. NVIC Code generation

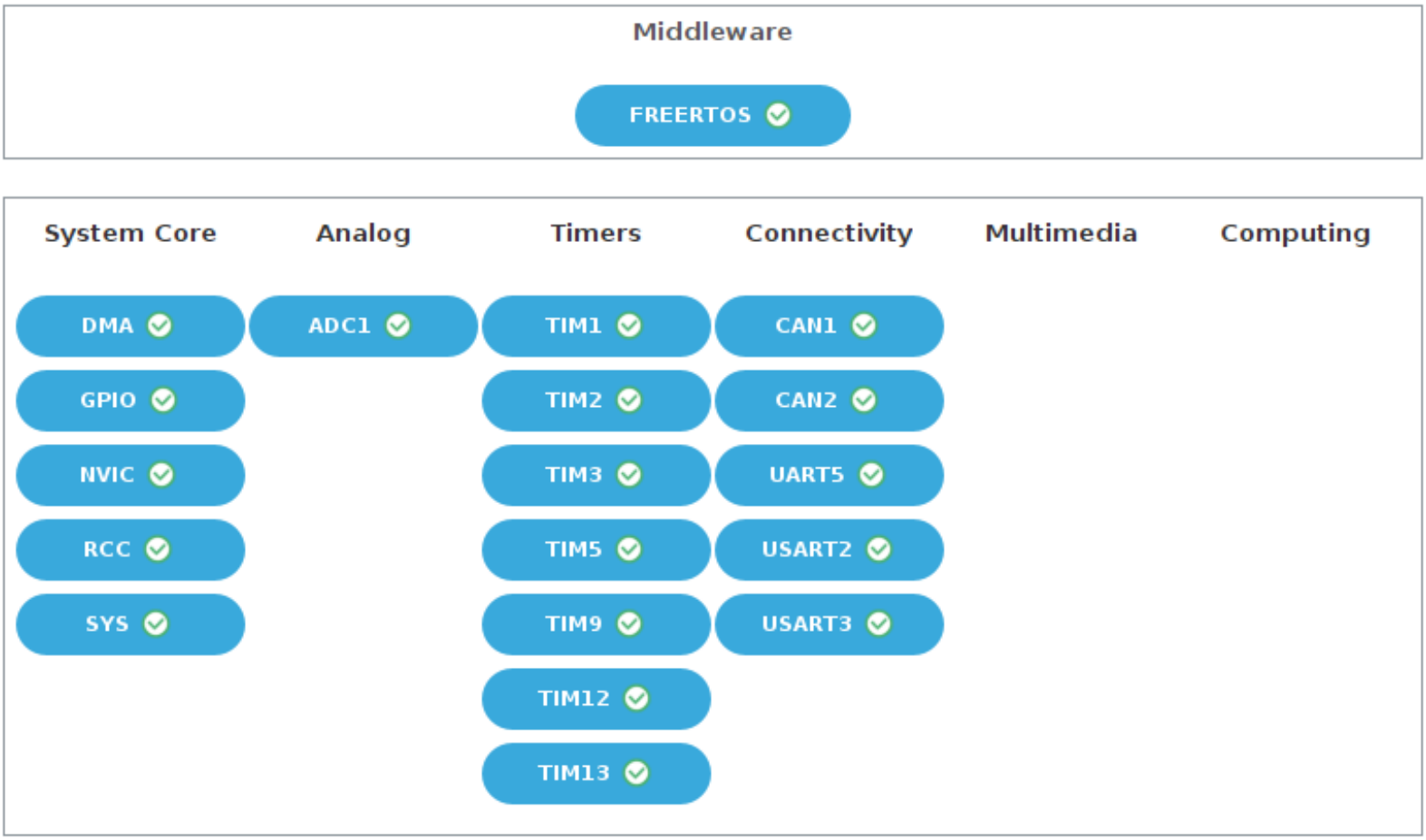
| Enabled interrupt Table | Select for init sequence ordering | Generate IRQ handler | Call HAL handler |
|---|---|---|---|
| Non maskable interrupt | false | true | false |
| Hard fault interrupt | false | true | false |
| Memory management fault | false | true | false |
| Pre-fetch fault, memory access fault | false | true | false |
| Undefined instruction or illegal state | false | true | false |
| System service call via SWI instruction | false | false | false |
| Debug monitor | false | true | false |
| Pendable request for system service | false | false | false |
| System tick timer | false | false | true |
| DMA1 stream0 global interrupt | false | true | true |
| DMA1 stream1 global interrupt | false | true | true |
| DMA1 stream3 global interrupt | false | true | true |
| DMA1 stream5 global interrupt | false | true | true |
| DMA1 stream6 global interrupt | false | true | true |
| CAN1 TX interrupt | false | true | true |
| CAN1 RX0 interrupt | false | true | true |
| CAN1 RX1 interrupt | false | true | true |
| TIM1 break interrupt and TIM9 global interrupt | false | true | true |
| USART2 global interrupt | false | true | true |
| USART3 global interrupt | false | true | true |
| TIM8 update interrupt and TIM13 global interrupt | false | true | true |
| TIM8 trigger and commutation interrupts and TIM14 global interrupt | false | true | true |
| TIM5 global interrupt | false | true | true |
| UART5 global interrupt | false | true | true |
| DMA2 stream0 global interrupt | false | true | true |
| CAN2 TX interrupt | false | true | true |
| CAN2 RX0 interrupt | false | true | true |
| CAN2 RX1 interrupt | false | true | true |

*** User modified value**

# 9. System Views

9.1. Category view

*9.1.1. Current*



# 10. Docs & Resources

| Type | Link |
|---|---|
| Datasheet | http://www.st.com/resource/en/datasheet/DM00141306.pdf |
| Reference manual | http://www.st.com/resource/en/reference_manual/DM00135183.pdf |
| Programming manual | http://www.st.com/resource/en/programming_manual/DM00046982.pdf |
| Errata sheet | http://www.st.com/resource/en/errata_sheet/DM00155929.pdf |
| Application note | http://www.st.com/resource/en/application_note/CD00167594.pdf |
| Application note | http://www.st.com/resource/en/application_note/CD00211314.pdf |
| Application note | http://www.st.com/resource/en/application_note/CD00249778.pdf |
| Application note | http://www.st.com/resource/en/application_note/CD00259245.pdf |
| Application note | http://www.st.com/resource/en/application_note/CD00264321.pdf |
| Application note | http://www.st.com/resource/en/application_note/CD00264342.pdf |
| Application note | http://www.st.com/resource/en/application_note/CD00264379.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00024853.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00040802.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00040808.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00042534.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00046011.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00072315.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00073742.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00073853.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00080497.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00081379.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00115714.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00129215.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00154959.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00160482.pdf |

| | |
|---|---|
| Application note | http://www.st.com/resource/en/application_note/DM00161778.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00213525.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00220769.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00226326.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00227538.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00236305.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00257177.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00272912.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00281138.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00296349.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00315319.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00327191.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00354244.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00373474.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00380469.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00395696.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00431633.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00493651.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00536349.pdf |
| Application note | http://www.st.com/resource/en/application_note/DM00725181.pdf |