



## 1. Description

### 1.1. Project

Project Name	drum
Board Name	custom
Generated with:	STM32CubeMX 6.0.1
Date	08/27/2020

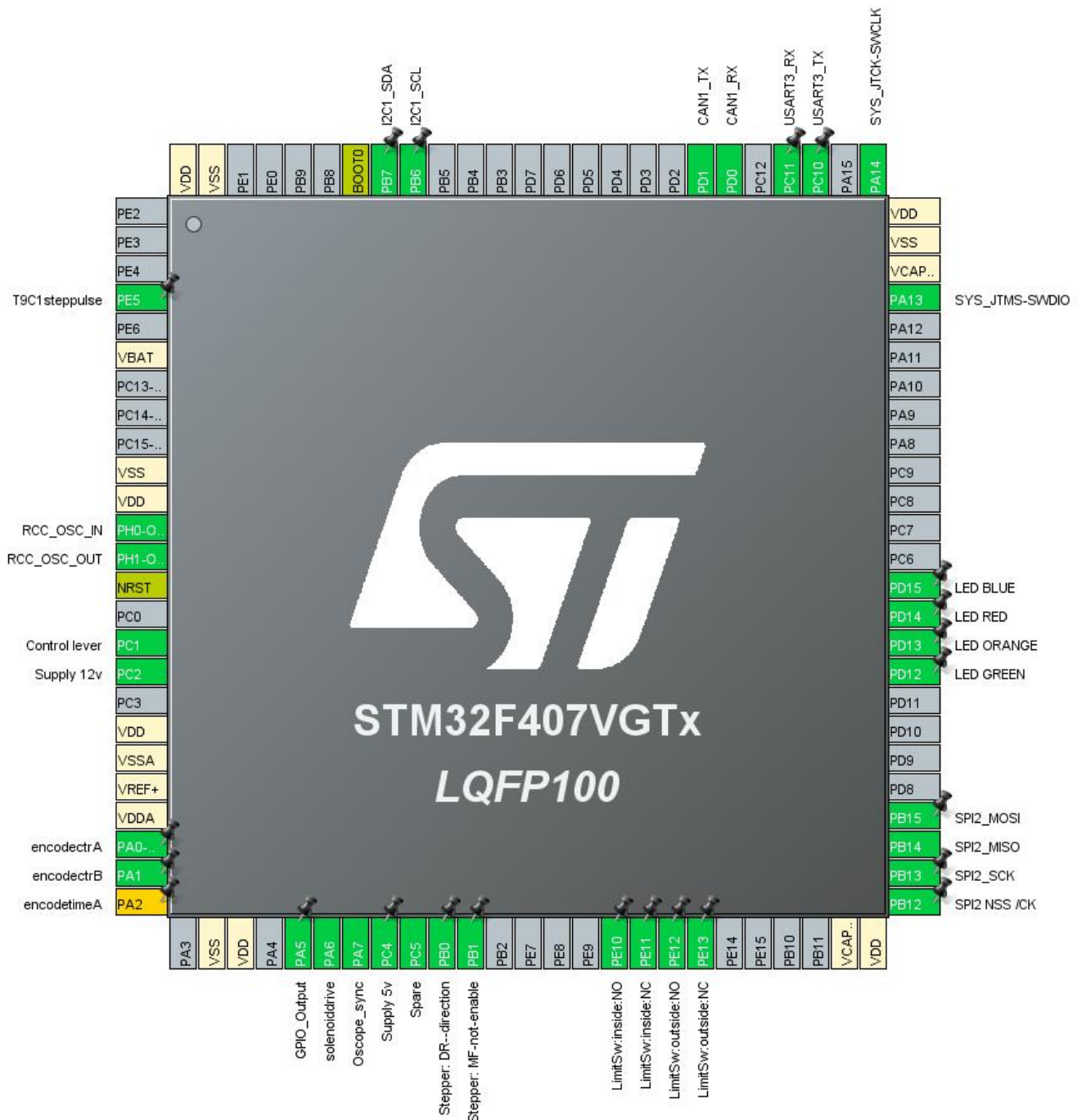
### 1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VGTx
MCU Package	LQFP100
MCU Pin number	100

### 1.3. Core(s) information

Core(s)	Arm Cortex-M4
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## 2. Pinout Configuration



### 3. Pins Configuration

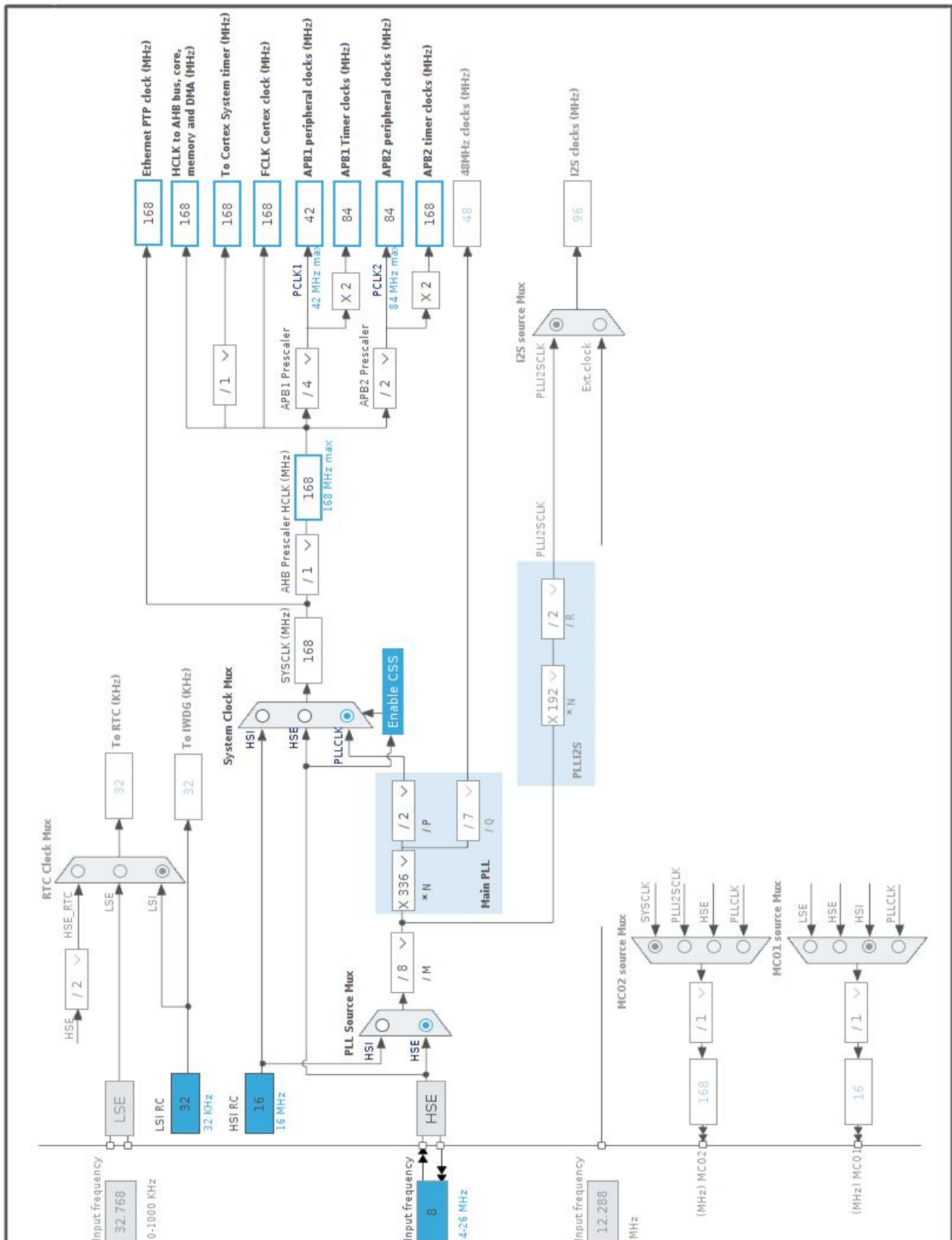
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
4	PE5	I/O	TIM9_CH1	T9C1steppulse
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
16	PC1	I/O	ADC1_IN11	Control lever
17	PC2	I/O	ADC1_IN12	Supply 12v
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	TIM5_CH1	encodectrA
24	PA1	I/O	TIM5_CH2	encodectrB
25	PA2 *	I/O	TIM2_CH3	encodetimeA
27	VSS	Power		
28	VDD	Power		
30	PA5 **	I/O	GPIO_Output	
31	PA6	I/O	TIM13_CH1	solenoiddrive
32	PA7	I/O	TIM14_CH1	Oscope_sync
33	PC4	I/O	ADC1_IN14	Supply 5v
34	PC5	I/O	ADC1_IN15	Spare
35	PB0 **	I/O	GPIO_Output	Stepper: DR--direction
36	PB1 **	I/O	GPIO_Output	Stepper: MF-not-enable
41	PE10	I/O	GPIO_EXTI10	LimitSw:inside:NO
42	PE11	I/O	GPIO_EXTI11	LimitSw:inside:NC
43	PE12	I/O	GPIO_EXTI12	LimitSw:outside:NO
44	PE13	I/O	GPIO_EXTI13	LimitSw:outside:NC
49	VCAP_1	Power		
50	VDD	Power		
51	PB12 **	I/O	GPIO_Output	SPI2 NSS /CK
52	PB13	I/O	SPI2_SCK	
53	PB14	I/O	SPI2_MISO	
54	PB15	I/O	SPI2_MOSI	
59	PD12 **	I/O	GPIO_Output	LED GREEN

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
60	PD13 **	I/O	GPIO_Output	LED ORANGE
61	PD14 **	I/O	GPIO_Output	LED RED
62	PD15 **	I/O	GPIO_Output	LED BLUE
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
78	PC10	I/O	USART3_TX	
79	PC11	I/O	USART3_RX	
81	PD0	I/O	CAN1_RX	
82	PD1	I/O	CAN1_TX	
92	PB6	I/O	I2C1_SCL	
93	PB7	I/O	I2C1_SDA	
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

\*\* The pin is affected with an I/O function

\* The pin is affected with a peripheral function but no peripheral mode is activated

## 4. Clock Tree Configuration



## 5. Software Project

### 5.1. Project Settings

Name	Value
Project Name	drum
Project Folder	/home/deh/GliderWinchItems/drum
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_F4 V1.25.0
Application Structure	Basic
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	IP Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_CAN1_Init	CAN1
5	MX_ADC1_Init	ADC1
6	MX_SPI2_Init	SPI2
7	MX_USART3_UART_Init	USART3
8	MX_I2C1_Init	I2C1
9	MX_TIM2_Init	TIM2
10	MX_TIM5_Init	TIM5
11	MX_TIM9_Init	TIM9

Rank	Function Name	IP Instance Name
12	MX_TIM4_Init	TIM4
13	MX_TIM13_Init	TIM13
14	MX_TIM14_Init	TIM14



## 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407VGTx
Datasheet	DS8626_Rev8

### 6.2. Parameter Selection

Temperature	25
Vdd	3.3

### 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

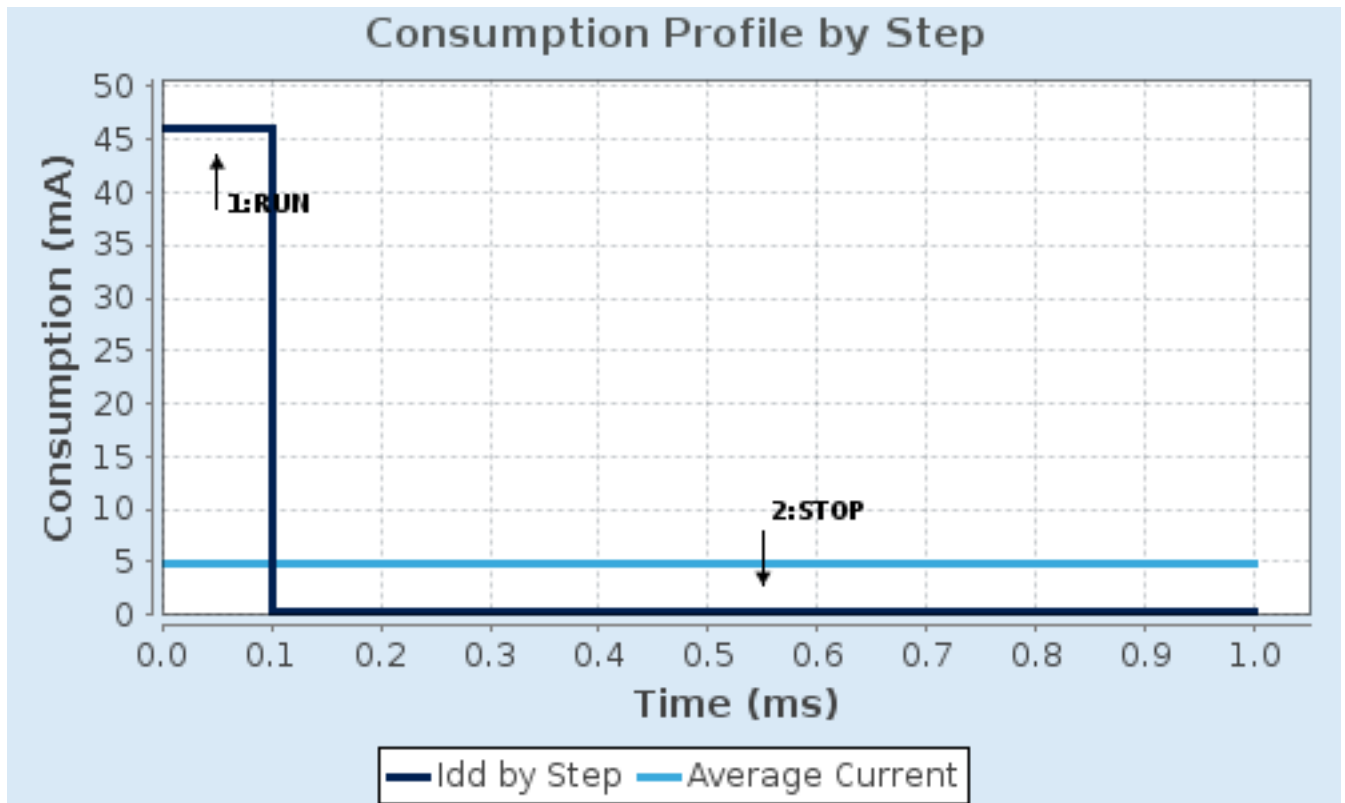
## 6.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.3	3.3
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	Scale1-High	No Scale
<b>Fetch Type</b>	FLASH	n/a
<b>CPU Frequency</b>	168 MHz	0 Hz
<b>Clock Configuration</b>	HSE PLL	Regulator LP Flash-PwrDwn
<b>Clock Source Frequency</b>	4 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	46 mA	280 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	210.0	0.0
<b>Ta Max</b>	98.47	104.96
<b>Category</b>	In DS Table	In DS Table

## 6.5. Results

Sequence Time	1 ms	Average Current	4.85 mA
Battery Life	29 days, 4 hours	Average DMIPS	210.0 DMIPS

## 6.6. Chart



## 7. IPs and Middleware Configuration

### 7.1. ADC1

mode: IN11

mode: IN12

mode: IN14

mode: IN15

mode: Temperature Sensor Channel

mode: Vrefint Channel

#### 7.1.1. Parameter Settings:

##### ADCs\_Common\_Settings:

Mode Independent mode

##### ADC\_Settings:

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode Enabled

Continuous Conversion Mode **Enabled \***

Discontinuous Conversion Mode Disabled

DMA Continuous Requests **Enabled \***

End Of Conversion Selection EOC flag at the end of single channel conversion

##### ADC\_Regular\_ConversionMode:

Number Of Conversion **6 \***

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel Channel 11

Sampling Time **84 Cycles \***

Rank **2 \***

Channel **Channel 12 \***

Sampling Time **84 Cycles \***

Rank **3 \***

Channel **Channel 14 \***

Sampling Time **84 Cycles \***

Rank **4 \***

Channel **Channel 15 \***

Sampling Time **84 Cycles \***

<u>Rank</u>	5 *
Channel	Channel Temperature Sensor *
Sampling Time	480 Cycles *
<u>Rank</u>	6 *
Channel	Channel Vrefint *
Sampling Time	480 Cycles *
<b>ADC_Injected_ConversionMode:</b>	
Number Of Conversions	0
<b>WatchDog:</b>	
Enable Analog WatchDog Mode	false

## 7.2. CAN1

### mode: Mode

#### 7.2.1. Parameter Settings:

##### **Bit Timings Parameters:**

Prescaler (for Time Quantum)	12 *
Time Quantum	285.7142857142857 *
Time Quanta in Bit Segment 1	5 Times *
Time Quanta in Bit Segment 2	1 Time
ReSynchronization Jump Width	1 Time

##### **Basic Parameters:**

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

##### **Advanced Parameters:**

Operating Mode	Normal
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## 7.3. GPIO

## 7.4. I2C1

### I2C: I2C

#### 7.4.1. Parameter Settings:

##### **Master Features:**

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

##### **Slave Features:**

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

### **7.5. RCC**

#### **High Speed Clock (HSE): Crystal/Ceramic Resonator**

#### 7.5.1. Parameter Settings:

##### **System Parameters:**

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

##### **RCC Parameters:**

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

##### **Power Parameters:**

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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### **7.6. SPI2**

#### **Mode: Full-Duplex Master**

#### 7.6.1. Parameter Settings:

##### **Basic Parameters:**

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

**Clock Parameters:**

Prescaler (for Baud Rate)	256 *
Baud Rate	164.062 KBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

**Advanced Parameters:**

CRC Calculation	Disabled
NSS Signal Type	Software

**7.7. SYS**

**Debug: Serial Wire**

**Timebase Source: TIM12**

**7.8. TIM2**

**Channel2: Output Compare No Output**

**Channel3: Output Compare No Output**

**Channel4: Output Compare No Output**

**7.8.1. Parameter Settings:****Counter Settings:**

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value )	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

**Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

**Output Compare No Output Channel 2:**

Mode	Frozen (used for Timing base)
Pulse (32 bits value)	0
Output compare preload	Disable
CH Polarity	High

**Output Compare No Output Channel 3:**

Mode	Frozen (used for Timing base)
Pulse (32 bits value)	0
Output compare preload	Disable
CH Polarity	High

#### Output Compare No Output Channel 4:

Mode	Frozen (used for Timing base)
Pulse (32 bits value)	0
Output compare preload	Disable
CH Polarity	High

## 7.9. TIM4

**Clock Source : Internal Clock**

**Channel1: Output Compare No Output**

**Channel2: Output Compare No Output**

### 7.9.1. Parameter Settings:

#### Counter Settings:

Prescaler (PSC - 16 bits value)	<b>840 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

#### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

#### Output Compare No Output Channel 1:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High

#### Output Compare No Output Channel 2:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High

## 7.10. TIM5

**Combined Channels: Encoder Mode**

### 7.10.1. Parameter Settings:

#### Counter Settings:



Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value )	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

#### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

#### Encoder:

Encoder Mode	Encoder Mode TI1
_____ Parameters for Channel 1 _____	

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

\_\_\_\_\_ Parameters for Channel 2 \_\_\_\_\_

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

## 7.11. TIM9

**mode: Clock Source**

**Channel1: PWM Generation CH1**

**mode: One Pulse Mode**

### 7.11.1. Parameter Settings:

#### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>1680 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

#### PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	<b>504 *</b>
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

## 7.12. TIM13

**mode: Activated**

**Channel1: PWM Generation CH1**

### 7.12.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>21000 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

#### **PWM Generation Channel 1:**

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

## 7.13. TIM14

**mode: Activated**

**Channel1: PWM Generation CH1**

**mode: One Pulse Mode**

### 7.13.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>840 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

#### **PWM Generation Channel 1:**

Mode	PWM mode 1
Pulse (16 bits value)	<b>420 *</b>
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

## 7.14. USART3

### Mode: Asynchronous

#### 7.14.1. Parameter Settings:

##### Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

##### Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

## 7.15. FREERTOS

### Interface: CMSIS\_V1

#### 7.15.1. Config parameters:

##### API:

FreeRTOS API	CMSIS v1
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##### Versions:

FreeRTOS version	10.2.1
CMSIS-RTOS version	1.02

##### MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

##### Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	<b>512 *</b>
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	<b>96 *</b>
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled

USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	<b>12 *</b>
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

#### Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	<b>32768 *</b>
Memory Management scheme	heap_4

#### Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	<b>Option2 *</b>

#### Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

#### Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

#### Software timer definitions:

USE_TIMERS	<b>Enabled *</b>
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	192

#### Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

#### Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

### 7.15.2. Include parameters:

#### Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	<b>Disabled *</b>
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	<b>Enabled *</b>
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	<b>Enabled *</b>
xTaskGetCurrentTaskHandle	<b>Enabled *</b>
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

### 7.15.3. Advanced settings:

#### **Newlib settings (see parameter description first):**

USE\_NEWLIB\_REENTRANT                      Disabled

#### **Project settings (see parameter description first):**

Use FW pack heap file                      Enabled

**\* User modified value**

## 8. System Configuration

### 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC1	ADC1_IN11	Analog mode	No pull-up and no pull-down	n/a	Control lever
	PC2	ADC1_IN12	Analog mode	No pull-up and no pull-down	n/a	Supply 12v
	PC4	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	Supply 5v
	PC5	ADC1_IN15	Analog mode	No pull-up and no pull-down	n/a	Spare
CAN1	PD0	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PD1	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	Very High *	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	Very High *	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI2	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM5	PA0-WKUP	TIM5_CH1	Alternate Function Push Pull	Pull-up *	Low	encodectrA
	PA1	TIM5_CH2	Alternate Function Push Pull	Pull-up *	Low	encodectrB
TIM9	PE5	TIM9_CH1	Alternate Function Push Pull	Pull-up *	Very High *	T9C1steppulse
TIM13	PA6	TIM13_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	solenoiddrive
TIM14	PA7	TIM14_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	Oscope_sync
USART3	PC10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down		

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					<b>Very High</b> *	
	PC11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
Single Mapped Signals	PA2	TIM2_CH3	Alternate Function Push Pull	<b>Pull-up</b> *	Low	encodetimeA
GPIO	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>Medium</b> *	Stepper: DR--direction
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Stepper: MF-not-enable
	PE10	GPIO_EXTI10	External Interrupt Mode with Rising edge trigger detection	<b>Pull-up</b> *	n/a	LimitSw:inside:NO
	PE11	GPIO_EXTI11	External Interrupt Mode with Rising edge trigger detection	<b>Pull-up</b> *	n/a	LimitSw:inside:NC
	PE12	GPIO_EXTI12	External Interrupt Mode with Rising edge trigger detection	<b>Pull-up</b> *	n/a	LimitSw:outside:NO
	PE13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	<b>Pull-up</b> *	n/a	LimitSw:outside:NC
	PB12	GPIO_Output	Output Push Pull	<b>Pull-up</b> *	<b>Medium</b> *	SPI2 NSS /CK
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED GREEN
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED ORANGE
	PD14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED RED
	PD15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED BLUE

## 8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Low
USART3_RX	DMA1_Stream1	Peripheral To Memory	Low
USART3_TX	DMA1_Stream3	Memory To Peripheral	Low
I2C1_TX	DMA1_Stream7	Memory To Peripheral	Low
I2C1_RX	DMA1_Stream0	Peripheral To Memory	Low

### ADC1: DMA2\_Stream0 DMA request Settings:

Mode: **Circular \***  
 Use fifo: Disable  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: Half Word  
 Memory Data Width: Half Word

### USART3\_RX: DMA1\_Stream1 DMA request Settings:

Mode: Normal  
 Use fifo: Disable  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: Byte  
 Memory Data Width: Byte

### USART3\_TX: DMA1\_Stream3 DMA request Settings:

Mode: Normal  
 Use fifo: Disable  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: Byte  
 Memory Data Width: Byte

### I2C1\_TX: DMA1\_Stream7 DMA request Settings:

Mode: Normal



Use fifo: Disable  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

*I2C1\_RX: DMA1\_Stream0 DMA request Settings:*

Mode: Normal  
Use fifo: Disable  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

### 8.3. NVIC configuration

#### 8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 stream0 global interrupt	true	8	0
DMA1 stream1 global interrupt	true	10	0
DMA1 stream3 global interrupt	true	10	0
ADC1, ADC2 and ADC3 global interrupts	true	6	0
CAN1 TX interrupts	true	7	0
CAN1 RX0 interrupts	true	7	0
CAN1 RX1 interrupt	true	7	0
TIM1 break interrupt and TIM9 global interrupt	true	6	0
TIM2 global interrupt	true	2	0
TIM4 global interrupt	true	2	0
I2C1 event interrupt	true	10	0
SPI2 global interrupt	true	13	0
USART3 global interrupt	true	8	0
EXTI line[15:10] interrupts	true	11	0
TIM8 break interrupt and TIM12 global interrupt	true	0	0
DMA1 stream7 global interrupt	true	12	0
DMA2 stream0 global interrupt	true	6	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
CAN1 SCE interrupt	unused		
I2C1 error interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM5 global interrupt	unused		
FPU global interrupt	unused		

### 8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	true	true	false
Hard fault interrupt	true	true	false
Memory management fault	true	true	false
Pre-fetch fault, memory access fault	true	true	false
Undefined instruction or illegal state	true	true	false
System service call via SWI instruction	true	false	false
Debug monitor	true	true	false
Pendable request for system service	true	false	false
System tick timer	true	false	false
DMA1 stream0 global interrupt	true	true	true
DMA1 stream1 global interrupt	true	true	true
DMA1 stream3 global interrupt	true	true	true
ADC1, ADC2 and ADC3 global interrupts	true	true	true
CAN1 TX interrupts	true	true	true
CAN1 RX0 interrupts	true	true	true
CAN1 RX1 interrupt	true	true	true
TIM1 break interrupt and TIM9 global interrupt	true	true	true
TIM2 global interrupt	true	true	true
TIM4 global interrupt	true	true	true
I2C1 event interrupt	true	true	true
SPI2 global interrupt	true	true	true
USART3 global interrupt	true	true	true
EXTI line[15:10] interrupts	true	true	true
TIM8 break interrupt and TIM12 global interrupt	true	true	true
DMA1 stream7 global interrupt	true	true	true
DMA2 stream0 global interrupt	true	true	true

\* User modified value

## 9. System Views

### 9.1. Category view

#### 9.1.1. Current

Middleware						
FREERTOS ✓						
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA ✓	ADC1 ✓	TIM2 ✓	CAN1 ✓			
GPIO ⚠		TIM4 ✓	I2C1 ✓			
NVIC ✓		TIM5 ✓	SPI2 ✓			
RCC ✓		TIM9 ✓	USART3 ✓			
SYS ✓		TIM13 ✓				
		TIM14 ✓				

## 10. Software Pack Report

### 10.1. Software Pack selected

Vendor	Name	Version	Component
STMicroelectronics	FreeRTOS	0.0.1	Class : CMSIS Group : RTOS SubGroup : FreeRTOS Version : 10.2.0 Class : RTOS Group : Core Version : 10.2.0

## 11. Docs & Resources

Type	Link
Datasheet	<a href="http://www.st.com/resource/en/datasheet/DM00037051.pdf">http://www.st.com/resource/en/datasheet/DM00037051.pdf</a>
Reference manual	<a href="http://www.st.com/resource/en/reference_manual/DM00031020.pdf">http://www.st.com/resource/en/reference_manual/DM00031020.pdf</a>
Programming manual	<a href="http://www.st.com/resource/en/programming_manual/DM00046982.pdf">http://www.st.com/resource/en/programming_manual/DM00046982.pdf</a>
Errata sheet	<a href="http://www.st.com/resource/en/errata_sheet/DM00037591.pdf">http://www.st.com/resource/en/errata_sheet/DM00037591.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00167594.pdf">http://www.st.com/resource/en/application_note/CD00167594.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00211314.pdf">http://www.st.com/resource/en/application_note/CD00211314.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00249778.pdf">http://www.st.com/resource/en/application_note/CD00249778.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00259245.pdf">http://www.st.com/resource/en/application_note/CD00259245.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264321.pdf">http://www.st.com/resource/en/application_note/CD00264321.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264342.pdf">http://www.st.com/resource/en/application_note/CD00264342.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264379.pdf">http://www.st.com/resource/en/application_note/CD00264379.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00024853.pdf">http://www.st.com/resource/en/application_note/DM00024853.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00025071.pdf">http://www.st.com/resource/en/application_note/DM00025071.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00040802.pdf">http://www.st.com/resource/en/application_note/DM00040802.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00040808.pdf">http://www.st.com/resource/en/application_note/DM00040808.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00042534.pdf">http://www.st.com/resource/en/application_note/DM00042534.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00046011.pdf">http://www.st.com/resource/en/application_note/DM00046011.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00050879.pdf">http://www.st.com/resource/en/application_note/DM00050879.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00072315.pdf">http://www.st.com/resource/en/application_note/DM00072315.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00073742.pdf">http://www.st.com/resource/en/application_note/DM00073742.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00073853.pdf">http://www.st.com/resource/en/application_note/DM00073853.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00080497.pdf">http://www.st.com/resource/en/application_note/DM00080497.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00081379.pdf">http://www.st.com/resource/en/application_note/DM00081379.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00115714.pdf">http://www.st.com/resource/en/application_note/DM00115714.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00123028.pdf">http://www.st.com/resource/en/application_note/DM00123028.pdf</a>

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