
STM32
CubeMX

1. Description

1.1. Project

Project Name	drum
Board Name	custom
Generated with:	STM32CubeMX 6.1.0
Date	02/05/2021

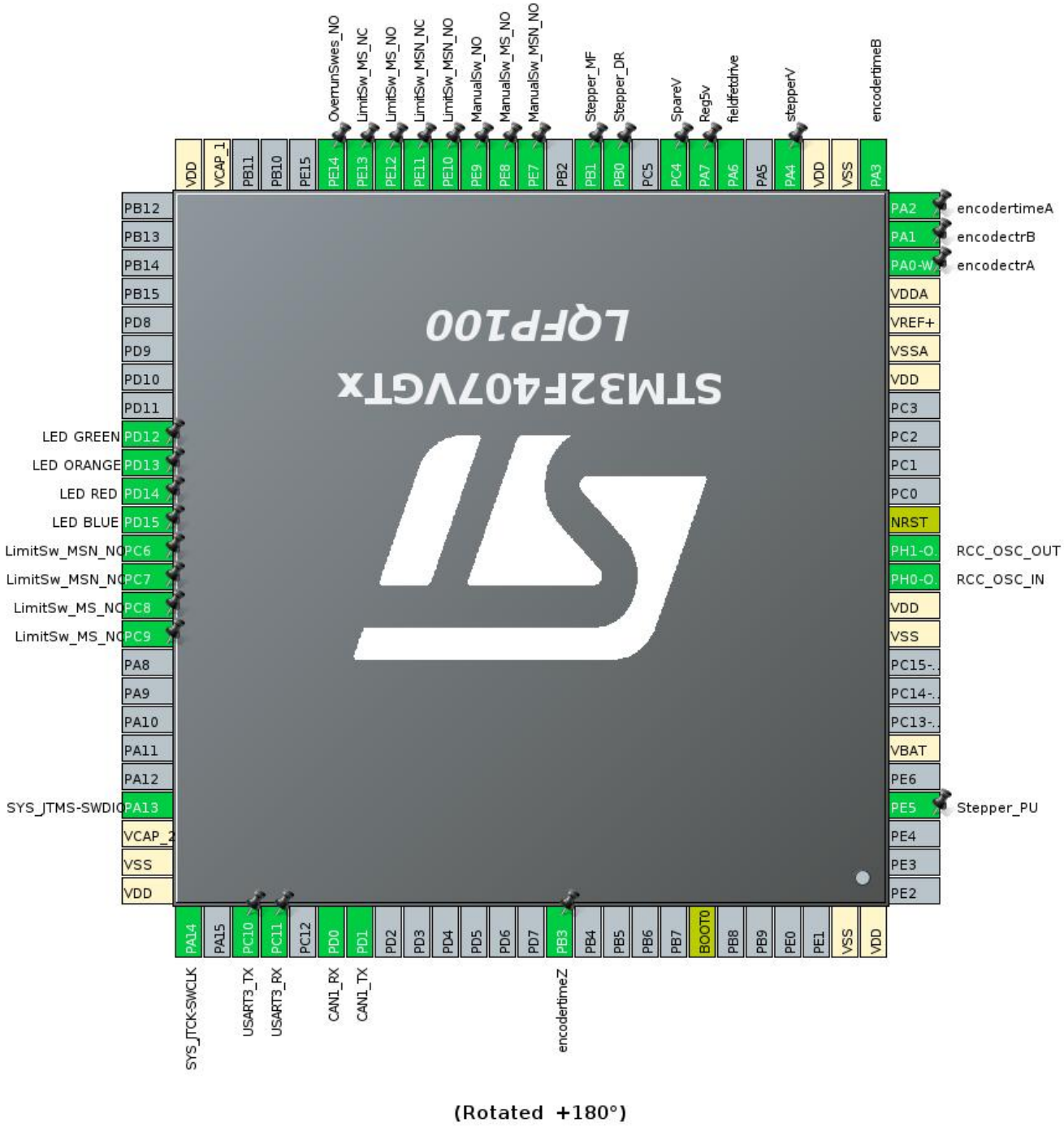
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VGTx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



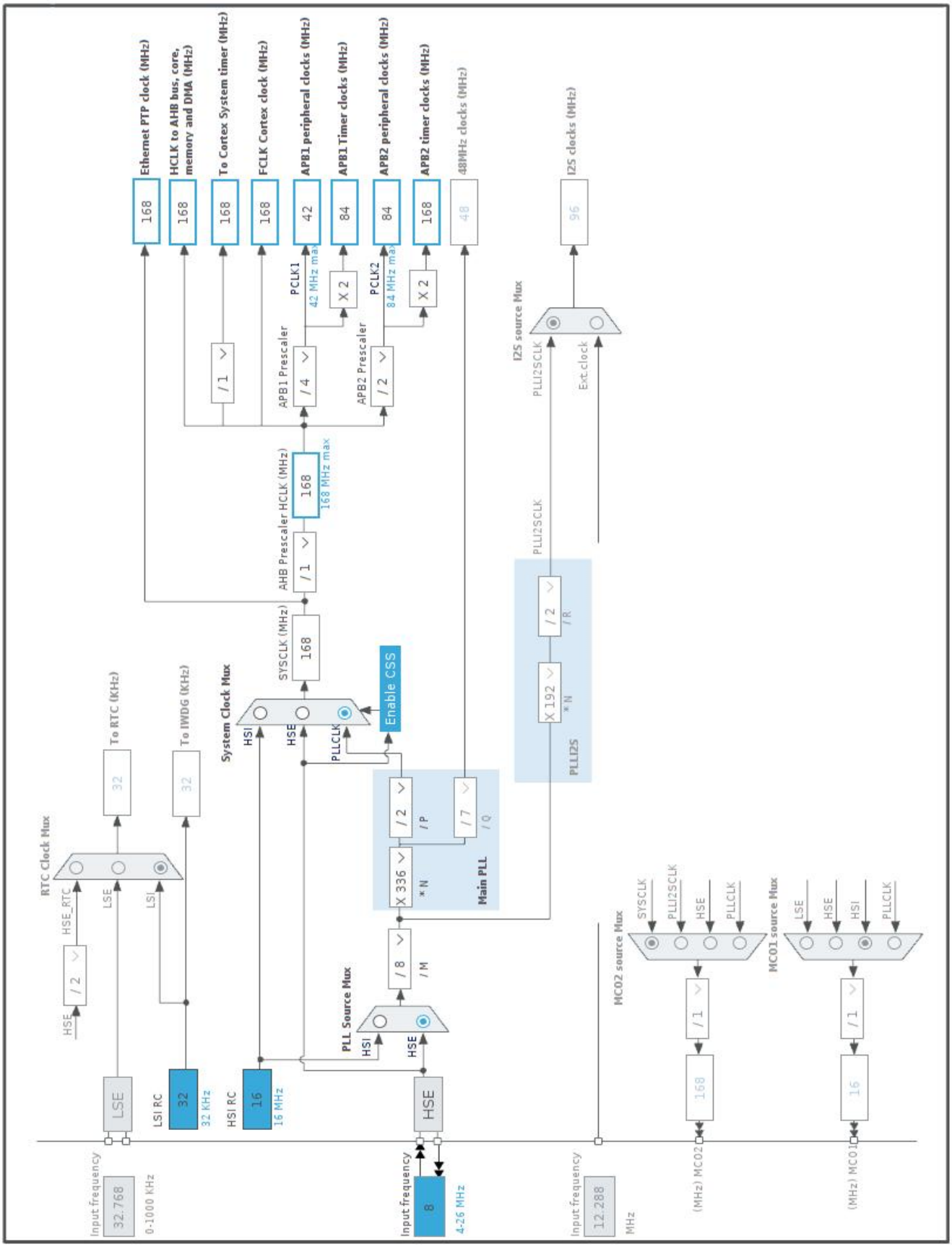
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
4	PE5	I/O	TIM9_CH1	Stepper_PU
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	TIM5_CH1	encodectrA
24	PA1	I/O	TIM5_CH2	encodectrB
25	PA2	I/O	TIM2_CH3	encodertimeA
26	PA3	I/O	TIM2_CH4	encodertimeB
27	VSS	Power		
28	VDD	Power		
29	PA4	I/O	ADC1_IN4	stepperV
31	PA6	I/O	TIM13_CH1	fieldfetdrive
32	PA7	I/O	ADC1_IN7	Reg5v
33	PC4	I/O	ADC1_IN14	SpareV
35	PB0 *	I/O	GPIO_Output	Stepper_DR
36	PB1 *	I/O	GPIO_Output	Stepper_MF
38	PE7 *	I/O	GPIO_Input	ManualSw_MSN_NO
39	PE8 *	I/O	GPIO_Input	ManualSw_MS_NO
40	PE9 *	I/O	GPIO_Input	ManualSw_NO
41	PE10	I/O	GPIO_EXTI10	LimitSw_MSN_NO
42	PE11	I/O	GPIO_EXTI11	LimitSw_MSN_NC
43	PE12	I/O	GPIO_EXTI12	LimitSw_MS_NO
44	PE13	I/O	GPIO_EXTI13	LimitSw_MS_NC
45	PE14 *	I/O	GPIO_Input	OverrunSwes_NO
49	VCAP_1	Power		
50	VDD	Power		
59	PD12 *	I/O	GPIO_Output	LED GREEN
60	PD13 *	I/O	GPIO_Output	LED ORANGE
61	PD14 *	I/O	GPIO_Output	LED RED

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
62	PD15 *	I/O	GPIO_Output	LED BLUE
63	PC6	I/O	TIM3_CH1	LimitSw_MSN_NO
64	PC7	I/O	TIM3_CH2	LimitSw_MSN_NC
65	PC8	I/O	TIM3_CH3	LimitSw_MS_NO
66	PC9	I/O	TIM3_CH4	LimitSw_MS_NC
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
78	PC10	I/O	USART3_TX	
79	PC11	I/O	USART3_RX	
81	PD0	I/O	CAN1_RX	
82	PD1	I/O	CAN1_TX	
89	PB3	I/O	TIM2_CH2	encodertimeZ
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	drum
Project Folder	/home/gsm/GliderWinchItems/drum
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_F4 V1.25.2
Application Structure	Basic
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_CAN1_Init	CAN1
5	MX_USART3_UART_Init	USART3
6	MX_TIM2_Init	TIM2
7	MX_TIM5_Init	TIM5
8	MX_TIM9_Init	TIM9
9	MX_TIM13_Init	TIM13
10	MX_TIM3_Init	TIM3
11	MX_ADC1_Init	ADC1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407VGTx
Datasheet	DS8626_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

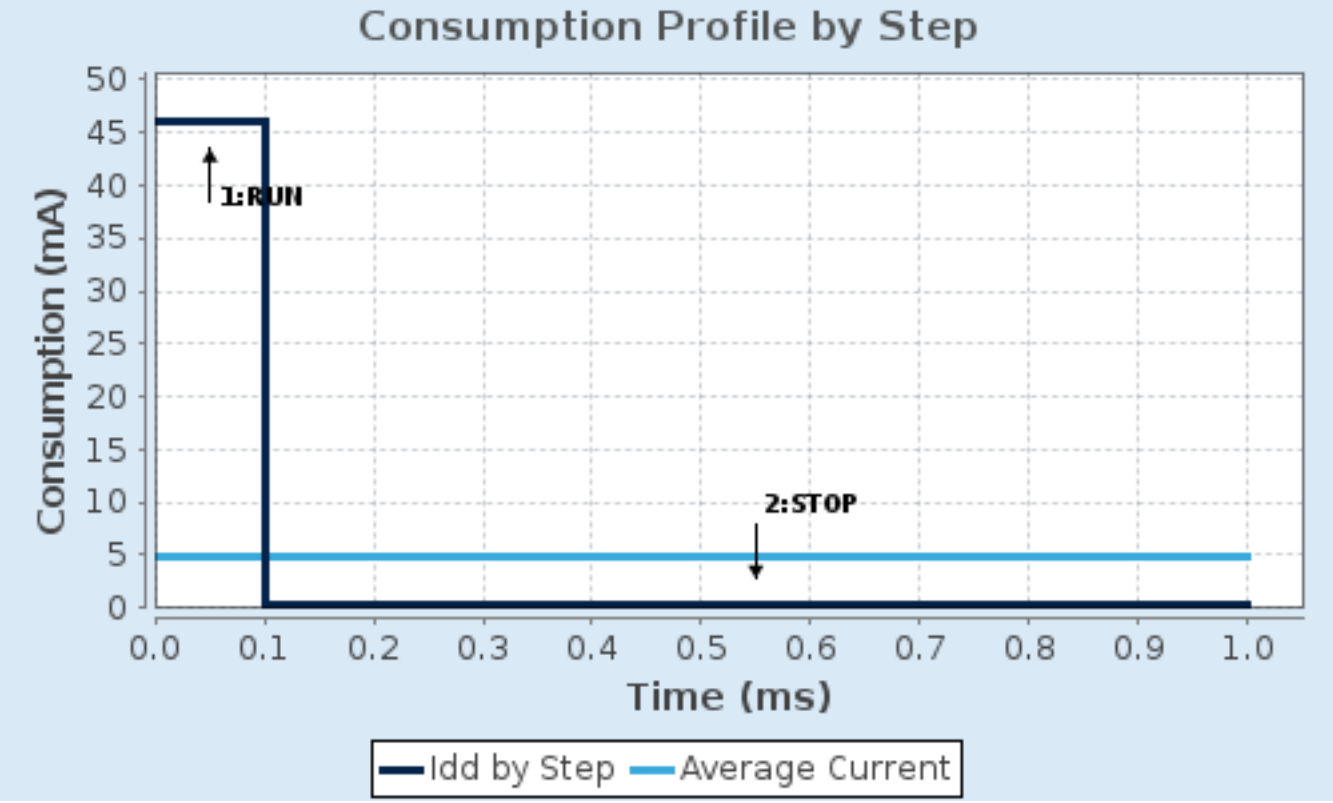
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	168 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	280 µA
Duration	0.1 ms	0.9 ms
DMIPS	210.0	0.0
Ta Max	98.47	104.96
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	4.85 mA
Battery Life	29 days, 4 hours	Average DMIPS	210.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
50
45
40
35
30
25
20
15
10
5
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN4

mode: IN7

mode: IN14

mode: Temperature Sensor Channel

mode: Vrefint Channel

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	**5 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 4
Sampling Time	**480 Cycles ***
Rank	**2 ***
Channel	**Channel 7 ***
Sampling Time	**480 Cycles ***
Rank	**3 ***
Channel	**Channel 14 ***
Sampling Time	**480 Cycles ***
Rank	**4 ***
Channel	**Channel Temperature Sensor ***
Sampling Time	**480 Cycles ***
Rank	**5 ***

Channel	**Channel Vrefint ***
Sampling Time	**480 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. CAN1

mode: Activated

7.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**12 ***
Time Quantum	**285.7142857142857 ***
Time Quanta in Bit Segment 1	**5 Times ***
Time Quanta in Bit Segment 2	1 Time
Time for one Bit	**1999.99 ***
Baud Rate	**500000 ***
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled

Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.4. SYS

Debug: Serial Wire

Timebase Source: TIM12

7.5. TIM2

Channel1: Output Compare No Output

Channel2: Input Capture direct mode

Channel3: Input Capture direct mode

Channel4: Input Capture direct mode

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Output Compare No Output Channel 1:

Mode	Frozen (used for Timing base)
Pulse (32 bits value)	0
Output compare preload	Disable
CH Polarity	High

Input Capture Channel 2:

Polarity Selection	**Both Edges ***
IC Selection	Direct

Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 3:

Polarity Selection	**Both Edges ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 4:

Polarity Selection	**Both Edges ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.6. TIM3

Clock Source : Internal Clock

Channel1: Input Capture direct mode

Channel2: Input Capture direct mode

Channel3: Input Capture direct mode

Channel4: Input Capture direct mode

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	**15 ***

Input Capture Channel 2:

Polarity Selection	**Falling Edge ***
IC Selection	Direct

Prescaler Division Ratio	No division
Input Filter (4 bits value)	**15 ***

Input Capture Channel 3:

Polarity Selection	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	**15 ***

Input Capture Channel 4:

Polarity Selection	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	**15 ***

7.7. TIM5

Combined Channels: Encoder Mode

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.8. TIM9

mode: Clock Source

Channel1: PWM Generation CH1

mode: One Pulse Mode

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1680 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**504 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.9. TIM13

mode: Activated

Channel1: PWM Generation CH1

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**21000 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.10. USART3

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.11. FREERTOS

Interface: CMSIS_V1

7.11.1. Config parameters:

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	10.2.1
CMSIS-RTOS version	1.02

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	**512 ***
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	**96 ***
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled

USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	**12 ***
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	**32768 ***
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	**Option2 ***

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	**Enabled ***
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	192

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

7.11.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	**Disabled ***
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	**Enabled ***
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	**Enabled ***
xTaskGetCurrentTaskHandle	**Enabled ***
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

7.11.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	Disabled

Project settings (see parameter description first):

Use FW pack heap file	Enabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	stepperV
	PA7	ADC1_IN7	Analog mode	No pull-up and no pull-down	n/a	Reg5v
	PC4	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	SpareV
CAN1	PD0	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD1	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM2	PA2	TIM2_CH3	**Alternate Function Open Drain ***	**Pull-up ***	Low	encodertimeA
	PA3	TIM2_CH4	**Alternate Function Open Drain ***	**Pull-up ***	Low	encodertimeB
	PB3	TIM2_CH2	**Alternate Function Open Drain ***	**Pull-up ***	Low	encodertimeZ
TIM3	PC6	TIM3_CH1	Alternate Function Push Pull	**Pull-up ***	Low	LimitSw_MSN_NO
	PC7	TIM3_CH2	Alternate Function Push Pull	**Pull-up ***	Low	LimitSw_MSN_NC
	PC8	TIM3_CH3	Alternate Function Push Pull	**Pull-up ***	Low	LimitSw_MS_NO
	PC9	TIM3_CH4	Alternate Function Push Pull	**Pull-up ***	Low	LimitSw_MS_NC
TIM5	PA0-WKUP	TIM5_CH1	Alternate Function Push Pull	**Pull-up ***	Low	encodectrA
	PA1	TIM5_CH2	Alternate Function Push Pull	**Pull-up ***	Low	encodectrB
TIM9	PE5	TIM9_CH1	Alternate Function Push Pull	**Pull-up ***	**Very High ***	Stepper_PU
TIM13	PA6	TIM13_CH1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	fieldfetdrive
USART3	PC10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High**	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
GPIO	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	Stepper_DR
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Stepper_MF
	PE7	GPIO_Input	Input mode	**Pull-up ***	n/a	ManualSw_MSN_NO
	PE8	GPIO_Input	Input mode	**Pull-up ***	n/a	ManualSw_MS_NO
	PE9	GPIO_Input	Input mode	**Pull-up ***	n/a	ManualSw_NO
	PE10	GPIO_EXTI10	**External Interrupt Mode with Falling edge trigger detection**	**Pull-up ***	n/a	LimitSw_MSN_NO
	PE11	GPIO_EXTI11	**External Interrupt Mode with Falling edge trigger detection**	**Pull-up ***	n/a	LimitSw_MSN_NC
	PE12	GPIO_EXTI12	**External Interrupt Mode with Falling edge trigger detection**	**Pull-up ***	n/a	LimitSw_MS_NO
	PE13	GPIO_EXTI13	**External Interrupt Mode with Falling edge trigger detection**	**Pull-up ***	n/a	LimitSw_MS_NC
	PE14	GPIO_Input	Input mode	**Pull-up ***	n/a	OverrunSwes_NO
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED GREEN
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED ORANGE
	PD14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED RED
	PD15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED BLUE

8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART3_RX	DMA1_Stream1	Peripheral To Memory	Low
USART3_TX	DMA1_Stream3	Memory To Peripheral	Low
ADC1	DMA2_Stream0	Peripheral To Memory	Low

USART3_RX: DMA1_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_TX: DMA1_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 stream1 global interrupt	true	10	0
DMA1 stream3 global interrupt	true	10	0
ADC1, ADC2 and ADC3 global interrupts	true	7	0
CAN1 TX interrupts	true	7	0
CAN1 RX0 interrupts	true	7	0
CAN1 RX1 interrupt	true	7	0
TIM1 break interrupt and TIM9 global interrupt	true	6	0
TIM2 global interrupt	true	2	0
USART3 global interrupt	true	8	0
EXTI line[15:10] interrupts	true	5	0
TIM8 break interrupt and TIM12 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	7	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
CAN1 SCE interrupt	unused		
TIM3 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM5 global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false

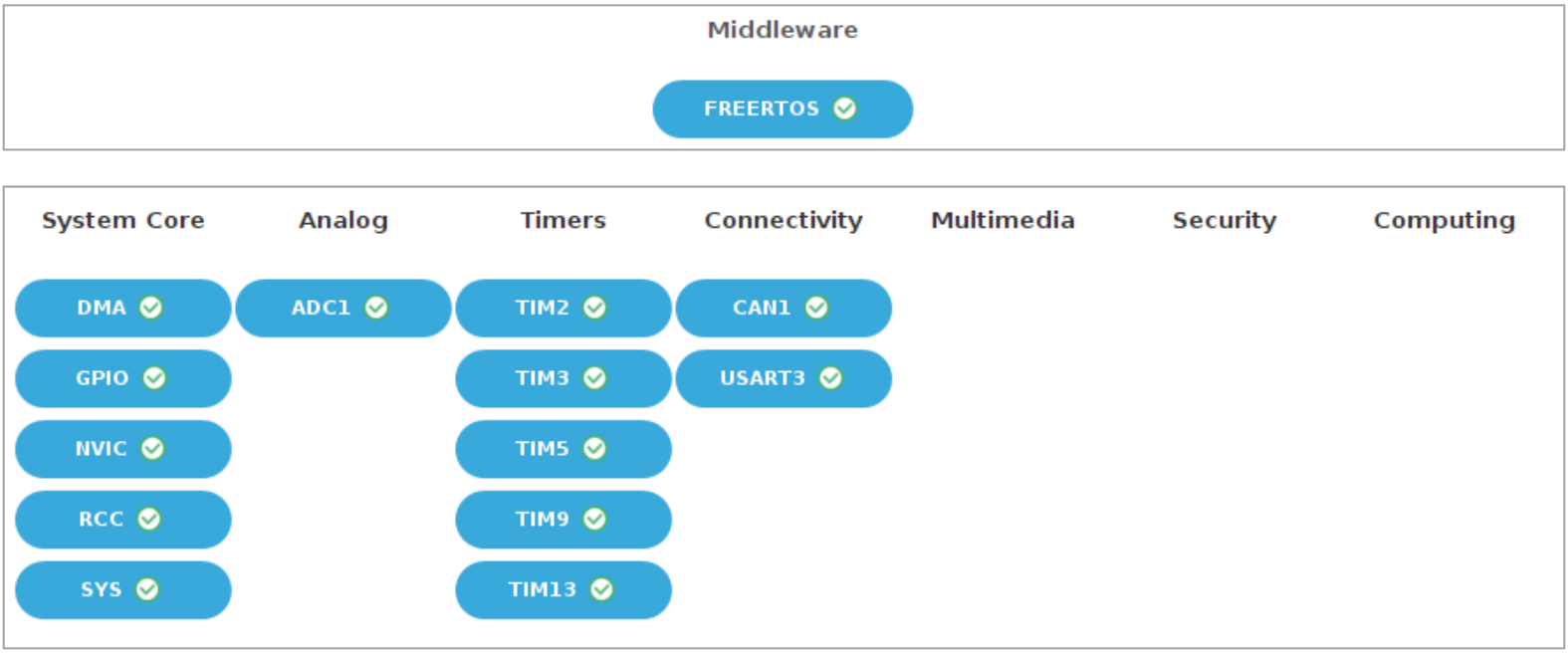
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
DMA1 stream1 global interrupt	false	true	true
DMA1 stream3 global interrupt	false	true	true
ADC1, ADC2 and ADC3 global interrupts	false	true	true
CAN1 TX interrupts	false	true	true
CAN1 RX0 interrupts	false	true	true
CAN1 RX1 interrupt	false	true	true
TIM1 break interrupt and TIM9 global interrupt	false	true	true
TIM2 global interrupt	false	true	true
USART3 global interrupt	false	true	true
EXTI line[15:10] interrupts	false	true	true
TIM8 break interrupt and TIM12 global interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00037051.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00031020.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00037591.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00025071.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040802.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040808.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00050879.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00115714.pdf
Application note	http://www.st.com/resource/en/application_note/DM00123028.pdf

Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00154959.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00213525.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00263732.pdf
Application note	http://www.st.com/resource/en/application_note/DM00281138.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00373474.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf