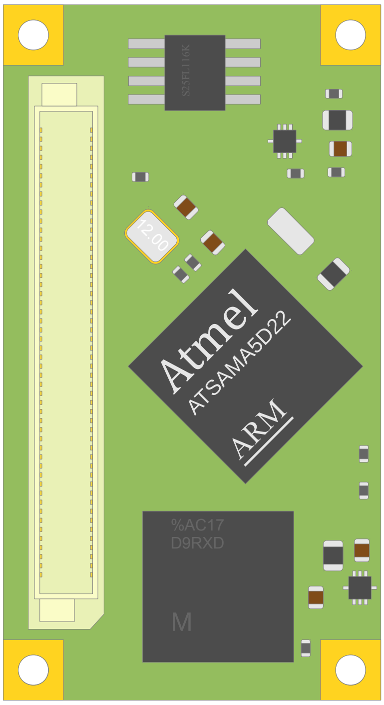

DropA5D22

Technical Reference

DropA5D22: Technical Reference

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- ARM V7-A Thumb2 Instruction Set.
- 64kB Level-1 Cache (32kB Instruction, 32kB Data)
- 128kB Level-2 Cache (available also for general use)
- Separated 16-Bit DDR-RAM Bus and 16-Bit EBI (External Bus Interface)
- Memory Management Unit (MMU)
- NEON™ Media Processing Engine, including Vector Floating Point Unit (VFPv4)
- Jazelle (direct Bytecode Execution) Java Acceleration
- ARM TrustZone® Advanced Security Functions
- Tamper Detection
- Secure Data Storage

1.2. Memory

- 64k L1 Cache (32k Data, 32k Instruction)
- 128k SRAM (L2 Cache or general use)
- 128k Scrambled SRAM
- LPDDR1 256 MB Main Memory
- Serial NOR-Flash: 2MB standard (boot device), other capacities on request
- On-board Micro SD-Card slot
- Optional: external NAND-Flash on 8-Bit EBI

1.3. Interfaces and external signals

- PIO-Controller: 72 Multi-configurable Digital I/O-Pins
- USB 2.0 High Speed (480MBit/s): 1x Host, 1x Host/Device
- 10/100MBit Ethernet MAC
- LCD Interface 24 Bit, up to 1024x768 Pixel
- Image Sensor Controller up to 5M-pixel sensors
- Serial Ports:

  Flexcom (USART) (4), configurable as: UART, SPI, I2C, LIN, RS485, SmartCard, Irda

  UART (5)

  SPI (2)

  QSPI (2)

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- PDM (Pulse Density Modulation) Microphone Input
- Audio Class-D (PWM controlled switching) Stereo Amplifier
- 6-Channel General Purpose 32-Bit Timer/Counter
- 4-Channel 16-Bit PWM-Controller
- 5-Channel ADC 12Bit resolution, 1 MS/s

1.4. Miscellaneous

- Periodic Interval Timer (PIT)
- Real Time Clock (RTC), with battery backup
- Watchdog Timer (WDT)
- Shutdown Controller (SDC)
- Hardware cryptography:

  SHA (SHA1, SHA224, SHA256, SHA384, SHA512)

  AES: 256-, 192-, 128-bit key, compliant with FIPS PUB 197

  Triple-DES: two-key or three-key, compliant with FIPS PUB 46-3

  True Random Number Generator (TRNG) compliant with NIST Special Publication 800-22 Test Suite and FIPS
- Security Module: Secure Boot, Intrusion Detection
- Hardware Identification and Configuration:

  Fuse Controller: 544 one-time-programmable fuse bits (32 for system, 512 available for user)

  Unique Hardware Serial Number 64 Bit

  Chip-ID Registers
- Ultra Low-power mode with fast wakeup capability

1.5. Power Supply

- 3.3V Power Supply
- 3.3V I/O Voltage, 1.8V Memory Voltage, 1.25V Core Voltage (internal)
- 3V backup power supply (lithium battery, or similar device)

1.6. Mechanical Characteristics

- Dimensions: 46x25x6mmm

- One 100-Pin Hirose FX8-P Connector

2. Hardware Description

2.1. Mechanics

The DropA5D3 is a versatile CPU module featuring an ARM Cortex-A5 processor and Linux as standard operating system. It is optimized for low power applications and ease of use. Although it only has one connector with only 100 external pins, its powerful peripheral multiplexer unit still makes it suited for a great number of requirements.

The DropA5D22 has one on-board MicroSD-Card slot. Its signals are also available on the FX8-connector.

2.2. SAMA5D22 Processor Core

The ATSAMA5D22 runs at 500 MHz with a memory bus frequency of 166 MHz.

Here are some of the most important features of the SAMA5D22 Cortex-A5 core:

- 64kB Level-1 Cache (32 Kbyte Data Cache, 32 Kbyte Instruction Cache, Write Buffer)
- Separated 16-Bit DDR-RAM Bus and 16-Bit EBI (External Bus Interface)
- ARM V7-A 32-bit Instruction Set, ARM Thumb 16 and 32 Bit Instruction Set
- ARM Jazelle® Technology for Java® Acceleration
- Embedded Trace "CoreSight" Macrocell, ICE/JTAG Interface, Debug Communication Channel Support
- NEON™ Media Processing Engine
- ARM TrustZone

2.3. Memory

The SAMA5D22 processor has two 16-bit external bus interfaces, one of which is dedicated to fast DRAM, the other one, EBI (External Bus Interface), for slower external devices. EBI is multiplexed with a number of PIO pins.

2.3.1. NAND Flash

The DropA5D22 does not contain on-board NAND flash. However, it is possible to use a subset of EBI (8-Bit interface, plus some control lines) to connect external NAND flash memory. Care has to be taken, as the same signals are also used for the on-board SD-Card slot, as well as the on-board serial NOR flash. Therefore, some hardware as well as software (operating system) adaptations will have to be provided in case that the SD-Card interface or the SPI0 serial NOR flash interface should still be used. As this involves a number of intricacies, such a strategy, while still possible, is not particularly recommended. An SD-Card may also be connected via SPI port (all SD-Card should provide an SPI-mode!). The data rate will be substantially lower, though.

2.3.2. LPDDR-SDRAM

The DropA5D22 is equipped with 256B LPDDR-SDRAM (Low power DDR-SDRAM). Using LPDDR RAM in self refresh mode provides an extremely low power (<1mA) standby mode while still maintaining a quick wake-up time of less than 100µs.

2.3.3. Serial Flash

The DropA5D22 has an 1MB serial NOR flash connected to SPI0_NPCS0. This is used as the boot device (level 1 boot device) in the standard configuration. In case that a different boot strategy has to be chosen, or if the SPI0 pins must be used for different purposes, it may be necessary to unmount the serial flash.

2.3.4. SRAM

The DropA5D22's microcontroller is equipped with 128 kB internal "scrambled" SRAM, as well as 128 kB level 2 cache. In case that level-2 cache is not required, this memory may also be used for general purposes. The internal SRAM can be accessed in one bus cycle and may be used for time critical sections of code or interrupt handlers.

2.4. Advanced Interrupt Controller (AIC)

The Advanced Interrupt Controller can handle up to 128 internal or external interrupt sources. The AIC integrates an 8-level priority controller. Interrupt sources can be programmed to be level sensitive or edge triggered. The polarity can be programmed for all external interrupt sources.

Moreover, all PIO lines can be used to generate a PIO interrupt. Each 32-bit PIO has one input to the AIC. The PIO lines can only generate level change interrupts, that is, positive as well as negative edges will generate an interrupt. The PIO interrupt itself (PIO to AIC line) is usually programmed to be level-sensitive. Otherwise interrupts will be lost if multiple PIO lines source an interrupt simultaneously.

On the DropA5D22, some pins ("IRQ" and "FIQ") are directly connected to the AIC. All PIO-pins can generate a PIO interrupt. The list of peripheral identifiers, which are used to program the AIC can be found in Table A.1, “Peripheral Identifiers”

2.5. Battery Backup

The following parts of the SAMA5D22 Processor can be backed-up by a battery:

- Slow Clock Oscillator
- Reset Controller
- Shutdown/Wake-Up Controller
- Real time Clock
- General Purpose Backup Registers

It is recommended to always use a backup power supply (normally a battery) in order to speed up the boot-up time.

2.6. Reset Controller (RSTC)

The embedded microcontroller has an integrated Reset Controller which samples the backup and the core voltage. The presence of a backup voltage (VDDBU) when the card is powered down speeds up the boot time of the microcontroller.

2.7. Serial Number

Every SAMA5D22 has a unique 64-bit hardware serial number which can be used by application software. The two 32-bit serial number registers are part of the "Special Function Registers" (SFR).

2.8. Peripheral Input/Output Controller (PIO)

72 programmable digital I/O ports ("PIO pins") are available on the connector of the DropA5D22. Most of these pins are multiplexed with several signals of other peripheral devices.

Each PIO pin is associated wih one 32-bit PIO controller: PIO-A, PIO-B, PIO-C, and PIO-D. In case of the SAMA5D22 processor, not all of the possible 128 bits are available (as opposed to its bigger relatives, the SAMA5D26, SAMA5D27, and SAMA5D28).

All PIO-pins of the DropA5D22 have 3.3V levels.

One Parallel Input/Output Controller(PIO) manages up to 32 programmable I/O ports. Each I/O port is associated with a bit number in the 32 bit register of the user interface. The I/O-multiplexer of the SAMA5d22 allows to select one of up to seven diffent functions for each PIO pin.

Output data can be set or reset with separate registers (no read back necessary of register bits not involved), or by using a synchronous output register (which will then affect all bits which are configured as "PIO").

The characteristics of each PIO pin can be configured individually in various ways:

- PIO enable
- Peripheral Function Select (one out of seven)
- Direction (Input/Output)
- Pull-Up Resistor 40..130kOhm (66 kOhm typ.)
- Pull-Down Resistor 40..160kOhm (77 kOhm typ.)
- Glitch Filter
- Glitch Filter Slow Clock (SLCK) or Master Clock (MCK) Select
- Open-Drain Output
- Schmitt-Trigger
- Output Drive Strength Select: 4, 20, or 32mA
- Event Detect Select (for Interrupt): Falling Edge, Rising Edge, Both Edges, Low Level, or High Level

All configurations as well as the pin status can be read back by using the appropriate status register. Multiple pins of each PIO can also be written simultaneously by using the synchronous output register.

For interrupt handling, the PIO Controllers are considered as user peripherals. This means that the PIO Controller interrupt lines are connected among the interrupt sources 2 to 128. Refer to the PIO Controller peripheral identifier Table A.1, “Peripheral Identifiers” to identify the interrupt sources dedicated to the PIO Controllers. The PIO Controller interrupt can be generated only if the PIO Controller clock is enabled.

A number of the PIO signals might be used internally on the module. Care has to be taken when accessing the PIO registers in order not to change the settings of these internal signals, otherwise a system crash is likely to happen.

On the DropA5D22, only four PIO lines are used internally: PB0, PB1, PA30, and PA31 (configured as SPI0, for the serial flash memory). If the USB device port is used, usually one extra PIO pin is required for VBus Detect. If the USB host port is used, one extra PIO pin may be used to shut down VBus of the USB port.

2.9. System Clocks

Mnemonic	**Description**	**Frequency**	**Possible Dividers/ Prescalers**	**Source**
MOSC	Main Oscillator	12 MHz		External 12MHz-Crystal
RCOSC64K	64 kHz RC-Oscillator	12 MHz		RC-Oscillator internal to CPU
RCOSC12M	12 MHz RC-Oscillator	12 MHz		RC-Oscillator internal to CPU
SOSC	Slow-Clock-Crystal-Oscillator	32kHz		External 32768Hz-Crystal
SLCK	Slow Clock	32 kHz		SOSC or RCOSC64K
MAINCK	Main Clock	12 MHz		MOSC or RCOSC12M
PLLACK	PLLA Clock	1000 MHz (typ.)		MAINCK

Mnemonic	Description	Frequency	Possible Dividers/ Prescalers	Source
PCK	Processor Clock	500 MHz (typ.)	1, 2, 4,.., 64	PLLACK, UPLLCK, MAINCK, or SLCK
MCK	Master Clock (for Peripherals)	125 MHz (typ.)	1, 2, 3, 4	PCK
DDRCK	DRAM Clock	125 MHz (typ.)		MCK
UPPLCK	USB PLL Clock	480 MHz		MOSC
AUDIOPLLCLK	Audio PLL Clock	700 Mhz max.		MOSC
CLK_AUDIO	Audio Pin Clock	11.2896 MHz, or 12.288 MHz (typ.)		AUDIOPLLCLK
USB_CLK	USB Clock	480 MHz, or 48MHz and 12MHz		UPLLCK, or PLLACK
LCD_CLK	LCD Pixel Clock	125 MHz max.	2 .. 257	MCK,or 2x MCK
LCDPWM_CLK	LCD PWM Clock (for Contrast or Brightness)	500kHz, 128Hz		MCK, or SCLK
GCLK	Generic Clock		1 .. 256	SLCK, MAINCK, PLLACK, UPLLCK, MCK, AUDIOPLLCK

Table 2.1. SAMA5D22 Clocks

Most of the on-chip peripherals of the SAMA5D22 either use MCK (master clock), or GCLK (generic clock) as their input clock. As MCK may change if the processor clock (PCK) is changed, the GCLK can be used. GCLK is configured individually (input source and 8-bit prescaler) for each peripheral. It therefore provides a very versatile means of clocking for peripherals.

2.10. Timer Counter (TC)

The DropA5D22 features two blocks of timer counters with three 32-bit counters each.

Each timer unit consists of three independent 32-bit Timer/Counter channels. The timers can be clocked be internal clock sources (GCLK, MCK/2, MCK/8, MCK/32, MCK/128), by external pins, or by outputs of other timer channels.

Each timer unit has 9 I/O pins (TIOA0/1/2, TIOB0/1/2, TCLK0/1/2) which can be used in various ways. On the SAMA5D22 processor, there is one exception, as TC1 channel 1 does not have any I/O pins, so there are no TIOA4, TIOB4, or TCLK4 pins.

A wide range of functions includes:

Frequency measurement

Event counting

Interval measurement

Delay timing

Pulse generation

Pulse Width Modulation

Up/down capabilities

Quadrature decoder

2-bit Gray up/down count for stepper motor

2.11. Periodic Interval Timer (PIT)

The PIT consists of a 20-bit counter running on MCK / 16. This counter can be preloaded with any value between 1 and 2^{20}. The counter increments until the preloaded value is reached. At this stage it rolls over and generates an interrupt. An additional 12-bit counter counts the interrupts of the 20 bit counter.

The PIT is intended for use as the operating system's scheduler interrupt.

2.12. Watchdog Timer

The watchdog timer is a 12-bit timer running at 256 Hz (Slow Clock / 128). The maximum watchdog timeout period is therefore equal to 16 seconds. If enabled, the watchdog timer asserts a hardware reset at the end of the timeout period. The application program must always reset the watchdog timer before the timeout is reached. If an application program has crashed for some reason, the watchdog timer will reset the system, thereby reproducing a well defined state once again.

The Watchdog Mode Register can be written only once. After a processor reset, the watchdog is already activated and running with the maximum timeout period. Once the watchdog has been reconfigured or deactivated by writing to the Watchdog Mode Register, only a processor reset can change its mode once again.

2.13. Real-time Clock (RTC)

The Real-time clock combines a complete time-of-day clock with alarm, a two-hundred-year Gregorian calendar and a programmable periodic interrupt. The time and calendar values are coded in BCD format.

2.14. True Random Number Generator (TRNG)

The True Random Generator (TRNG) passes the American NIST Special Publication 800-22 and the Diehard Random Tests Suites. It provides a 32-bit value every 84 clock cycles.

2.15. Peripheral DMA Controller (PDC)

The Peripheral DMA Controller (PDC) transfers data between on-chip serial peripherals and the on- and/or off-chip memories. The PDC contains unidirectional and bidirectional channels. The full-duplex peripherals feature unidirectional channels used in pairs (transmit only or receive only). The half-duplex peripherals feature one bidirectional channel. Typically full-duplex peripherals are USARTs, SPI or SSC. The MCI is a half duplex device.

The user interface of each PDC channel is integrated into the user interface of the peripheral it serves. The user interface of unidirectional channels (receive only or transmit only), contains two 32-bit memory pointers and two 16-bit counters, one set (pointer, counter) for current transfer and one set (pointer, counter) for next transfer. The bidirectional channel user interface contains four 32-bit memory pointers and four 16-bit counters. Each set (pointer, counter) is used by current transmit, next transmit, current receive and next receive.

Using the PDC removes processor overhead by reducing its intervention during the transfer. This significantly reduces the number of clock cycles required for a data transfer, which improves microcontroller performance. To launch a transfer, the peripheral triggers its associated PDC channels by using transmit and receive signals. When the programmed data is transferred, an end of transfer interrupt is generated by the peripheral itself. There are four kinds of interrupts generated by the PDC:

- End of Receive Buffer
- End of Transmit Buffer
- Receive Buffer Full
- Transmit Buffer Empty

The "End of Receive Buffer" / "End of Transmit Buffer" interrupts signify that the DMA counter has reached zero. The DMA pointer and counter register will be reloaded from the reload registers ("DMA new pointer register" and "DMA new counter register") provided that the "DMA new counter register" has a non-zero value. Otherwise a "Receive Buffer Full" or, respectively, a "Transmit Buffer Empty" interrupt is generated, and the DMA transfer terminates. Both reload registers are set to zero automatically after having been copied to the DMA pointer and counter registers.

2.16. Debug Unit (DBGU)

Any of the five UARTS of the SAMA5D22 processor can be selected to serve as the serial console for Firmware and Operating Systems. Also, the SAM-BA monitor can be configured to use the DBGU.

2.17. JTAG Unit

The JTAG unit can be used for hardware diagnostics, hardware initialization, flash memory programming, and debug purposes. The JTAG unit supports two different modes, namely the "ICE Mode", and the "Boundary Scan" mode. It is normally jumpered for "ICE Mode".

JTAG interface devices are available for the unit. However, the use of them is not within the scope of this document.

2.18. Two-wire Interface (TWI)

The TWI is also known under the expression "I^2C-Bus", which used to be subjected to licensing by Philips in the past (not any more). However, interoperability is guaranteed. The TWI supports both master or slave mode.

The TWI uses only two lines, namely serial data (SDA) and serial clock (SCL). According to the standard, the TWI clock rate is limited to 400 kHz in fast mode and 100 kHz in normal mode, but configurable baud rate generator permits the output data rate to be adapted to a wide range of core clock frequencies.

Caveat: The TWI hardware unit has been known to be error prone in various microcontrollers, which has lead operating systems like Linux to use a bit-banging driver on the same (or other) pins instead.

2.19. Multimedia Card Interface (MCI)

The DropA5D22 features a onboard Micro-SD-Card slot, which is connected to the MCI-B interface of the microcontroller. The MCI-A interface is provided for external additional use.

The MultiMedia Card Interface (MCI) supports the MultiMedia Card (MMC) Specification V3.11, the SDIO Specification V1.1 and the SD Memory Card Specification V1.0.

The MCI includes a command register, response registers, data registers, timeout counters and error detection logic that automatically handle the transmission of commands and, when required, the reception of the associated responses and data with a limited processor overhead. The MCI supports stream, block and multi-block data read and write, and is compatible with the Peripheral DMA Controller (PDC) channels, minimizing processor intervention for large buffer transfers.

The MCI operates at a rate of up to Master Clock divided by 2 and supports the interfacing of 2 slot(s). Each slot may be used to interface with a MultiMediaCard bus (up to 30 Cards) or with a SD Memory Card. Only one slot can be selected at a time (slots are multiplexed). A bit field in the SD Card Register performs this selection.

The SD Memory Card communication is based on a 9-pin interface (clock, command, four data and three power lines) and the MultiMedia Card on a 7-pin interface (clock, command, one data, three power lines and one reserved for future use). The SD Memory Card interface also supports MultiMedia Card operations. The main differences between SD and MultiMedia Cards are the initialization process and the bus topology.

2.20. USB Host Port (UHP)

The DropA5D22 integrates two USB host ports supporting speeds up to 480 MBit/s. USB Host Port A is connected directly to the transceiver, USB Host Port B is multiplexed with the USB device port. Thus, only one of these can be used at a time.

The controller is fully compliant with the Enhanced HCI(EHCI) specification. It supports both High-speed 480 Mbps and Full-speed 12 Mbps devices.

The USB Host Port (UHP) interfaces the USB with the host application. It handles Open HCI protocol (Open Host Controller Interface) as well as USB v2.0 Full-speed and Low-speed protocols.

The USB Host Port integrates a root hub and transceivers on downstream ports. It provides several high-speed half-duplex serial communication ports. Up to 127 USB devices (printer, camera, mouse, keyboard, disk, etc.) and an USB hub can be connected to the USB host in the USB "tiered star" topology.

2.21. USB Device Port (UDP)

The DropA5D22 integrates one USB device port supporting speeds up to 480 MBit/s. It is multiplexed with the USB Host Port B. Only one of these can be used at a time.

The controller is fully compliant with the Enhanced HCI(EHCI) specification. It supports both High-speed 480 Mbps and Full-speed 12 Mbps devices.

The USB Device Port (UDP) is compliant with the Universal Serial Bus (USB) V2.0 full-speed device specification. The USB device port enables the product to act as a device to other host controllers.

The USB device port can also be implemented to power on the board. One I/O line may be used by the application to check that VBUS is still available from the host. Self-powered devices may use this entry to be notified that the host has been powered off. In this case, the pullup on DP must be disabled in order to prevent feeding current to the host. The application should disconnect the transceiver, then remove the pullup.

2.22. Ethernet Interface (EMAC, GMAC)

The Ethernet interface of the DropA5D22 contains a MAC (Media Access Controllers) but not a PHY (Physical Layer Transceiver). Hence, an external "PHY" chip is required to implement an complete Ethernet port. A suitable IC is the SMSC/Microchip LAN8720A which is small, inexpensive and relatively easy to route. Please refer to the PHY's datasheet for hints on routing high speed signals.

The SAMA5D22 "GMAC" (100Mbit/s, not "G"igabit, anyway) may be used via its 4-bit MII (Media Independent Interface) or 2-bit RMII (Reduced ...). This latter is the standard interface in the usual initialization of the DropA5D22, and it is the one which fits to the LAN8720A PHY.

A sample implementation is found on the Starterkit Board.

2.23. Universal Asynchronous Receiver and Transmitter (UART)

The DropA5D22 has up to five independent UARTs.

The Universal Asynchronous Receiver Transceiver (UART) provides one full duplex universal asynchronous serial link. Data frame format is widely programmable (data length, parity, number of stop bits). The receiver implements parity error, framing error and overrun error detection. The receiver time-out enables handling variable-length frames and the transmitter timeguard facilitates communications with slow remote devices. Multidrop communications are also supported through address bit handling in reception and transmission.

The UART supports the connection to the Peripheral DMA Controller, which enables data transfers to the transmitter and from the receiver. The PDC provides chained buffer management without any intervention of the processor.

Signals of the Serial Interfaces. All UARTs/USARTs have one receiver and one transmitter data line (full duplex). Not all USARTs are implemented with full modem control lines. Furthermore the available lines depend largely on the used multiplexing. Most modem control lines can be implemented with standard digital ports.

Hardware Interrupts. There are several interrupt sources for each USART:

- Receive: RX Ready, (DMA) Buffer Full, End of Receive Buffer
- Transmit: TX Ready, (DMA) Buffer Empty, End of Transmit Buffer, Shift Register Empty
- Errors: overrun, parity, framing, and timeout errors
- Break: the receiver has detected a break condition on RXD

Please refer to the chapter about the DMA unit (PDC) for a description of the "Buffer Full" and "End of Receive / Transmit Buffer" events.

2.24. Universal Sychronous Asynchronous Receiver and Transmitter (USART, FLEXCOM)

The DropA5D22 has up to four independent USARTs.

The Universal Synchronous Asynchronous Receiver Transceiver (USART) provides one full duplex universal synchronous asynchronous serial link. Data frame format is widely programmable (data length, parity, number of stop bits) to support a maximum of standards. The receiver implements parity error, framing error and overrun error detection. The receiver time-out enables handling variable-length frames and the transmitter timeguard facilitates communications with slow remote devices. Multidrop communications are also supported through address bit handling in reception and transmission.

The USART supports the connection to the Peripheral DMA Controller, which enables data transfers to the transmitter and from the receiver. The PDC provides chained buffer management without any intervention of the processor.

Six different modes are implemented within the USARTs:

- Normal (standard RS232 mode)
- RS485
- Hardware Handshaking
- ISO7816 Protocol: T=0 or T=1
- IrDA

RS485. In RS485 operating mode the RTS pin is automatically driven high during transmit operations. If RTS is connected to the "enable" line of the RS485 driver, the driver will thus be enabled only during transmit operations.

Hardware Handshaking. The hardware handshaking feature enables an out-of-band flow control by automatic management of the pins RTS and CTS. The receive DMA channel must be active for this mode. The RTS signal is driven high if the receiver is disabled or if the DMA indicates a buffer full condition. As the RTS signal is connected to the CTS line of the connected device, its transmitter is thus prevented from sending any more characters.

ISO7816. The USARTs have an ISO7816-compatible mode which permits interfacing with smart cards and Security Access Modules (SAM). Both T=0 and T=1 protocols of the ISO7816 specification are supported.

IrDA. The USART features an infrared (IrDA) mode supplying half-duplex point-to-point wireless communication. It includes the modulator and demodulator which allows a glueless connection to the infrared transceivers. The modulator and demodulator are compliant with the IrDA specification version 1.1 and support data transfer speeds ranging from 2.4 kb/s to 115.2 kb/s.

Signals of the Serial Interfaces. All UARTs/USARTs have one receiver and one transmitter data line (full duplex). Not all USARTs are implemented with full modem control lines. Furthermore the available lines depend largely on the used multiplexing. Most modem control lines can be implemented with standard digital ports.

Hardware Interrupts. There are several interrupt sources for each USART:

- Receive: RX Ready, (DMA) Buffer Full, End of Receive Buffer
- Transmit: TX Ready, (DMA) Buffer Empty, End of Transmit Buffer, Shift Register Empty
- Errors: overrun, parity, framing, and timeout errors

- Handshake: the status of CTS has changed
- Break: the receiver has detected a break condition on RXD
- NACK: non acknowledge (ISO7816 mode only)
- Iteration: the maximum number of repetitions has been reached (ISO7816 mode only)

Please refer to the chapter about the DMA unit (PDC) for a description of the "Buffer Full" and "End of Receive / Transmit Buffer" events.

2.25. Synchronous Peripheral Interface (SPI)

The DropA5D22 has two standard SPI ports, each one with four chip selects. However, SPI0 NPCS0 is used for the internal serial flash and should thus not be used by external peripherals.

Moreover, there are two additional QSPI ports on the DropA5D22 (Quad SPI). These may be used in 4-bit, 2-bit, or 1-bit operating mode.

Yet another four SPI's are available within the "Flexcom" (USART) interfaces (see Flexcom).

The Serial Peripheral Interface (SPI) circuit is a synchronous serial data link that provides communication with external devices in Master or Slave Mode. It also enables communication between processors if an external processor is connected to the system.

The Serial Peripheral Interface is essentially a shift register that serially transmits data bits to other SPIs. During a data transfer, one SPI system acts as the "master" which controls the data flow, while the other devices act as "slaves" which have data shifted into and out by the master.

A slave device is selected when the master asserts its NSS signal. If multiple slave devices exist, the master generates a separate slave select signal for each slave (NPCS). The SPI system consists of two data lines and two control lines:

- Master Out Slave In (MOSI): This data line supplies the output data from the master shifted into the input(s) of the slave(s).
- Master In Slave Out (MISO): This data line supplies the output data from a slave to the input of the master. There may be no more than one slave transmitting data during any particular transfer.
- Serial Clock (SPCK): This control line is driven by the master and regulates the flow of the data bits. The master may transmit data at a variety of baud rates; the SPCK line cycles once for each bit that is transmitted. The SPI baudrate is Master Clock (MCK) divided by a value between 1 and 255
- Slave Select (NSS): This control line allows slaves to be turned on and off by hardware.

Each SPI Controller has a dedicated receive and transmit DMA channel.

2.26. Synchronous Serial Controller (SSC)

The DropA5D22 has one SSC interface available, depending on the multiplexing of the pins.

The SSC supports many serial synchronous communication protocols generally used in audio and telecom applications such as I2S, Short Frame Sync, Long Frame Sync, etc.

The SSC has separated receive and transmit channels. Each channel has a data, a clock and a frame synchronization signal (RD, RK, RF, resp. TD, TK, TF). Both a receive and a transmit DMA channel are assigned to each SSC.

2.27. LCD Controller (LCDC)

The SAMA5D22 has a full featured LCD-controller on chip which is capable to drive TFT displays with up to 1024x768 pixels.

2.27.1. LCD Signals and Timing

Usual 7 inch or 5.7 inch display have a color resolution of 18 bits. Thus 20 I/O lines, including "Data Enable" (LCD_DEN) and Pixel Clock (LCD_PCK) are required to display the complete color spectrum of the LCD. Of course, due to the limited number of I/O lines on the DropA5D22, this will inhibit a substantial number of other peripheral interfaces.

Many industrial applications only require a restricted number of colors, as in diagrams or user menus. In this case, a smaller subset of LCD data lines will be required, like 12 lines (4096 colors), 9 lines (512 colors), or even 6 lines (64 colors). If the application programmer has full control of the color space he is going to use, any subset of LCD data lines can be used to implement a fixed color set on the LCD.

The LCD_VS (VSYNC) and LCD_HS (HSYNC) signals are not necessary for most displays, as the "one-signal control" using only the LCD_DEN signal is sufficient in most cases. The DEN signal uses a "short" pulse as a line synchronization signal, and a "long" pulse as the frame synchronization signal. "Short" usually meaning something like 20 or 30 clock pulses, and "long" the duration of several lines, e.g. 10 or 20.

As most displays differ from each other, the correct timing has to be adapted for each display model. The following basic points must be configured in the LCDC in order to get a proper display output:

- the pixel clock rate,
- polarity of LCD_PCK and LCD_DEN signals,
- vertical and horizontal front porch of LCD_DEN,
- LCD_DEN pulse length (vertical and horizontal),

These values have to be taken from the datasheet of the LCD manufacturer.

The LCD_DISP (display on/off) and LCD_PWM (useful for backlight control!) are optional, but useful in many cases. The LCD_DISP signal may be connected to the respective pin of the LCD, or - in case that the LCD in question does not have such a pin - to the enable pin of a power distribution switch in order to switch the power supply of the LCD. A current limited switch like the TPS2552 should be used to avoid instantaneous capacitive loading of the supply voltage.

2.27.2. LCDC Initialisation and LCD Power Sequencing

LCD cells (pixels) should not be subjected to DC power for prolonged periods of time, as chemical decomposition might take place. Therefore, the LCD controller has to be initialized appropriately before switching on the LCD supply voltage.

Accordingly, the LCDC should not be stopped without deactivating the LCD supply voltage. The same is true if the LCDC is stopped indirectly by stopping the respective clock source.

The LCD backlight supply is not involved in these considerations. It may switched on or off at any time independently of the state of the LCDC. However, it is good practice to switch the backlight on only after the LCD controller has been initialised and a proper output screen is displayed.

2.27.3. Color Resolution

- 1, 2, 4, 8 bits per pixel in palletized mode
- 12, 16, 18, 19, 24, 25 or 32 bits per pixel in standard mode

The color resolutions of 1, 2, 4, and 8 bpp (bits per pixel) use a palette table which is made up of 24-bit entries (as part of 32-bit registers). The value of each pixel in the frame buffer serves as an index into the palette table.

Alpha-channel (transparency) information can be provided optionally as part of 16-, 19-, 25- and 32-bit resolutions, either as 1 bit, or as 8 bit transparency. A two dimension scaler is available for the "High End

Overlay" (overlay 3). Video information can also be provided as "YUV" in several modes. A color space conversion unit generates the RGB output in this case.

2.27.4. LCDC Frame Buffer

The LCDC frame buffer typically resides in the external DRAM. If overlays are used, each overlay has a frame buffer on its own.

- Base Layer (Background)
- Overlay 1 Layer Window
- Overlay 2 Layer Window
- High End Overlay (HEO) Window

The Linux frame buffer driver offers a function which returns the information about the frame buffer structure including the assignment of each frame buffer bit to a color channel bit. It is recommended that graphics software uses this function in order to achieve a correct color representation.

2.28. Image Sensor Interface (ISI)

The Image Sensor Interface (ISI) supports direct connection to the ITU-R BT. 601/656 8-bit mode compliant sensors and up to 12-bit grayscale sensors. It receives the image data stream from the image sensor on the 12-bit data bus. This module receives up to 12 bits for data, the horizontal and vertical synchronizations and the pixel clock. The reduced pin count alternative for synchronization is supported for sensors that embed SAV (start of active video) and EAV (end of active video) delimiters in the data stream.

The Image Sensor Interface interrupt line is generally connected to the Advanced Interrupt Controller and can trigger an interrupt at the beginning of each frame and at the end of a DMA frame transfer. If the SAV/EAV synchronization is used, an interrupt can be triggered on each delimiter event.

For 8-bit color sensors, the data stream received can be in several possible formats: YCbCr 4:2:2, RGB 8:8:8, RGB 5:6:5 and may be processed before the storage in memory. The data stream may be sent on both preview path and codec path if the bit CODEC_ON in the ISI_CR1 is one. To optimize the bandwidth, the codec path should be enabled only when a capture is required.

In grayscale mode, the input data stream is stored in memory without any processing. The 12-bit data, which represent the grayscale level for the pixel, is stored in memory one or two pixels per word, depending on the GS_MODE bit in the ISI_CR2 register. The codec datapath is not available when grayscale image is selected.

2.29. Analog-to-Digital Converter (ADC)

The ADC Controller is a 12-bit Analog-to-Digital Converter supporting resistive touch screen panels. It can be used as Touch Screen Controller, ADC or both supporting five lines maximum. It integrates a 5-to-1 analog multiplexer for analog to digital conversions of up to five analog lines, four power switches that measure both axis positions and a pen-interrupt and pen-loss switch.

The conversions extend from 0V to V_{ADVREF}, an external voltage reference for better accuracy. Every channel can be enabled and disabled seperately. It supports a sampling rate of 1 Mega-samples/sec.

3. Designing your own base board

3.1. Ethernet Controller (EMAC)

The emac needs an aditional PHY design. The emac supports both, MII and RMII interface.

Please take care of the specific layout requirements of the Ethernet port when designing a base board. The two signals of the transmitter pair (ETX+ and ETX-) should be routed in parallel (constant distance, e.g. 0.5mm) with no vias on their way to the RJ45-jack. The same is true for the receiver pair (ERX+ and ERX-). No other signals should be crossing or get next to these lines. If a ground plane is used on the base board, it should be omitted in the vicinity of the Ethernet signals.

A 1nF / 2kV capacitor should be connected between board ground and chassis ground (which is usually connected to the shield of the RJ45-jack).

3.2. USB Host Controller (UHP)

External Parts. A few external parts are required for the proper operation of the UHP:

- No pull-down resistors are needed.
- No series resistors are needed.
- ESD protection devices are recommended for applications which are subject to external contact. The restrictions with regard to capacitive loading have to be applied when selecting a protection device.
- A circuit to generate the 5V VBUS supply voltage.

V_{BUS} considerations for USB Host. A USB host port has to provide a supply voltage V_{BUS} of 5V +- 5% which has to be able to source a maximum of 500mA, or 100mA in case of battery operation. Please refer to the appropriate rules in the USB specification. A low ESR capacitor of at least 120µF has to be provided on V_{BUS} in order to avoid excessive voltage drops during current spikes.

V_{BUS} has to have an over-current protection. The over-current drawn temporarily on V_{BUS} must not exceed 5A. Polymeric PTCs or solid state switches are recommended by the specification. Suitable PPTCs are "MultiFuse" (Bourns), "PolyFuse" (Wickmann/Littelfuse), "PolySwitch" (Raychem/Tyco).

It is required that the over-current condition can be detected by software, so that V_{BUS} can be switched off or be reduced in power in such a case.

Layout considerations. The two traces of any of the differential pairs (USB-Host A+ and USB-Host A- , as well as USB-Host B+ and USB-Host B-) have to be routed closely in parallel to the USB connector. This is especially critical if the high speed mode is used.

3.3. USB Device Controller (UDP)

External Parts. A few external parts are required for the proper operation of the UDP:

- No pull-down resistors are needed.
- No series resistors are needed.
- A voltage divider on the 5V USB supply voltage VBUS converting this voltage to 3.3V (1.8V), e.g. 27 kΩ / 47 kΩ, for the VBUS monitoring input (USB_CNX), which has to chosen as a suitable PIO port.
- ESD protection devices are recommended for applications which are subject to external contact. The restrictions with regard to capacitive loading have to be applied when selecting a protection device.

The USB specification demands a switchable pull-up resistor of 1.5 kΩ on USB-Device+ which identifies the UDP as a full speed device to the attached host controller. On this module, this resistor is integrated on the chip. This pull-up resistor is required to be switchable in order not to source current to an attached but powered down host. This would otherwise constitute an irregular condition on the host. The software has to take care of this fact.

Operation with V_{BUS} as a Supply. Special care has to be taken if the module is powered by the VBUS supply. Please refer to the appropriate rules in the USB specification with regard to inrush current limiting and power switching. As the module draws more than 100mA in normal mode, it is a "high-power" device according to the specification (<100mA = "low-power", 100..500mA = "high-power"). It therefore requires staged switching which means that at power-up it should draw not more than 100mA on VBUS. The capacitive load of a USB device on VBUS should be not higher than 10µF.

3.4. Booting Strategies

3.4.1. Boot Sequence

On power-up the SAMA5D22 always boots the first level bootloader from internal ROM memory at address 0x0 (level-0 boot device). It can boot in standard boot mode, which will be described in this chapter, or in secure boot mode. How the secure boot mode can be enabled and how the chip operates in this mode is explained in an application note by Atmel which is only available under NDA. Please contact taskit support if you want to employ the secure bootloader.

The recommended boot device is the on-board serial flash memory (level-1 boot device). The "bootstrap loader" from serial flash will then load the operating system from an SD-Card. If no valid boostrap loader is present, the system will default to the SAM-BA monitor, implementing a connection via the USB device port.

Other boot strategies, e.g. NAND flash boot, are possible but not recommended.

3.4.2. SAM-BA Monitor

If no valid code is found among the configured boot devices, the SAM-BA monitor is launched. The SAM-BA Monitor initializes the DBGU and USB-Device. It then checks if an USB device enumeration occurs or if characters are received on the DBGU. Once the communication interface is identified, it runs an infinite loop, waiting for commands.

The SAM-BA monitor allows programming of flash and related functions. For this purpose Atmel provides a tool running on desktop PCs. If you need to use the SAM-BA monitor and have valid code on one of the booting devices, these have to be disabled first (e.g. disable chipselect of serial or nand flash or remove SD/MMC-Card).

Appendix A. Peripheral Identifiers and Address Map

After the execution of the remap command the 4 GB physical address space is separated as shown in the following table. Accessing these addresses directly is only possible if the MMU (memory management unit) is deactivated. As soon as the MMU is activated the visible address space is changed completely. If absolute memory addresses should be accessed within an application, the corresponding address space has first to be mapped to the virtual address space using mmap or ioremap under Linux.

Address	Peripheral ID	Mnemonic	Peripheral Name
Internal memories:			
0x00000000		ROM	
0x00040000		ECC ROM	
0x00100000		NFC (SRAM)	
0x00200000		SRAM0	
0x00220000		SRAM1	
0x00300000		UDPHS (RAM)	
0x00400000		UHPHS (OHCI)	
0x00500000		UHPHS (EHCI)	
0x00600000		AXIMX	
0x00700000		DAP	
0x00800000		L2CC	
External memories:			
0x10000000		EBI NCS0	EBI Chip Select 0
0x20000000		DDRCS	DDR Chip Select
0x40000000		DDRAESBCS	DDR AESB Chip Select
0x60000000		EBI NCS1	EBI Chip Select 1
0x70000000		EBI NCS2	EBI Chip Select 2
0x80000000		EBI NCS3	EBI Chip Select 3
0x90000000			QSPI0 AESB MEM
0x98000000			QSPI1 AESB MEM
0xA0000000	31;71	SDMMC0	SD-Card Controller memory
0xB0000000	32;72	SDMMC1	SD-Card Controller memory
0xC0000000		NFC CR	NAND Flash Controller Command Register
0xD0000000			QSPI0 MEM
0xD8000000			QSPI1 MEM
Internal peripherals:			
0xF0000000	45	LCDC	LCD-Controller
0xF0004000	7	XDMAC1	DMA-Controller
0xF0008000	46	ISC	Image Sensor Controller
0xF000C000	13	MPDDRC	Multiport DDR-SDRAM Controller
0xF0010000	6	XDMAC0	DMA Controller 0
0xF0014000	74	PMC	Power Management Controller
0xF0018000	15	MATRIX0	
0xF001C000	10	AESB	Advanced Encryption Standard Bridge
0xF0020000	52	QSPI0	Quad SPI Controller 0
0xF0024000	53	QSPI1	Quad SPI Controller 1
0xF0028000	12	SHA	Secure Hash Algorithm Engine
0xF002C000	9	AES	Advanced Encryption Standard Engine
0xF8000000	33	SPI0	SPI Controller 0
0xF8004000	43	SSC0	Synchronous Serial Controller 0

Address	Peripheral ID	Mnemonic	Peripheral Name
0xF8008000	5;66;67	GMAC	Ethernet Controller
0xF800C000	35	TC0 Ch0	32-Bit Timer 0 Channel 0
0xF800C040	35	TC0 Ch1	32-Bit Timer 0 Channel 1
0xF800C080	35	TC0 Ch2	32-Bit Timer 0 Channel 2
0xF8010000	36	TC1 Ch3	32-Bit Timer 1 Channel 3
0xF8010040	36	TC1 Ch4	32-Bit Timer 1 Channel 4
0xF8010080	36	TC1 Ch5	32-Bit Timer 1 Channel 5
0xF8014000	17	HSMC	Static Memory Controller (for NAND-Flash or SRAM)
0xF8018000	48	PDMIC	Pulse Density Modulation Microphone
0xF801c000	24	UART0	Asynchronous Serial Port 0
0xF801c000	25	UART1	Asynchronous Serial Port 1
0xF801c000	26	UART2	Asynchronous Serial Port 2
0xF8028000	29	TWIHS0	TWI Controller 0 (I2C)
0xF802C000	38	PWM	Pulse Width Modulation Controller
0xF8030000	60	SFR	Special Function Register
0xF8034000	19	FLEXCOM0	USART 0 - UART, SPI, TWI, LIN
0xF8038000	20	FLEXCOM1	USART 1 - UART, SPI, TWI, LIN
0xF803C000	0;61	SAIC	Secure Advanced Interrupt Controller
0xF8040000	8	ICM	Integrity Check Monitor
0xF8044000	51	SECURAM	Secured SRAM
0xF8048000	74	SYSC RSTC	Reset Controller (System Controller)
0xF8048010		SYSC SHDWC	Shutdown/Wakeup Controller (Part of System Controller)
0xF8048030	3	SYSC PIT	Periodic Interval Timer (Part of System Controller)
0xF8048040	4	SYSC WDT	Watchdog Timer (Part of System Controller)
0xF8048050		SYSC SCKC	Slow Clock Controller (Part of System Controller)
0xF80480b0	74	SYSC RTC	Real Time Clock (Part of System Controller)
0xF8049000	76	RXLP	Low Power Asynchronous Receiver (for Wakeup)
0xF804A000	75	ACC	Analog Comparator
0xF804B000		RESERVED	
0xF804C000	50	SFC	Secure Fuse Controller
0xF8050000	54	I2SC0	Inter-IC Sound Controller 0
0xF8054000	56;64	CAN0	CAN Controller 0
0xFC000000	34	SPI1	SPI Controller 1
0xFC004000	44	SSC1	Synchronous Serial Controller 1
0xFC008000	27	UART3	Asynchronous Serial Port
0xFC00C000	28	UART4	Asynchronous Serial Port
0xFC010000	21	FLEXCOM2	USART 2 (not available on "DropA5D2")
0xFC014000	22	FLEXCOM3	USART 3 - UART, SPI, TWI, LIN
0xFC018000	23	FLEXCOM4	USART 4 - UART, SPI, TWI, LIN
0xFC01C000	47	TRNG	True Random Number Generator
0xFC020000	49;62	AIC	
0xFC024000		RESERVED	
0xFC028000	30	TWIHS1	TWI Controller 1 (I2C)
0xFC02C000	42	UDPHS	USB Host Controller
0xFC030000	40	ADC	Analog-to-Digital Converter
0xFC034000		RESERVED	
0xFC038000	18	PIOA	32-Bit Peripheral I/O Controller A
0xFC03C000	14	MATRIX1	
0xFC040000	16	SECUMOD	Security Module

Address	Peripheral ID	Mnemonic	Peripheral Name
0xFC044000	11	TDES	Triple-DES Engine
0xFC048000	59	CLASSD	Stereo Audio Class-D Amplifier
0xFC04C000	55	I2SC1	Inter-IC Sound Controller 1
0xFC050000	57;65	CAN1	CAN Controller 1 (not availabe on DropA5D2)
0xFC054000		UTMI	USB 2.0 Transceiver Macrocell Interface
0xFC058000		RESERVED	
0xFC05C000	77	SFRBU	Special Function Registers Backup
0xFC060000		RESERVED	
0xFC064000		RESERVED	
0xFC068000		RESERVED	
0xFC069000	78	CHIPID	Chip Identifier Registers
0xFC06A000		RESERVED	

Table A.1. Peripheral Identifiers

Appendix B. DropA5D22 PIO Functions

Pin#	PIO#	SD-Card, LCD, EMAC, ADC	UART, USART	QSPI, TWI, CAN, IRQ	SPI, SSC, PCK	I2S, ClassD-Amplifier, Microphone	Timer	EBI	ISC, PWM
99	PA18	SD_D0							
97	PA19	SD_D1							
95	PA20	SD_D2							
93	PA21	SD_D3		IRQ	PCK2		TIOA0		
91	PA22	SD_CLK	US1_SCK	QSPI0_SCK	SPI1_SCK		TIOB0	D0	
89	PA23		US1_TXD	QSPI0_CS	SPI1_MOSI		TCLK0	D1	
87	PA24		US1_RXD	QSPI0_IO0	SPI1_MISO			D2	
85	PA25		US1_CTS	QSPI0_IO1	SPI1_CS0			D3	
83	PA26		US1_RTS	QSPI0_IO2	SPI1_CS1			D4	
81	PA27			QSPI0_IO3	SPI0/1_CS2		TIOA1	D5	
79	PA28	SD_CMD			SPI0/1_CS3	CLASSD_L0	TIOB1	D6	
77	PA29				SPI0_CS1	CLASSD_L1	TCLK1	D7	
75	PA30				SPI0_CS0	CLASSD_L2		WR0/WE	PWMH0
73	PA31				SPI0_MISO	CLASSD_L3		CS3	PWML0
78	PB0				SPI0_MOSI			A21/ALE	PWMH1
76	PB1				SPI0_SCK	CLASSD_R0		A22/CLE	PWML1
74	PB2					CLASSD_R1		RD/OE	PWMFI0
72	PB3		URXD4	IRQ		CLASSD_R2		D8	PWMTRG0
70	PB4		UTXD4	FIQ		CLASSD_R3		D9	
68	PB5			QSPI1_SCK			TCLK2	D10	PWMH2
66	PB6			QSPI1_CS			TIOA2	D11	PWML2
64	PB7			QSPI1_IO0			TIOB2	D12	PWMH3
60	PB8			QSPI1_IO1			TCLK3	D13	PWML3
58	PB9			QSPI1_IO2			TIOA3	D14	PWMFI1
56	PB10			QSPI1_IO3			TIOB3	D15	PWMTRG1
54	PB11	LCD_BL0	URXD3			PDMIC_DAT		A0/BS0	
52	PB12	LCD_BL1	UTXD3			PDMIC_CLK		A1	
50	PB13	LCD_BL2			PCK1			A2	
48	PB14	LCD_BL3		QSPI1_SCK	SSC1_TK	I2S1_MCK		A3	
46	PB15	LCD_BL4		QSPI1_CS	SSC1_TF	I2S1_CK		A4	
44	PB16	LCD_BL5		QSPI1_IO0	SSC1_TD	I2S1_WS		A5	
42	PB17	LCD_BL6		QSPI1_IO1	SSC1_RD	I2S1_DI0		A6	
40	PB18	LCD_BL7		QSPI1_IO2	SSC1_RK	I2S1_DO0		A7	
38	PB19	LCD_GR0		QSPI1_IO3	SSC1_RF		TIOA3	A8	
34	PB20	LCD_GR1			SSC0_TK		TIOB3	A9	
32	PB21	LCD_GR2	US3_SCK		SSC0_TF		TCLK3	A10	
30	PB22	LCD_GR3	US3_RXD		SSC0_TD		TIOA2	A11	
28	PB23	LCD_GR4	US3_TXD		SSC0_RD		TIOB2	A12	
26	PB24	LCD_GR5	US3_CTS		SSC0_RK		TCLK2	A13	ISC_D10
24	PB25	LCD_GR6	US3_RTS		SSC0_RF			A14	ISC_D11
22	PB26	LCD_GR7	URXD0			PDMIC_DAT		A15	ISC_D0
20	PB27	LCD_RED0	UTXD0			PDMIC_CLK		A16	ISC_D1
18	PB28	LCD_RED1	US0_TXD				TIOA5	A17	ISC_D2
16	PB29	LCD_RED2	US0_RXD				TIOB5	A18	ISC_D3
14	PB30	LCD_RED3	US0_SCK				TCLK5	A19	ISC_D4
12	PB31	LCD_RED4	US0_CTS	TWD0				A20	ISC_D5

Pin#	PIO#	SD-Card, LCD, EMAC, ADC	UART, USART	QSPI, TWI, CAN, IRQ	SPI, SSC, PCK	I2S, ClassD-Amplifier, Microphone	Timer	EBI	ISC, PWM
1	PC0	LCD_RED5	US0_RTS	TWCK0				A23	ISC_D6
3	PC1	LCD_RED6		CANTX0	SPI1_SCK	I2S0_CK		A24	ISC_D7
5	PC2	LCD_RED7		CANRX0	SPI1_MOSI	I2S0_MCK		A25	ISC_D8
7	PC3	LCD_PWM			SPI1_MISO	I2S0_WS	TIOA1	WAIT	ISC_D9
9	PC4	LCD_DISP			SPI1_CS0	I2S0_DI0	TIOB1	WR1/BS1	ISC_PCK
11	PC5	LCD_VS			SPI1_CS1	I2S0_DO0	TCLK1	CS0	ISC_VS
13	PC6	LCD_HS		TWD1	SPI1_CS2			CS1	ISC_HS
15	PC7	LCD_PCK	URXD1	TWCK1	SPI1_CS3			CS2	ISC_MCK
19	PC8	LCD_DEN	UTXD1	FIQ	PCK0			NANDRDY	ISC_FIELD
59	PD7								
57	PD8								
55	PD9	GTXCK							
53	PD10	GTXEN							
51	PD11	GRXDV			PCK2		TIOA1		ISC_MCK
49	PD12	GRXER	US4_TXD				TIOB1		ISC_D4
47	PD13	GRX0	US4_RXD				TCLK1		ISC_D5
45	PD14	GRX1	US4_SCK						ISC_D6
43	PD15	GTX0	US4_CTS						ISC_D7
39	PD16	GTX1	US4_RTS						ISC_D8
37	PD17	GMDC							ISC_D9
35	PD18	GMDIO							ISC_D10
33	PD19	AD0	URXD2	TWD1	PCK0	I2S0_CK			ISC_D11
31	PD20	AD1	UTXD2	TWCK1		I2S0_MCK	TIOA2		ISC_PCK
29	PD21	AD2	US4_TXD	TWD0		I2S0_WS	TIOB2		ISC_VS
27	PD22	AD3	US4_RXD	TWCK0		I2S0_DI0	TCLK2		ISC_HS
25	PD23	AD4	US4_SCK			I2S0_DO0			ISC_FIELD

Table B.1.

Appendix C. DropA5D22 PIO Multiplexing

Pin FX8	PIO# / A/D Channel	Function A	I/O Set	Function B	I/O Set	Function C	I/O Set	Function D	I/O Set	Function E	I/O Set	Function F	I/O Set
99	PA18	SPI0_NPCS1	1	RK1	1	QSPI0_IO2	2	I2SC1_DO0	2	SDMMC1_DAT0	1	D13	2
97	PA19	SPI0_NPCS2	1	RF1	1	QSPI0_IO3	2	TIOA0	1	SDMMC1_DAT1	1	D14	2
95	PA20	SPI0_NPCS3	1					TIOB0	1	SDMMC1_DAT2	1	D15	2
93	PA21	IRQ	2	PCK2	3			TCLK0	1	SDMMC1_DAT3	1	NANDRDY	2
91	PA22	FLEXCOM1_IO2	1	D0	1	TCK/SWCLK	4	SPI1_SPCK	2	SDMMC1_CK	1	QSPI0_SCK	3
89	PA23	FLEXCOM1_IO1	1	D1	1	TDI	4	SPI1_MOSI	2			QSPI0_CS	3
87	PA24	FLEXCOM1_IO0	1	D2	1	TDO	4	SPI1_MISO	2			QSPI0_IO0/MOSI	3
85	PA25	FLEXCOM1_IO3	1	D3	1	TMS/SWDIO	4	SPI1_NPCS0	2			QSPI0_IO1/MISO	3
83	PA26	FLEXCOM1_IO4	1	D4	1	NTRST	4	SPI1_NPCS1	2			QSPI0_IO2	3
81	PA27	TIOA1	2	D5	1	SPI0_NPCS2	2	SPI1_NPCS2	2	SDMMC1_RSTN	1	QSPI0_IO3	3
79	PA28	TIOB1	2	D6	1	SPI0_NPCS3	2	SPI1_NPCS3	2	SDMMC1_CMD	1	CLASSD_L0	1
77	PA29	TCLK1	2	D7	1	SPI0_NPCS1	2			SDMMC1_WP	1	CLASSD_L1	1
75	PA30			NWE/NANDWE	1	SPI0_NPCS0	2	PWMH0	1	SDMMC1_CD	1	CLASSD_L2	1
73	PA31			NCS3	1	SPI0_MISO	2	PWML0	1			CLASSD_L3	1
78	PB0			A21/NANDALE	1	SPI0_MOSI	2	PWMH1	1				
76	PB1			A22/NANDCLE	1	SPI0_SPCK	2	PWML1	1			CLASSD_R0	1
74	PB2			NRD/NANDOE	1			PWMFI0	1			CLASSD_R1	1
72	PB3	URXD4	1	D8	1	IRQ	3	PWMEXTRG0	1			CLASSD_R2	1
70	PB4	UTXD4	1	D9	1	FIQ	4					CLASSD_R3	1
68	PB5	TCLK2	1	D10	1	PWMH2	1	QSPI1_SCK	2			GTSUCOMP	3
66	PB6	TIOA2	1	D11	1	PWML2	1	QSPI1_CS	2			GTXER	3
64	PB7	TIOB2	1	D12	1	PWMH3	1	QSPI1_IO0/MOSI	2			GRXCK	3
60	PB8	TCLK3	1	D13	1	PWML3	1	QSPI1_IO1/MISO	2			GCRS	3
58	PB9	TIOA3	1	D14	1	PWMFI1	1	QSPI1_IO2	2			GCOL	3
56	PB10	TIOB3	1	D15	1	PWMEXTRG1	1	QSPI1_IO3	2			GRX2	3
54	PB11	LCDDAT0	1	A0/NBS0	1	URXD3	3	PDMIC_DAT	2			GRX3	3
52	PB12	LCDDAT1	1	A1	1	UTXD3	3	PDMIC_CLK	2			GTX2	3
50	PB13	LCDDAT2	1	A2	1	PCK1	3					GTX3	3
48	PB14	LCDDAT3	1	A3	1	TK1	2	I2SC1_MCK	1	QSPI1_SCK	3	GTXCK	3
46	PB15	LCDDAT4	1	A4	1	TF1	2	I2SC1_CK	1	QSPI1_CS	3	GTXEN	3
44	PB16	LCDDAT5	1	A5	1	TD1	2	I2SC1_WS	1	QSPI1_IO0/MOSI	3	GRXDV	3
42	PB17	LCDDAT6	1	A6	1	RD1	2	I2SC1_DI0	1	QSPI1_IO1/MISO	3	GRXER	3
40	PB18	LCDDAT7	1	A7	1	RK1	2	I2SC1_DO0	1	QSPI1_IO2	3	GRX0	3
38	PB19	LCDDAT8	1	A8	1	RF1	2	TIOA3	2	QSPI1_IO3	3	GRX1	3
34	PB20	LCDDAT9	1	A9	1	TK0	1	TIOB3	2	PCK1	4	GTX0	3
32	PB21	LCDDAT10	1	A10	1	TF0	1	TCLK3	2	FLEXCOM3_IO2	3	GTX1	3
30	PB22	LCDDAT11	1	A11	1	TD0	1	TIOA2	2	FLEXCOM3_IO1	3	GMDC	3
28	PB23	LCDDAT12	1	A12	1	RD0	1	TIOB2	2	FLEXCOM3_IO0	3	GMDIO	3
26	PB24	LCDDAT13	1	A13	1	RK0	1	TCLK2	2	FLEXCOM3_IO3	3	ISC_D10	3
24	PB25	LCDDAT14	1	A14	1	RF0	1			FLEXCOM3_IO4	3	ISC_D11	3
22	PB26	LCDDAT15	1	A15	1	URXD0	1	PDMIC_DAT	1			ISC_D0	3
20	PB27	LCDDAT16	1	A16	1	UTXD0	1	PDMIC_CLK	1			ISC_D1	3
18	PB28	LCDDAT17	1	A17	1	FLEXCOM0_IO0	1	TIOA5	2			ISC_D2	3
16	PB29	LCDDAT18	1	A18	1	FLEXCOM0_IO1	1	TIOB5	2			ISC_D3	3
14	PB30	LCDDAT19	1	A19	1	FLEXCOM0_IO2	1	TCLK5	2			ISC_D4	3
12	PB31	LCDDAT20	1	A20	1	FLEXCOM0_IO3	1	TWD0	1			ISC_D5	3
1	PC0	LCDDAT21	1	A23	1	FLEXCOM0_IO4	1	TWCK0	1			ISC_D6	3
3	PC1	LCDDAT22	1	A24	1	CANTX0	1	SPI1_SPCK	1	I2SC0_CK	1	ISC_D7	3
5	PC2	LCDDAT23	1	A25	1	CANRX0	1	SPI1_MOSI	1	I2SC0_MCK	1	ISC_D8	3
7	PC3	LCDPWM	1	NWAIT	1	TIOA1	1	SPI1_MISO	1	I2SC0_WS	1	ISC_D9	3
9	PC4	LCDDISP	1	NWR1/NBS1	1	TIOB1	1	SPI1_NPCS0	1	I2SC0_DI0	1	ISC_PCK	3
11	PC5	LCDVSYNC	1	NCS0	1	TCLK1	1	SPI1_NPCS1	1	I2SC0_DO0	1	ISC_VSYNC	3
13	PC6	LCDHSYNC	1	NCS1	1	TWD1	1	SPI1_NPCS2	1			ISC_HSYNC	3
15	PC7	LCDPCK	1	NCS2	1	TWCK1	1	SPI1_NPCS3	1	URXD1	2	ISC_MCK	3
19	PC8	LCDDEN	1	NANDRDY	1	FIQ	1	PCK0	3	UTXD1	2	ISC_FIELD	3
59	PD7	TDI	2			UTMI_RXVAL	1	GTX2	2	ISC_D0	2	NWR1/NBS1	2
57	PD8	TDO	2			UTMI_RXERR	1	GTX3	2	ISC_D1	2	NANDRDY	2
55	PD9	TMS/SWDIO	2			UTMI_RXACT	1	GTXCK	2	ISC_D2	2		
53	PD10	NTRST	2			UTMI_HDIS	1	GTXEN	2	ISC_D3	2		
51	PD11	TIOA1	3	PCK2	2	UTMI_LS0	1	GRXDV	2	ISC_D4	2	ISC_MCK	4
49	PD12	TIOB1	3	FLEXCOM4_IO(	2	UTMI_LS1	1	GRXER	2	ISC_D5	2	ISC_D4	4
47	PD13	TCLK1	3	FLEXCOM4_IO'	2	UTMI_CDRCPSEL	1	GRX0	2	ISC_D6	2	ISC_D5	4
45	PD14	TCK/SWCLK	1	FLEXCOM4_IO2	2	UTMI_CDRCPSEL	1	GRX1	2	ISC_D7	2	ISC_D6	4
43	PD15	TDI	1	FLEXCOM4_IO3	2	UTMI_CDRCPDIV	1	GTX0	2	ISC_PCK	2	ISC_D7	4
39	PD16	TDO	1	FLEXCOM4_IO4	2	UTMI_CDRBISTE	1	GTX1	2	ISC_VSYNC	2	ISC_D8	4
37	PD17	TMS/SWDIO	1			UTMI_CDRCPSEL	1	GMDC	2	ISC_HSYNC	2	ISC_D9	4
35	PD18	NTRST	1					GMDIO	2	ISC_FIELD	2	ISC_D10	4
33	PD19 / AD0	PCK0	1	TWD1	3	URXD2	3			I2SC0_CK	2	ISC_D11	4
31	PD20 / AD1	TIOA2	3	TWCK1	3	UTXD2	3			I2SC0_MCK	2	ISC_PCK	4
29	PD21 / AD2	TIOB2	3	TWD0	4	FLEXCOM4_IO0	3			I2SC0_WS	2	ISC_VSYNC	4
27	PD22 / AD3	TCLK2	3	TWCK0	4	FLEXCOM4_IO1	3			I2SC0_DI0	2	ISC_HSYNC	4
25	PD23 / AD4	URXD2	2			FLEXCOM4_IO2	3			I2SC0_DO0	2	ISC_FIELD	4

Figure C.1.

Color Codes

Supply Rail for PIO Pin:
VDDIOP0
VDDIOP1
VDDANA

FLEXCOM Functions			
Name	W	USART/UART	SPI
FLEXCOM_IO0	N	TXD	MOSI
FLEXCOM_IO1	V	RXD	MISO
FLEXCOM_IO2		SCK	SPCK
FLEXCOM_IO3		CTS	NPCS0/NSS
FLEXCOM_IO4		RTS	NPCS1

SDMMC	SD-Card	SPI	Serial Peripheral Interface
RMII	Ethernet	QSPI	Quad SPI
FLEXCOM	USART/SPI/TWI	I2S	Inter-IC Sound Controller
UART		SSC	Synchronous Serial Controlle
TWI	aka I2C	LCD	
JTAG/SWD	JTAG/Single Wire Debug	ISC	Image Sensor Interface
TIMER		PWM	Pulse Width Modulator
EBI	Parallel Bus (EBI / HSMC)	PDMIC	Microphone
IRQ/FIQ	Interrupt/Fast Interrupt	CLASSD	Stereo Speaker
PCK	Programmable Clock	PNU	Probably never used
AD	Analog-Digital-Converter	TDO	Incomplete Peripherals on BGA196 package, therefor not to be used
CAN	CAN-Bus		

Figure C.2.

Appendix D. DropA5D22 Pin Assignment

Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	PC0	PIO C	2	VDD3V3	Supply Voltage 3.3V
3	PC1	PIO C	4	VDD3V3	Supply Voltage 3.3V
5	PC2	PIO C	6	NRST	System Reset, active low
7	PC3	PIO C	8	CLK_AUDIO	Audio Clock Output
9	PC4	PIO C	10	GND	System Ground
11	PC5	PIO C	12	PB31	PIO B
13	PC6	PIO C	14	PB30	PIO B
15	PC7	PIO C	16	PB29	PIO B
17	GND	System Ground	18	PB28	PIO B
19	PC8	PIO C	20	PB27	PIO B
21	SHDN	Shutdown Output, active low	22	PB26	PIO B
23	WKUP	Wakeup Input	24	PB25	PIO B
25	PD23	PIO D	26	PB24	PIO B
27	PD22	PIO D	28	PB23	PIO B
29	PD21	PIO D	30	PB22	PIO B
31	PD20	PIO D	32	PB21	PIO B
33	PD19	PIO D	34	PB20	PIO B
35	PD18	PIO D	36	GND	System Ground
37	PD17	PIO D	38	PB19	PIO B
39	PD16	PIO D	40	PB18	PIO B
41	GND	System Ground	42	PB17	PIO B
43	PD15	PIO D	44	PB16	PIO B
45	PD14	PIO D	46	PB15	PIO B
47	PD13	PIO D	48	PB14	PIO B
49	PD12	PIO D	50	PB13	PIO B
51	PD11	PIO D	52	PB12	PIO B
53	PD10	PIO D	54	PB11	PIO B
55	PD9	PIO D	56	PB10	PIO B
57	PD8	PIO D	58	PB9	PIO B
59	PD7	PIO D	60	PB8	PIO B
61	HHSDPB	USB Host B/USB Device "+"	62	GND	System Ground
63	HHSDMB	USB Host B/USB Device "-"	64	PB7	PIO B
65	GND	System Ground	66	PB6	PIO B
67	HHSDPA	USB Host A "+"	68	PB5	PIO B
69	HHSDMA	USB Host A "-"	70	PB4	PIO B
71	GND	System Ground	72	PB3	PIO B
73	PA31	PIO A	74	PB2	PIO B
75	PA30	PIO A	76	PB1	PIO B
77	PA29	PIO A	78	PB0	PIO B
79	PA28	PIO A	80	COMPP	Analog Comparator Positive Input
81	PA27	PIO A	82	COMPN	Analog Comparator Negative Input
83	PA26	PIO A	84	VDDBU	Backup Supply Voltage
85	PA25	PIO A	86	ADVREF	ADC Reference Voltage Input
87	PA24	PIO A	88	GND	System Ground
89	PA23	PIO A	90	PIOBU5	Tamper Detection Pin
91	PA22	PIO A	92	PIOBU4	Tamper Detection Pin
93	PA21	PIO A	94	PIOBU3	Tamper Detection Pin
95	PA20	PIO A	96	PIOBU2	Tamper Detection Pin

Pin	Mnemonic	Description	Pin	Mnemonic	Description
97	PA19	PIO A	98	PIOBU1	Tamper Detection Pin
99	PA18	PIO A	100	PIOBU0	Tamper Detection Pin

Table D.1.

Appendix E. DropA5D22 Electrical Characteristics

Ambient temperature 25°C, unless otherwise indicated

Symbol	Description	Parameter	Min.	Typ.	Max	Unit
V_{CC}	Operating Voltage		3.1	3.3	3.6	V
V_{ADVREF}	ADC Reference Voltage		2.0		V_{CC}	V
I_{ADVREF}	I_{ADVREF} input current	V_{ADVREF} = 3.3V			460	µA
V_{RES}	Reset Treshhold		2.85	2.93	3.0	V
T_{RES}	Duration of Reset Pulse		140		460	ms
V_{IH}	High-Level Input Voltage	V_{CC} = 3.3V	2.0		V_{CC} + 0.3	V
V_{IL}	Low-Level Input Voltage	3.3V	-0.3		0.8	V
P	Normal Operation			TBD		mW
	Full Load	max.		TBD		mW
	Stand-By			TBD		mW
	Power-Down			TBD		mW
V_{BATT}	Battery Voltage		1.65	3.0	V_{CC}	V
I_{BATT}	Battery Current	Ambient temp. = 25°C		5		µA
		Ambient temp. = 70°C			17	µA
		Ambient temp. = 85°C			22	µA

Table E.1. Electrical Characteristics

Appendix F. DropA5D22 Clock Characteristics

Symbol	Description	Dependency	Tolerance	Typical Value	Unit
MAINCK	Main Oscillator frequency			12.000	MHz
SLCK	Slow Clock			32.768	KHz
PLLACK	PLLA Clock	MAINCK		800.000	MHz
PCK	Processor Clock	PLLACK		400.000	MHz
MCK	Master Clock	PCK		133.000	MHz
DDCK	DDRAM Clock	MCK		266.000	MHz
BCK	Baudrate Clock	MCK	1.5%	8.25(max)	MHz
UPLLCK	USB Clock	MAINCK	0.25%	480.000	MHz

Table F.1. Clock Characteristics

Appendix G. DropA5D22 Environmental Ratings

Symbol	Description	Parameter	Operating		Storage		Unit
			Min.	**Max.**	**Min.**	**Max.**	
T_A	Ambient temperature		-30	85	-45	85	°C
	Relative Humidity	no condensation		90		90	%RH
	Absolute Humidity		<= Humidity@T_A = 60°C, 90%RH				
	Corrosive Gas		not admissible				

Table G.1. Environmental Ratings

Appendix H. DropA5D22 Dimensions

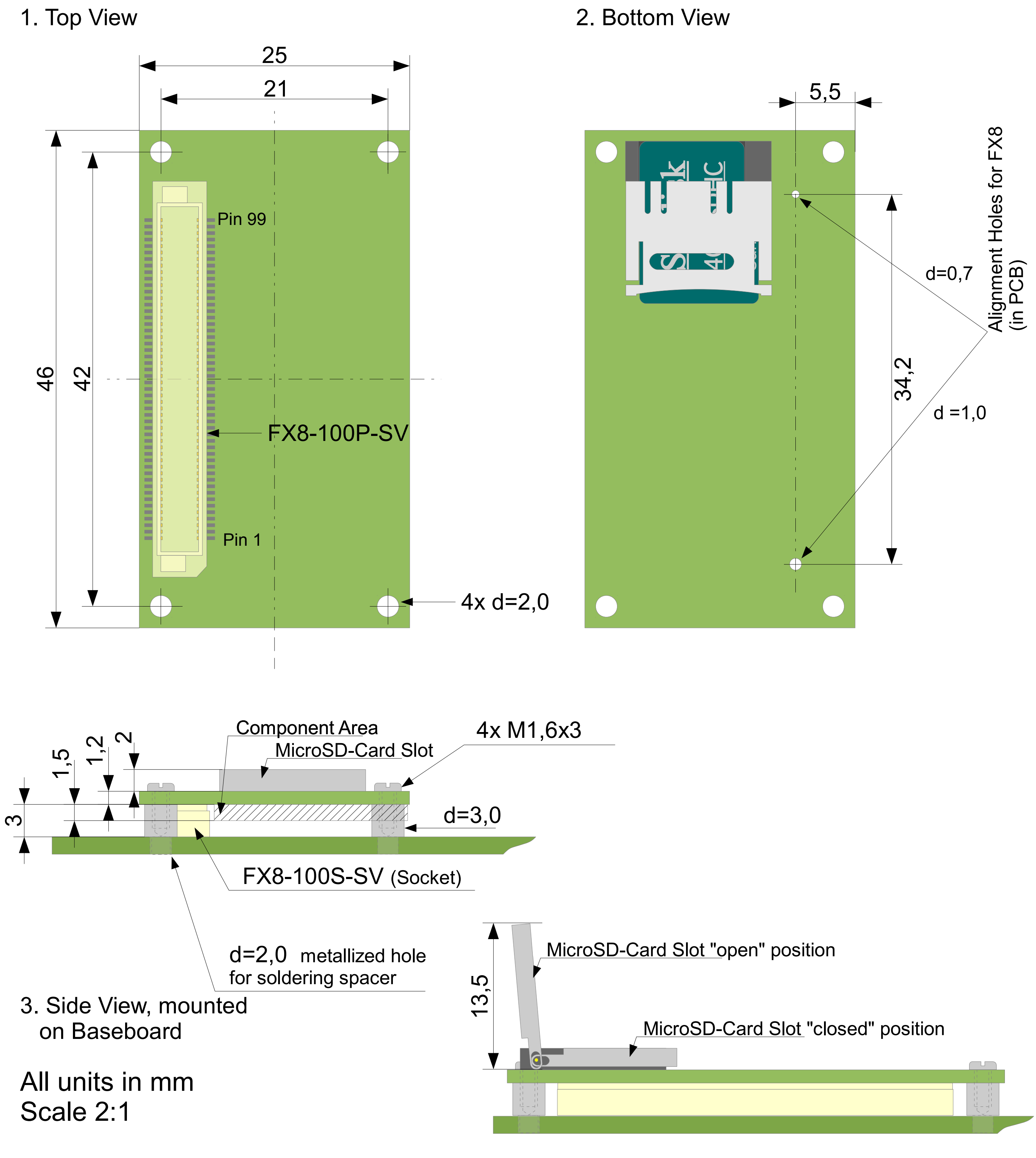

Figure H.1. DropA5D22 Dimensions

Appendix I. Starterkit Schematics

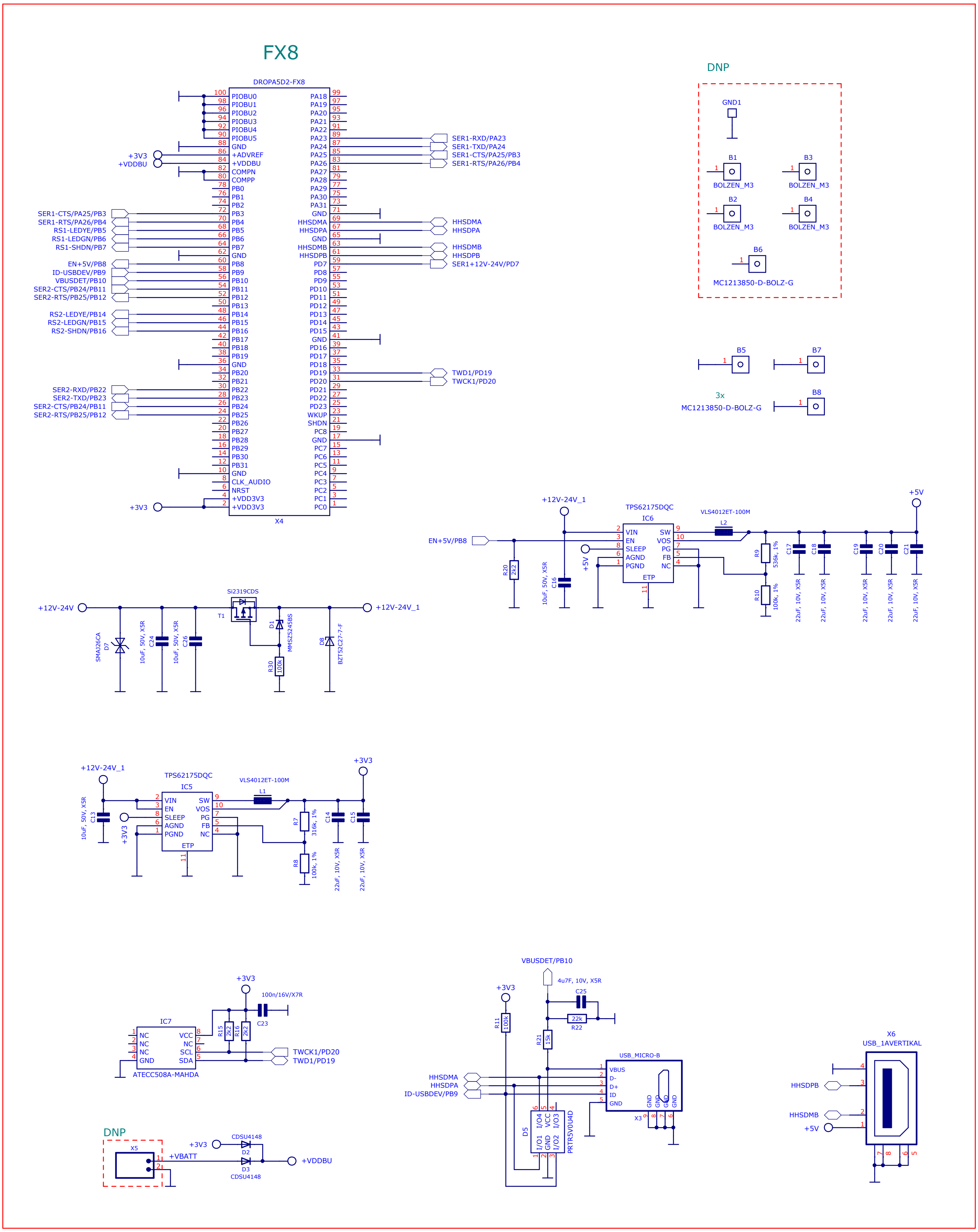

Figure I.1. Starterkit FX8

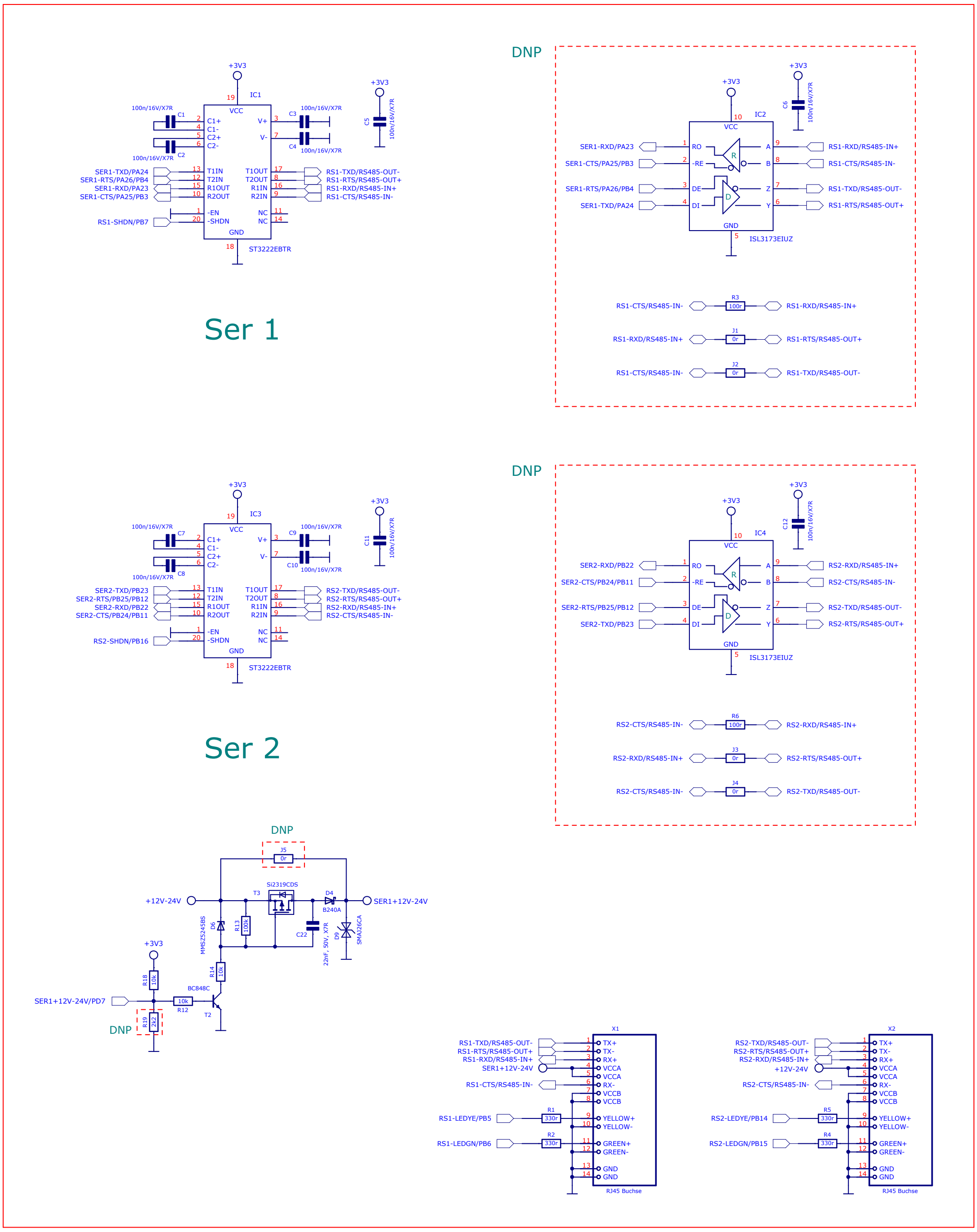

Figure I.2. Starterkit Buffer

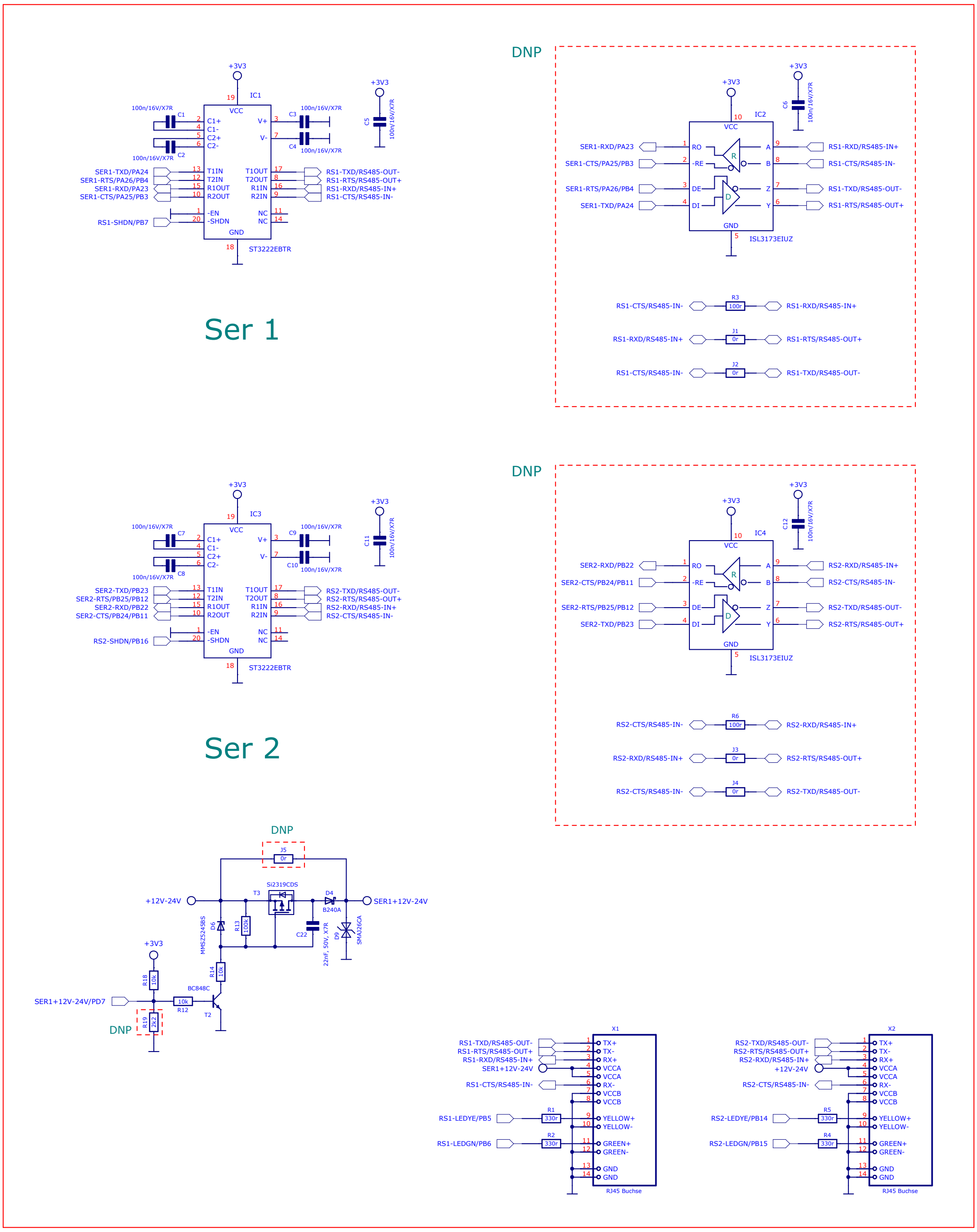

Figure I.3. Starterkit Buffer