

GMA306 $\pm 16g$ 2+1-Axis Digital Accelerometer

General Introduction

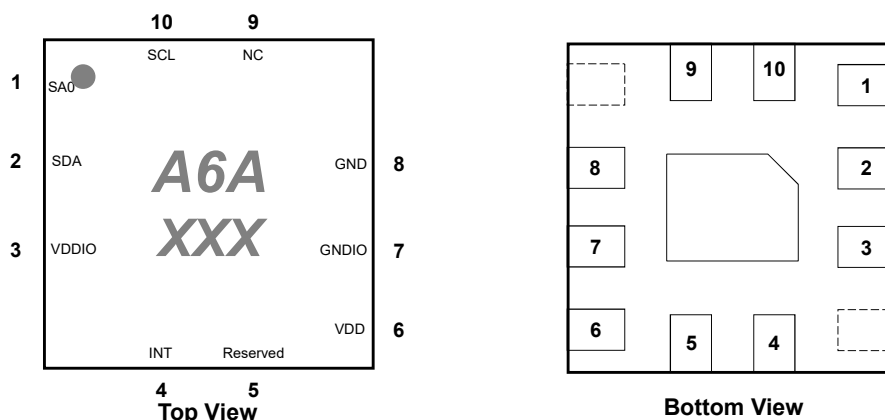
GMA306 is a 2+1-Axis digital accelerometer of $\pm 16g$ dynamic range with 13-bit ADC resolution along X/Y axes and 11-bit ADC resolution along Z axis. It integrates a MEMS sensing element and a CMOS conditioning IC in a compact $2 \times 2 \times 1 \text{ mm}^3$ package. The high resolution makes feasible precise applications like e-Compass tilt compensation. The wide sensing range further opens enough windows for motion detection. Finally the small form factor makes it an easy fit-in for compact applications like wearables.

Features

- 2+1-Axis digital accelerometer with $\pm 16g$ dynamic range
- 13 bit ADC resolution with sensitivity 256 LSB/g for X/Y axes
- 11 bit ADC resolution with sensitivity 64 LSB/g for Z axis
- Digital I2C interface supporting both fast mode (400kHz) and normal mode (100kHz)
- Temperature sensor for internal compensation and capable of digital output
- Operation voltage: +1.7V ~ +3.6V; IO interface voltage: +1.7V ~ +3.6V
- Power consumption:
 - Continuous mode (CM): typical 140uA to 250uA for 128Hz ODR
 - Non-Continuous mode (NCM): typical 85uA to 100uA for 1~8Hz ODR
 - Suspend current < 1uA
- One interrupt pin with selectable polarity and push-pull/open-drain option
- Built-in functions:
 - Data-ready interrupt
 - Motion detection: normal and differential modes
 - Auto-Wake/Sleep transition
 - 4-tap moving average filter with high-/low-pass option
- 5000g shock tolerance
- 12-pin QFN (10 pin-out) lead-free, RoHS compliance package: $2 \times 2 \times 1 \text{ mm}^3$.

Applications

Smart user interface, e-compass tilt-compensation, motion detection and analysis



Specifications

Table 1: Pin Descriptions

| Pin# | Name | Description | Pin# | Name | Description |
|------|----------|-------------------------|------|-------|-----------------------------|
| 1 | SA0 | Slave address selection | 6 | VDD | Operation voltage, 1.7~3.6V |
| 2 | SDA | I2C serial data | 7 | GNDIO | Ground for IO power |
| 3 | VDDIO | IO voltage, 1.7~3.6V | 8 | GND | Ground for operation power |
| 4 | INT | Interrupt output | 9 | NC | No connection inside |
| 5 | Reserved | Floating or grounded | 10 | SCL | I2C serial clock |

Table 2: General Specification

Operation voltage VDD = 3V, environment temperature $T_a = 25^{\circ}\text{C}$ if not specified otherwise

| Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---------------------------------|---|-----------|-------------------|-----------|------------------------|
| Operation voltage (VDD) | $T_a = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ | 1.7 | 3.0 | 3.6 | V |
| IO voltage (VDDIO) | $T_a = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ | 1.7 | — | 3.6 | V |
| CM operating current | ODR = 128 Hz, low power ODR = 128 Hz, low noise ODR = 128 Hz, high resolution | — | 140 180 250 | — | uA |
| NCM operating current | ODR = 8 Hz ODR = 4 Hz ODR = 2 Hz ODR = 1 Hz | 85 | — | 100 | uA |
| Suspend current | | — | 1 | — | uA |
| Dynamic range | | — | ± 16 | — | g |
| Sensitivity | X/Y Z | 230 58 | 256 64 | 282 70 | LSB/g |
| Zero-g offset, calibrated | | — | ± 60 | — | mg |
| Sensitivity to temp. dependency | $T_a = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ | — | ± 0.08 | — | %/ $^{\circ}\text{C}$ |
| Zero-g offset temp. dependency | $T_a = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ | — | ± 2 | — | mg/ $^{\circ}\text{C}$ |
| Nonlinearity | | — | ± 2 | — | %FS |
| Cross axis sensitivity | | — | 2 | — | % |
| Noise | X/Y Z | — | 1.1 4.5 | — | mg/ $\sqrt{\text{Hz}}$ |
| Operation temperature | | -40 | — | +85 | $^{\circ}\text{C}$ |

| | | | | | |
|---------------------|--|-----|---|------|----|
| Storage temperature | | -40 | — | +125 | °C |
|---------------------|--|-----|---|------|----|

Table 3: Absolute Maximum Rating

| Parameter | Rating |
|------------------------------|---------------------------|
| $V_{op}-GND$ | -0.3 ~ 4 V |
| Any other pin voltage | GND-0.3 to $V_{op}+0.3$ V |
| Temperature Range (Storage) | -40°C to +125°C |
| ESD | 2KV (HBM) |
| Mechanical Shock (unpowered) | 5,000 g for 0.2ms |
| Freefall on concrete surface | 1.5 m |

Note: Stress above the absolute maximum rating as listed in Table 3 may cause permanent damage to the device

Block Diagram and Connection

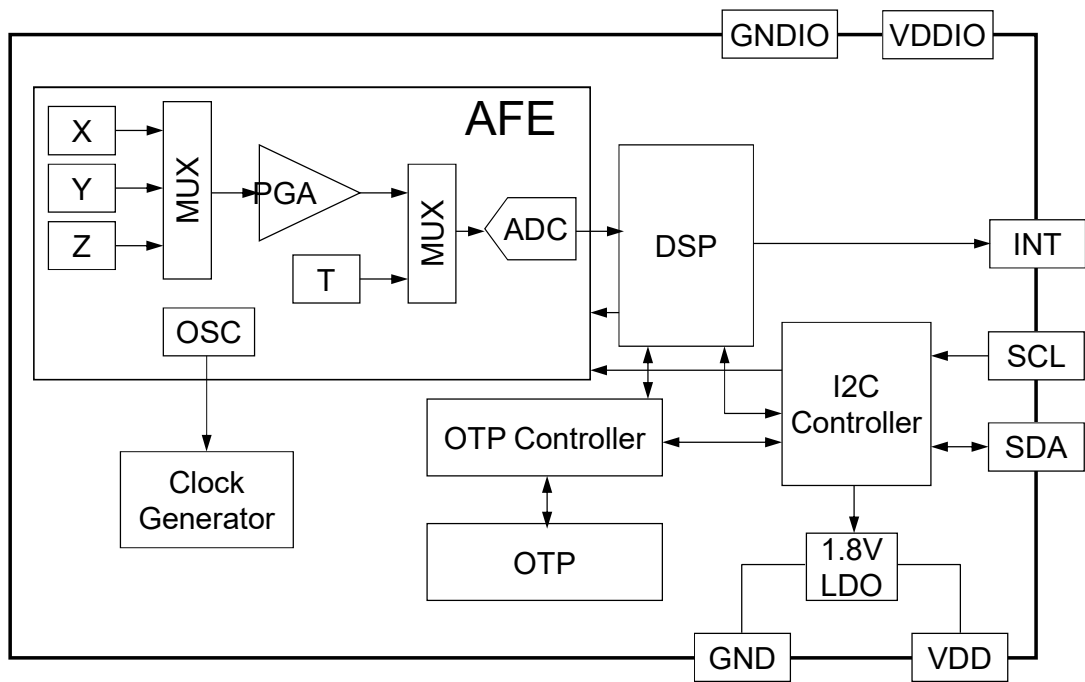


Figure 1: GMA306 Block Diagram

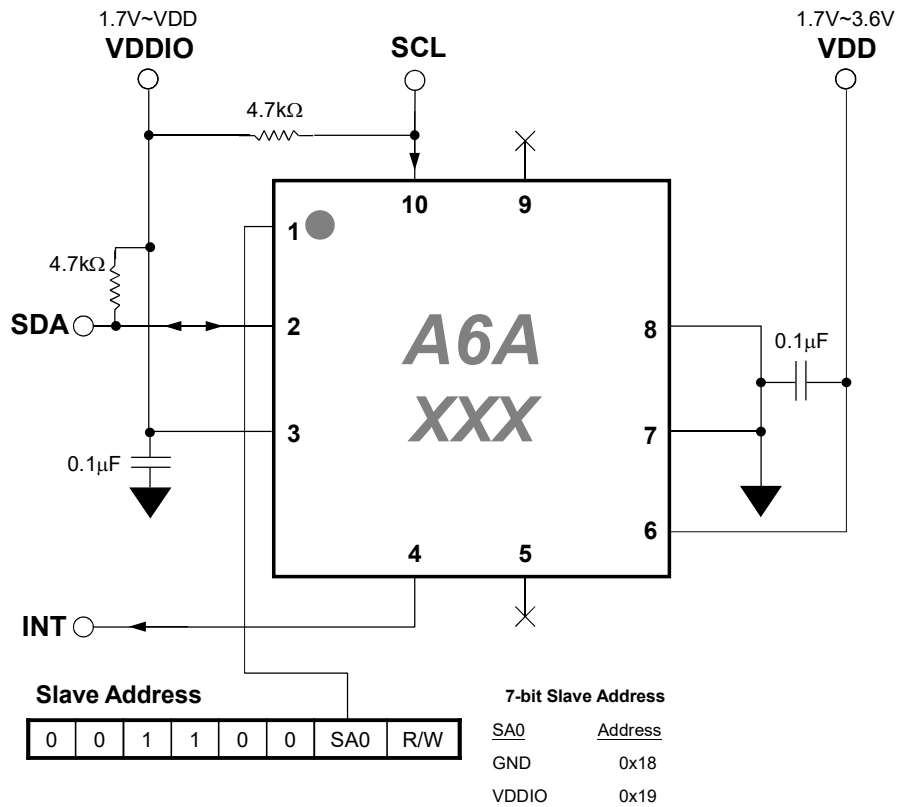


Figure 2: GMA306 I2C Connection Example

General Operation

Power-on reset

GMA306 have a built-in power-on reset (POR) generator. It will reset the core logics and all the registers to default values. There is no limitation on the sequence of switching on the supply voltages of VDD and VDDIO. It is recommended to do a soft reset when VDD and VDDIO are fully applied before the following initialization step. The soft reset can be done by set 1'b1 to RST bit. Please refer to Register 01h[1] for RST bit description.

Initialization

GMA306 will automatically initialize to continuous mode (CM) upon power-up. High-pass filtered acceleration data is available without further setup. Nevertheless the following steps are provided as a reference for further customization. The register description section has more detail information on individual register settings.

- Step1.** Read the Register 00h (PID) for product ID. The PID value should be 0xA3. Check the I2C connections if the report value is otherwise.
- Step2.** Write 0x40 to Register 18h. This will turn on the offset temperature compensation.
- Step3.** Write 0x2A to Register 15h. This will turn on the data ready interrupt and configure the INT pin to active high, push-pull type.
- Step4.** Write 0x09 to Register 16h. This will turn on the internal low-pass filter. Depending on the application, user may set 0x00 to Register 16h to turn it off, or set 0x12 to Register 16h to turn on the high-pass filter instead.
- Step5.** The default power scheme is high resolution scheme. Depending on the need, user may set 0x5F to Register 38h to the low noise scheme, or set 0x9F to 38h to the low power scheme.

Operation Modes

GMA306 provides two operation modes: the continuous mode (CM) and non-continuous mode (NCM). GMA306 will automatically power-up to CM. The CM ODR is fixed at 128Hz. The NCM ODR has options of 1/2/4/8Hz, and can be selected by NCLK bits of Register 17h. To switch between these two modes, follow below steps:

- Switch from CM to NCM: Write the byte sequence 0x02, 0x00, 0x08, 0x00 to Register 02h in one I2C transaction. This will first stop DSP and then enter the non-continuous mode.
- Switch from NCM to CM: Write the byte sequence 0x02, 0x00, 0x04, 0x00 to Register 02h in one I2C transaction. This will first stop DSP and then enter the continuous mode.

Power-Down Modes

There are two power-down modes: the standby and suspend mode. The DSP is stopped at standby mode, but all register are accessible and their values will be kept intact. The suspend mode will cut most of the chip power, so all registers except Register 01h are not accessible and values may be corrupted after leaving the suspend mode. Follow the steps to switch between

power-down and operation modes:

- Switch from operation to standby mode: Write byte sequence 0x02, 0x00 to Register 02h. This will stop DSP to enter the standby mode.
- Switch from standby mode to operation mode: Write byte sequence 0x04, 0x00 to Register 02h to switch to CM, or write byte sequence 0x08, 0x00 to Register 02h to NCM.
- Switch from operation mode to suspend mode: Write 0x05 to Register 01h. This will power down the on-chip LDO and band-gap circuit.
- Switch from suspend mode to operation mode: Write 0x02 to Register 01h. This will power up the on-chip LDO and band-gap circuit, and reset the chip. Do the usual initialization steps after leaving the suspend mode.

Power Schemes for Power-Noise Optimization

GMA306 power scheme can be configured to optimize the trade-off between power and noise. GMA306 provide low power scheme that can be achieved by reducing the oversampling ratio. On the other hand by selecting high oversampling ratio, the noise can be suppressed to improve resolution. GMA306 provides three oversampling ratios of 64/32/16 that can be configured by the Register 38h. Below table summarizes the settings for the three power schemes. Please refer to register description for more details.

Table 4: Power Scheme Settings

| Register 38h | Oversampling Ratio | Power Schemes |
|--------------|--------------------|-----------------|
| 0x1F | 64 | High resolution |
| 0x5F | 32 | Low noise |
| 0x9F | 16 | Low power |

Motion Detection Function

Motion detection is used to detect the event when the acceleration reading from any of three axes exceeds a preset threshold. It can be enabled in both CM and NCM operation modes. Interrupt signal can be enabled as well.

Motion detection works in two favors: normal and differential style. In normal detection style, the acceleration reading is checked against the preset threshold directly. When the reading is larger than the threshold value, motion detection is asserted. On the contrary, the differential detection style compares the difference between the current and the previous reading with the threshold value. The detection is asserted when the *difference* is larger than the threshold.

Below summarizes the steps to use motion detection function. For more information on the mentioned registers, see the respective register description.

Step1. Set the threshold value to Register 03h. The scale factor for the setting is 1 threshold code = 0.25g for X/Y-axis, and 0.5g for Z-axis.

Step2. Select the detection favor between normal and differential styles. For differential style, set 1'b1 to MM_CM or MM_NCM bits of Register 16h for CM and NCM mode respectively. Set 1'b0 to MM_CM or MM_NCM for normal style instead.

Step3. Turn on the motion detection interrupt enable. Set 1'b1 to IMEN_CM or IMEN_NCM of Register 15h for CM and NCM mode respectively.

Auto Wake-up/Sleep

GMA306 can be configured to automatically transit between CM and NCM mode based on the motion detection function. When the system is not used and does not require high sampling rate, a preset timeout put GMA306 in sleep/NCM mode to save precious power. It automatically wake-up to CM/high data-rate mode when motion is detected, which usually implies the system begin being used.

Below summarizes the steps to setup auto wake-up/sleep function. For more information on the mentioned registers, see the respective register description.

Step1. Set the timeout value to TOCT bits of Register 17h. The timeout to auto-transit from NCM/sleep to CM/wake-up mode can be set from 0.5 to 6.0 sec.

Step2. Enable the motion detection function following the steps described in the “Motion Detection Function” section. The motion detection is used to enable transition from NCM to CM, so be sure to turn on the motion detection function at NCM.

Step3. Set 1'b1 to MO_EN bit of Register 16h to enable the auto-transit from NCM to CM.

Step4. Set 1'b1 to TO_EN bit of Register 16h to enable the auto timeout transition from CM to NCM.

Low-/High-pass Filter

GMA306 has built-in low-pass and high-pass filter. Use the low-pass filter to remove high-frequency noise, which is particular useful for static acceleration application like e-Compass tilt compensation. The high-pass filter can be used to eliminate the DC offset and low-frequency disturbance, which is helpful in transient application like motion detection. Below summarizes the steps to setup low-/high pass filter. For more information on the mentioned registers, see the respective register description.

- Low-pass filter:
 - Set 1'b1 to MVE_CM or MVE_NCM of Register 16h to turn on the 4-tap moving average filter for CM and NCM respectively.
 - Set 1'b0 to HP_CM or HP_NCM of Register 16h to turn off the high-pass option and make it low-pass for CM and NCM respectively.
- High-pass filter:
 - Set 1'b1 to MVE_CM or MVE_NCM of Register 16h to turn on the 4-tap moving average filter for CM and NCM respectively.
 - Set 1'b1 to HP_CM or HP_NCM of Register 16h to turn on the high-pass option and make it high-pass for CM and NCM respectively.

User Registers

User Register Map

Table 5: User Register Map Table

| Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Access | Default |
|---------|-------------|-----------|----------|-----------|-----------|---------|----------|----------|--------|---------|
| 00h | PID[7:0] | | | | | | | | R | 0xA3 |
| 01h | Reserved | | | | | PD_BG | RST | PD_LDO | R/W | 0x00 |
| 02h | Reserved | | Not used | | ACTR[3:0] | | | | R/W | 0x00 |
| 03h | Not used | | | MTHR[4:0] | | | | | R/W | 0x01 |
| 04h | STADR[7:0] | | | | | | | | R | 0x0055 |
| | STADR[15:8] | | | | | | | | | |
| 05h | RST_DP | PG_DONE | RD_DONE | OTP_VALID | Motion | CM | DAOW | DRDY | R | NA |
| 06h | DX[6:0] | | | | | | | Not used | R | NA |
| 07h | DX[14:7] | | | | | | | | R | NA |
| 08h | DY[6:0] | | | | | | | Not used | R | NA |
| 09h | DY[14:7] | | | | | | | | R | NA |
| 0Ah | DZ[5:0] | | | | | | Not used | | R | NA |
| 0Bh | DZ[13:6] | | | | | | | | R | NA |
| 0Ch | DT[7:0] | | | | | | | | R | NA |
| 0Dh | DT[15:8] | | | | | | | | R | NA |
| 0E~15h | Reserved | | | | | | | | — | — |
| 15h | Not used | IMEN_NCM | IDEN_NCM | ITYPE_NCM | IPOL | IMEN_CM | IDEN_CM | ITYPE_CM | R/W | 0x4C |
| 16h | MO_EN | TO_EN | MM_NCM | HP_NCM | MVE_NCM | MM_CM | HP_CM | MVE_CM | R/W | 0x1B |
| 17h | Reserved | TOCT[2:0] | | | NCLK[1:0] | | Reserved | | R/W | 0xF0 |
| 18h | OFFSEL[1:0] | | Reserved | | MACT[3:0] | | | | R/W | 0x00 |
| 19~37h | Reserved | | | | | | | | — | — |
| 38h | OSM[1:0] | | Reserved | | | | | | R/W | 0x1F |
| 39~3Ch | Reserved | | | | | | | | — | — |

Description of Registers

Register 00h: Product identification

| Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Access | Default |
|---------|----------|------|------|------|------|------|------|------|--------|---------|
| 00h | PID[7:0] | | | | | | | | R | 0xA3 |

The register contains the GMA306 product identification code. Always read to be 0xA3.

Register 01h: Power down control

| Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Access | Default |
|---------|----------|------|------|------|------|-------|------|--------|--------|---------|
| 01h | Reserved | | | | | PD_BG | RST | PD_LDO | R/W | 0x00 |

PD_BG and PD_LDO bits manage the on-chip power. When set to 1'b1, the band-gap and LDO will be shut down respectively. All registers values except 01h are lost.

RST is used to reset the chip. When set to 1'b1, core logics will be reset and registers values will return to the default values.

Register 02h: Action register

| Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Access | Default |
|---------|----------|------|----------|------|-----------|------|------|------|--------|---------|
| 02h | Reserved | | Not used | | ACTR[3:0] | | | | R/W | 0x00 |

1'b1 bit set to the ACTR[3:0] bits will trigger the following actions respectively:

| Bit Set | Action |
|---------|---------------------------|
| ACTR[0] | Reset DSP and AFE |
| ACTR[1] | Stop DSP |
| ACTR[2] | Enter continuous mode |
| ACTR[3] | Enter non-continuous mode |

Register 03h: Motion threshold

| Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Access | Default |
|---------|----------|------|------|-----------|------|------|------|------|--------|---------|
| 03h | Not used | | | MTHR[4:0] | | | | | R/W | 0x01 |

MTHR[4:0] is used to set the threshold for the built-in motion detect function. The scale factor for the setting is 1 threshold code = 0.25g for X/Y-axis and 0.5g for Z-axis. Thus the full range of the threshold setting is from 0.25 to 7.75g for X/Y-axis and 0.5 to 15.5g for Z-axis.

Register 04h: Start register for data reading

| Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Access | Default |
|---------|-------------|------|------|------|------|------|------|------|--------|---------|
| 04h | STADR[7:0] | | | | | | | | R | 0x0055 |
| | STADR[15:8] | | | | | | | | | |

For sensor data output, users should read 11 bytes starting from 04h register (STADR) to 0Dh

in one I2C transaction. Note the register has 2-byte word length and its value is fixed to 0x0055. When the I2C data read reach 0Dh, the I2C address pointer will automatically rewind to this start register.

Register 05h: Status register

| Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Access | Default |
|---------|--------|---------|---------|-----------|--------|------|------|------|--------|---------|
| 05h | RST_DP | PG_DONE | RD_DONE | OTP_VALID | Motion | CM | DAOW | DRDY | R | NA |

The status register indicates the interrupt and DSP status. The register value will be cleared after reading data by the procedure described in the Register 04h section. Descriptions when the bit is set are summarized below.

- RST_DP: DSP is stopped
- PG_DONE: programming OTP data is completed
- RD_DONE: loading OTP data to DSP is completed
- OTP_VALID: OTP data is valid when loading OTP to DSP
- Motion: motion interrupt is asserted
- CM: DSP is in continuous mode. Otherwise DSP is in the non-continuous mode.
- DAOW: data has been over-written before read. Otherwise data has not been over-written.
- DRDY: interrupt asserted by new data arrival

Register 06h~0Dh: Data registers

| Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Access | Default |
|---------|----------|------|------|------|------|------|----------|----------|--------|---------|
| 06h | DX[6:0] | | | | | | | Not used | R | NA |
| 07h | DX[14:7] | | | | | | | | R | NA |
| 08h | DY[6:0] | | | | | | | Not used | R | NA |
| 09h | DY[14:7] | | | | | | | | R | NA |
| 0Ah | DZ[5:0] | | | | | | Not used | | R | NA |
| 0Bh | DZ[13:6] | | | | | | | | R | NA |
| 0Ch | DT[7:0] | | | | | | | | R | NA |
| 0Dh | DT[15:8] | | | | | | | | R | NA |

The XY data output is encoded to a 15-bit value and stored across two bytes. Data representation is 2's complement, i.e. MSB (bit 14) is the sign bit with 1'b1 representing negative value.

The Z data output is encoded to a 14-bit value and stored across two bytes. Data representation is 2's complement, i.e. MSB (bit 13) is the sign bit with 1'b1 representing negative value.

The acceleration sensing has dynamic range of $\pm 16g$ with sensitivity of 256 LSB/g for the X/Y-axis and 64 LSB/g for the Z axis. The central value (0x00) stands for 0g.

The temperature sensor has sensitivity of 0.5 LSB/°C. The central value (0x00) stands for 25°C.

Typical acceleration reading when GMA306 is stationary under gravitational field is summarized in the following table and Figure.

| Orientation | X | Y | Z |
|---------------|------|------|-----|
| Orientation 1 | +256 | 0 | 0 |
| Orientation 2 | 0 | +256 | 0 |
| Orientation 3 | -256 | 0 | 0 |
| Orientation 4 | 0 | -256 | 0 |
| Orientation 5 | 0 | 0 | -64 |
| Orientation 6 | 0 | 0 | +64 |

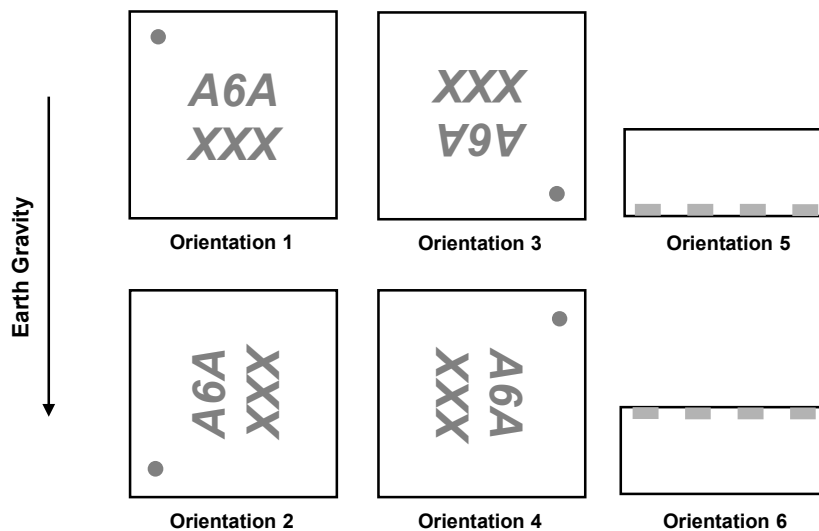


Figure 3: Typical stationary reading in gravity field

Register 15h: Interrupt configuration register

| Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Access | Default |
|---------|----------|----------|----------|-----------|------|---------|---------|----------|--------|---------|
| 15h | Not used | IMEN_NCM | IDEN_NCM | ITYPE_NCM | IPOL | IMEN_CM | IDEN_CM | ITYPE_CM | R/W | 0x4C |

The register configures the interrupt control.

- IPOL: control the polarity for the interrupt pin output. Set to 1'b1 for active high and to 1'b0 for active low.
- The other control bits are divided into two groups. Control bits end with _NCM control the designated features of NCM (non-continuous mode); while bits end with _CM control those of CM (continuous mode). The common designated features are described below.
 - IMEN: interrupt enable for motion detection. Set to 1'b0 to disable motion interrupt; Set to 1'b1 to enable motion interrupt.
 - IDEN: interrupt enable for data ready. Set to 1'b0 to disable data ready interrupt; Set

to 1'b1 to enable data ready interrupt.

- ITYPE: interrupt push-pull/open drain selection. 1'b0 for push-pull; 1'b1 for open drain.

Register 16h: Control register 1

| Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Access | Default |
|---------|-------|-------|--------|--------|---------|-------|-------|--------|--------|---------|
| 16h | MO_EN | TO_EN | MM_NCM | HP_NCM | MVE_NCM | MM_CM | HP_CM | MVE_CM | R/W | 0x1B |

The register controls the DSP configuration.

- MO_EN: enable the motion transition from NCM to CM.
- TO_EN: enable the timeout auto-transition from CM to NCM
- The other control bits are divided into two groups. Control bits end with _NCM control the designated features of NCM (non-continuous mode); while bits end with _CM control those of CM (continuous mode). The common designated features are described below.
 - MM: enable motion detection to the normal/differential mode. Set to 1'b0 to the normal motion detection mode, or to 1'b1 to the differential mode.
 - HP: enable the high pass filter. Set to 1'b0 to disable and set to 1'b1 to enable the high-pass filter.
 - MVE: enable the 4-tap moving average. Set to 1'b0 to disable and set to 1'b1 to enable the low-pass filter.

Register 17h: Control register 2

| Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Access | Default |
|---------|----------|-----------|------|------|-----------|------|----------|------|--------|---------|
| 17h | Reserved | TOCT[2:0] | | | NCLK[1:0] | | Reserved | | R/W | 0xF0 |

TOCT[2:0] is used to set the timeout value for auto-transition from NCM to CM. The timeout values for TOCT setting are summarized below:

| TOCT[2:0] | Timeout (Sec) |
|-----------|---------------|
| 3'b000 | 0 |
| 3'b001 | 0 |
| 3'b010 | 0.5 |
| 3'b011 | 1.0 |
| 3'b100 | 1.5 |
| 3'b101 | 2.0 |
| 3'b110 | 2.5 |
| 3'b111 | 3.0 |

NCLK[1:0] is used to set the ODR in NCM mode as shown in the following:

| NCLK[1:0] | Description |
|-----------|--------------|
| 2'b00 | 1 Hz NCM ODR |
| 2'b01 | 2 Hz NCM ODR |

| | |
|-------|--------------|
| 2'b10 | 4 Hz NCM ODR |
| 2'b11 | 8 Hz NCM ODR |

Register 18h: Control register 3

| Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Access | Default |
|---------|-------------|------|----------|------|-----------|------|------|------|--------|---------|
| 18h | OFFSEL[1:0] | | Reserved | | MACT[3:0] | | | | R/W | 0x00 |

OFFSEL[1:0] is used to control the offset temperature compensation.

| OFFSEL[1:0] | Description |
|-------------|--|
| 2'b00 | Turn off offset temperature compensation |
| 2'b01 | Turn on offset temperature compensation |
| others | reserved |

1'b1 bit set to the MACT[3:0] bits will trigger the following actions respectively:

| Bit Set | Action |
|---------|----------------------------|
| MACT[0] | Download OTP data into DSP |
| MACT[1] | Reserved |
| MACT[2] | Reserved |
| MACT[3] | Initialize oscillator |

Register 38h: Oversampling mode register

| Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Access | Default |
|---------|----------|------|----------|------|------|------|------|------|--------|---------|
| 38h | OSM[1:0] | | Reserved | | | | | | R/W | 0x1F |

OSM[1:0] selects which oversampling mode is to be used shown in the following Table. The output data rate is always 128Hz for continuous mode (CM). For non-continuous mode (NCM), the output data rate can be set to 1/2/4/8Hz, see Register 17h description for details.

| OSM[1:0] | Oversampling Ratio | Power Scheme |
|----------|--------------------|-----------------|
| 2'b00 | 64 | High resolution |
| 2'b01 | 32 | Low noise |
| 2'b10 | 16 | Low power |
| 2'b11 | Reserved | — |

Digital Interface

I2C Interface General Description

The I2C interface is compliant with fast mode (400kHz) and normal mode (100 kHz) I2C standard. The 7-bit device slave address can be selected from 0x18 or 0x19 by setting pin SA0 to GND or VDDIO respectively.

The I2C bus takes master clock through SCL pin and exchanges serial data via SDA. SDA is a bidirectional (input/output) connection. Both are open-drain connection and must be connected externally to VDDIO via a pull-up resistor.

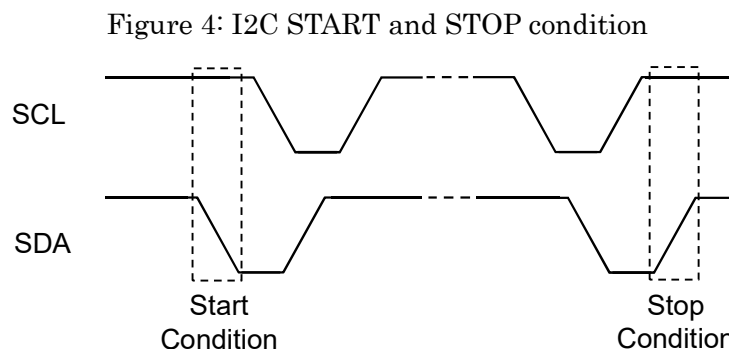
The I2C interface supports multiple read and write. When using multiple read/write, generally the internal I2C address pointer will automatically increase by 1 for the next access. But exceptions to this general rule are highlighted in the following table. For example, a multiple write to 01h (ACTR) will write multiple bytes sequence to 01h. This will make state transition easily.

| Multiple R/W | Current Address | Next Address |
|----------------|-----------------|--------------|
| Multiple Write | 01h | 01h |
| Multiple Write | 02h | 02h |
| Multiple Read | 0Dh | 04h |
| Multiple Write | 18h | 18h |

I2C Access Format

One data bit is transferred for each SCL cycle. The SDA must not change level when the SCL is high. The level changes in SDA while SCL is high are reserved control signals. The SDA and SCL remain high when I2C bus is idle.

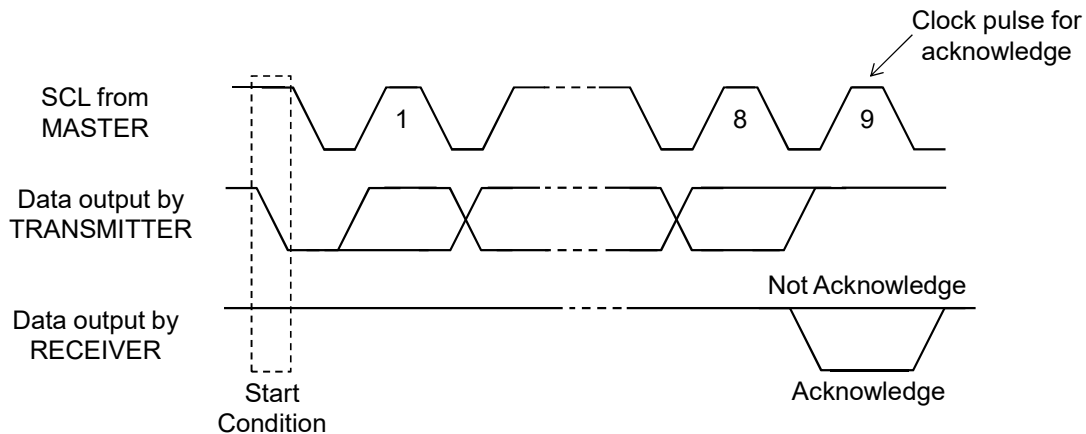
Data transfer begins by bus master indicating a start condition (ST) of a falling edge on SDA when SCL is high. The master terminates transmission and frees the bus by issuing a STOP condition (SP). Stop condition is a rising edge on SDA while SCL is high. The bus remains active if a repeated START (SR) condition is generated instead of a STOP condition. Figure 4 illustrates the START and STOP condition.



After a start condition (ST), the 7-bit slave address + RW bit must be sent by master. If the slave address does not match with GMA306, there is no acknowledge and the following data

transfer will not affect GMA306. If the slave address corresponds to GMA306, it will acknowledge by pulling SDA to low and the SDA line should be let free by bus master to enable the data transfer. The master should let the SDA high (no pull down) and generate a high SCL pulse for GMA306 acknowledge. Figure 5 illustrates the acknowledge signal sequence.

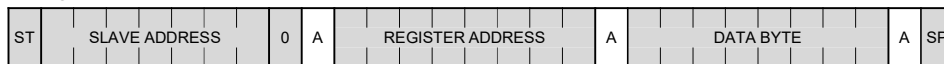
Figure 5: Acknowledge signal sequence



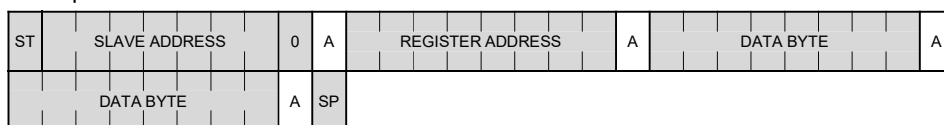
A write to GMA306 includes transmission of a START condition, the slave address with R/W bit=1'b0, one byte of data to specify the register address to write, subsequent one or more bytes of data, and finally a STOP condition. “Single Write” and “Multiple Write” in Figure 6 illustrates the frame format of single and multiple write to GMA306 respectively.

Figure 6: I2C access format

Single Write



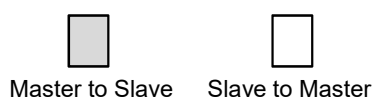
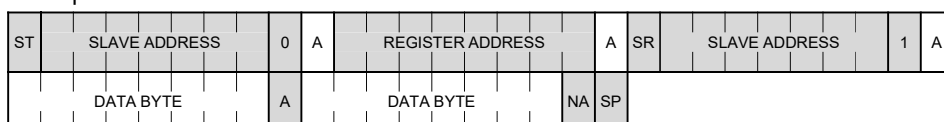
Multiple Write



Single Read



Multiple Read



A = acknowledge
 NA = not acknowledge
 ST = START condition
 SR = repeated START condition
 SP = STOP condition

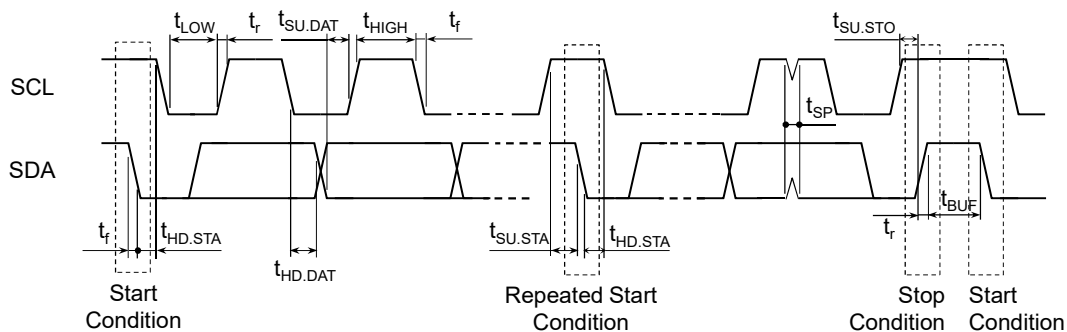
A read from GMA306 starts with transmission of a START condition, the slave address with R/W bit=1'b0, and one byte of data to specify the register address to read. A repeated START condition and the slave address with R/W bit=1'b1 are transmitted subsequently. The slave address with R/W bit=1'b1 initiates a read operation. GMA306 acknowledge receipt of the read operation command by pulling SDA low during the 9th SCL clock and begin transmitting the contents starting from the specified register address. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and the STOP condition. “Single Read” and “Multiple Read” in Figure 6 illustrates the frame format for reading single or multiple byte from GMA306.

I2C Specifications

Table 6: I2C Timing Specification

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|-----------------------|--------------|---------|---------|---------|---------|
| SCL clock frequency | f_{SCL} | — | — | 400 | kHz |
| Clock low period | t_{LOW} | 1.3 | — | — | μs |
| Clock high period | t_{HIGH} | 0.6 | — | — | μs |
| Bus free to new start | t_{BUF} | 1.3 | — | — | μs |
| Start hold time | $t_{HD.STA}$ | 0.6 | — | — | μs |
| Start setup time | $t_{SU.STA}$ | 0.6 | — | — | μs |
| Data-in hold time | $t_{HD.DAT}$ | 0 | — | — | μs |
| Data-in setup time | $t_{SU.DAT}$ | 100 | — | — | ns |
| Stop setup time | $t_{SU.STO}$ | 0.6 | — | — | μs |
| Rise time | t_r | — | — | 0.3 | μs |
| Fall time | t_f | — | — | 0.3 | μs |
| Spike width | t_{SP} | — | — | 50 | μs |

Figure 7: I2C Timing Diagram



Package

Outline Dimension

Unit: mm

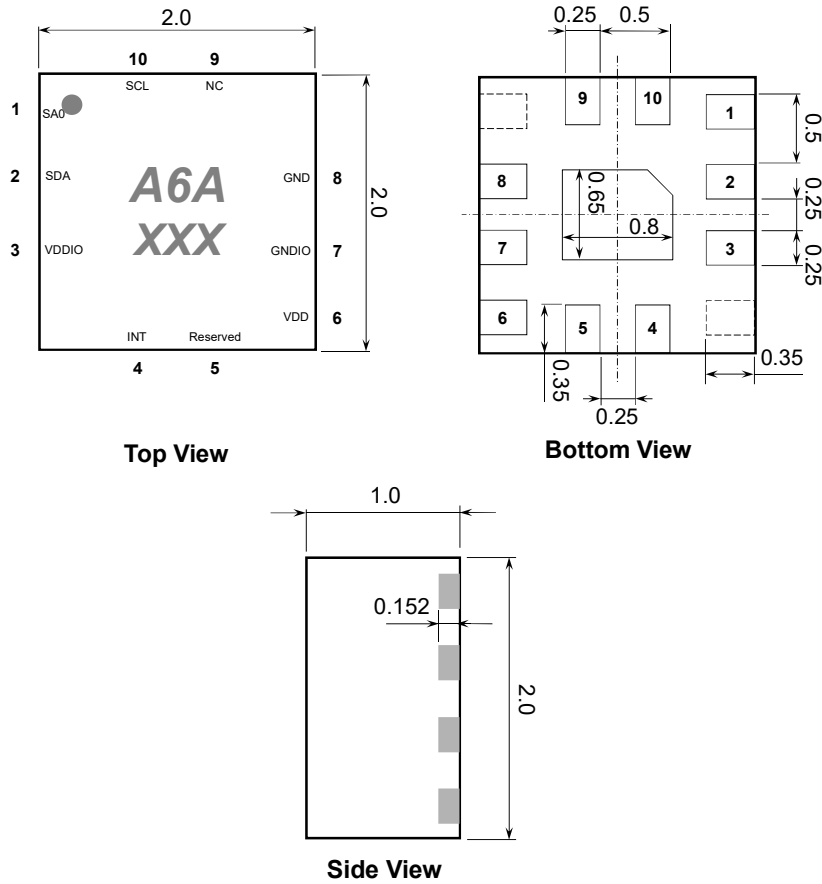


Figure 8: Package Outline Dimension

Axes Orientation

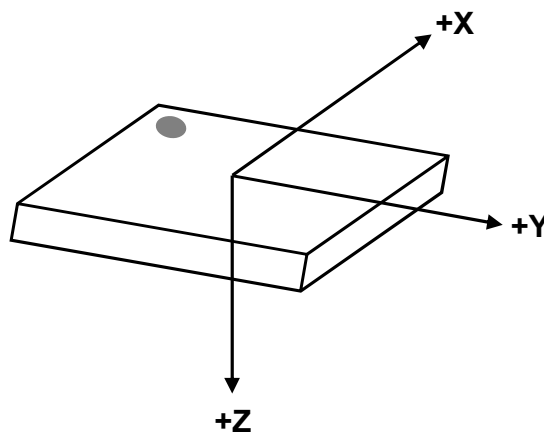


Figure 9: GMA306 Axes Orientation

RoHS Compliance

GMEMS QFN sensors are compliant with Restrictions on Hazardous Substances (RoHS), having halide-free molding compound (green) and lead-free terminations. Reflow profiles applicable to those processes can be used successfully for soldering the devices.

Surface Mounting Information

The accelerometer is a delicate device that is sensitive to the mechanical and thermal stress. Proper PCB board design and well-executed soldering processes are crucial to ensure consistent performance. A recommended land pad layout can be found in the below Figure.

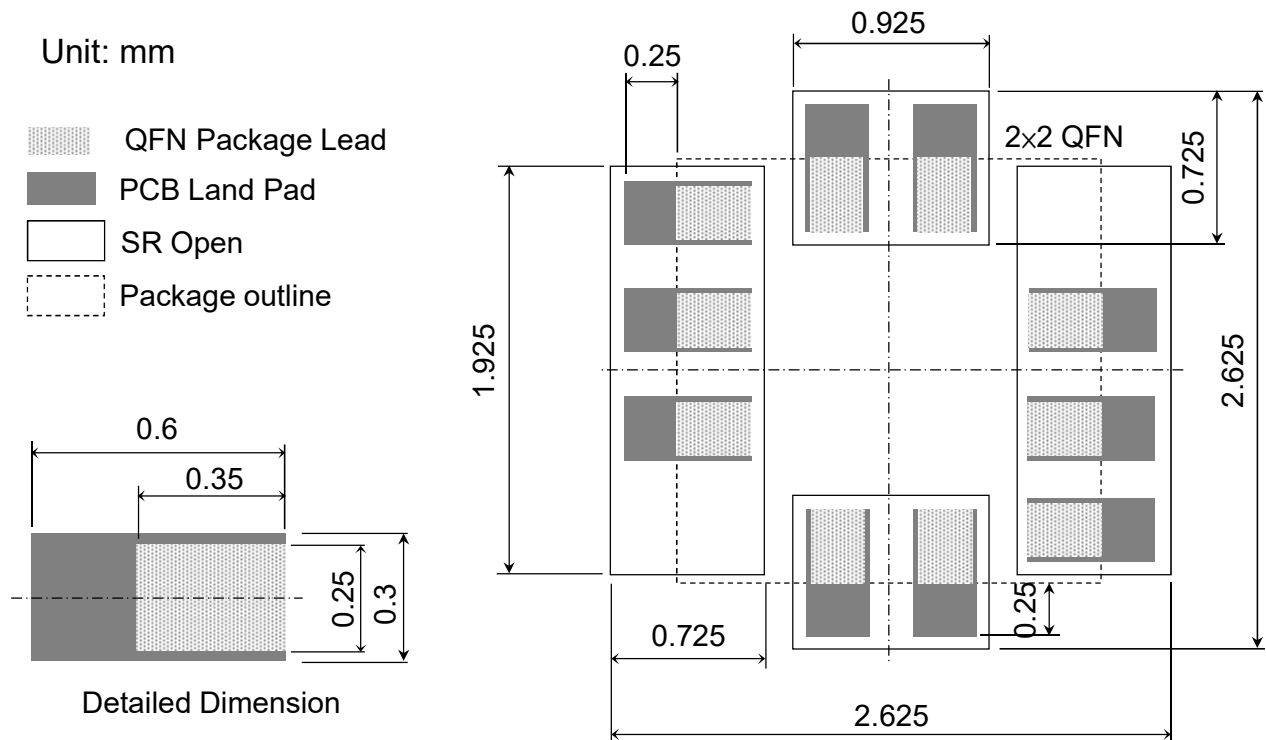


Figure 10: Layout Recommendation for PCB Land Pad

Moisture Sensitivity Level

GMA306 package MSL rating is Level 3.

Tape Specification

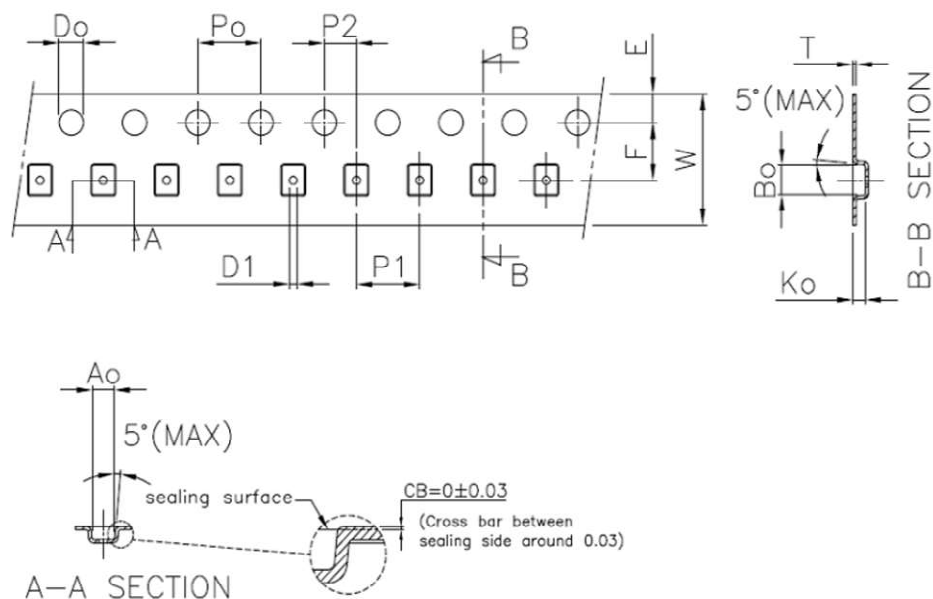


Figure 11: Tape Outline Drawing

Table 7: Tape Dimension

| Symbol | Dimension (mm) |
|--------|------------------|
| A_0 | 2.25 ± 0.1 |
| B_0 | 2.25 ± 0.1 |
| K_0 | 1.3 ± 0.1 |
| P_0 | 4.0 ± 0.1 |
| P_1 | 8.0 ± 0.1 |
| P_2 | 2.0 ± 0.05 |
| T | 0.3 ± 0.03 |
| E | 1.75 ± 0.1 |
| F | 5.5 ± 0.05 |
| D_0 | $1.5 + 0.1 / -0$ |
| D_1 | 1.0 |
| W | 12.0 ± 0.3 |

Document History and Modification

| Revision No. | Description | Date |
|--------------|-----------------------------------|------------|
| V0.1 | First release for customer review | 2016/11/16 |
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