

# GMFPC101 Digital Force Sensor

## General Introduction

GMFPC101 is a digital force sensor especially designed for consumer applications like touch panels, seamless buttons, styluses, and smart shoes. It is assembled on an FPC with a thickness less than 0.4mm. The force sensor is based on the industry-recognized piezo-resistive technology featuring long-term stability and EMC robustness. A high-performance 24-bit ADC provides extra fine force resolution up to 0.1mN. The force sensor is capable of measuring forces up to 10N.

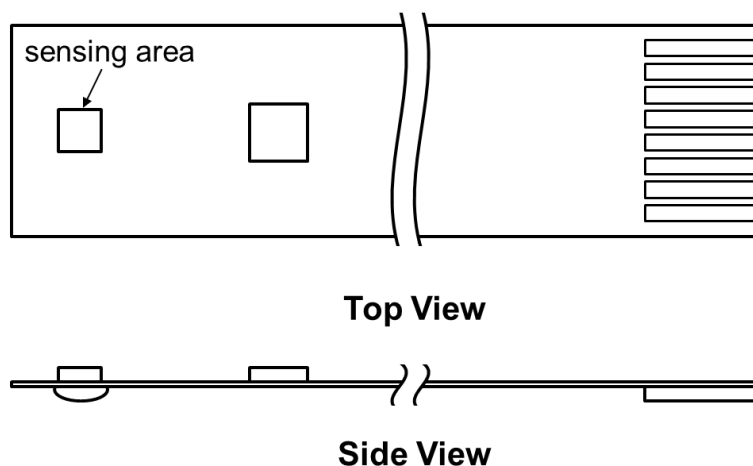
Focusing on micro force (less than 1N) measurement, the high sensitivity, and the high resolution makes GMFPC101 especially suitable for applications that detect forces of delicate hand related movement such as finger taps or pen drawing.

## Features

- Operation range:
  - Force: 0~10N
  - Temperature: -40~+85°C
- Built-in 24-bit ADC:
  - Force resolution: up to 0.1mN
- Digital interface:
  - I2C supporting both standard (100kHz), and fast (400kHz) mode
  - SPI 3-/4-wire, up to 10MHz clock
- Supply voltage:
  - VDD: +1.8V ~ +3.6V
  - VID: +1.2V ~ +3.6V
- Power Consumption:
  - Standby ~ 1uA
- RoHS-compliance package:
  - FPC package
  - FPC size: 30 × 4.5 mm<sup>2</sup>
  - Height: 0.65±0.1 mm.

## Applications

Force buttons, active styluses, digital pianos, gaming, robotic end-effectors, and insoles of smart shoes



## Specifications

Table 1: Pin Descriptions

| Pin# | Name    | Description   |
|------|---------|---|
| 1    | GND     | Ground pin  |
| 2    | SDO     | I2C slave address select pin<br>SPI data output pin |
| 3    | SCK/SCL | I2C/SPI clock pin                                   |
| 4    | SDI/SDA | I2C data I/O pin<br>SPI data input pin              |
| 5    | CSB     | SPI chip select                                     |
| 6    | NC      | No connection inside                                |
| 7    | VID     | Digital interface power supply in                   |
| 8    | VDD     | Core circuit power supply in                        |

Table 2: Specification

| Parameter   | Symbol | Condition                           | Min. | Typ.   | Max. | Unit  |
|---|--------|-------------------------------------|------|--|------|-------|
| Operation voltage   | VDD    |                                     | 1.8  | —  | 3.6  | V     |
| IO voltage  | VID    |                                     | 1.2  | —  | VDD  | V     |
| Temperature range   | Ta     |                                     | -40  | 25   | +85  | °C    |
| Force range   | F      |                                     | 0    | —  | 10   | N     |
| Operation current<br>OSR=256<br><b><u>OSR=1024(default)</u></b><br>OSR=4096<br>OSR=16384<br>OSR=32768 | IDD    | VDD = 3.3V,<br>20Hz,<br>forced mode | —    | 97<br><b><u>120</u></b><br>190<br>420<br>800 | —    | uA    |
| Standby current   | IDDSD  | After POR or<br>soft reset          | —    | 1  | —    | uA    |
| Full scale span   | FS     |                                     |      | 5,000,000                                    |      | LSB   |
| Zero offset   |        |                                     |      | 11,000                                       |      | LSB   |
| Sensitivity   |        |                                     | —    | 500,000                                      | —    | LSB/N |
| Linearity <sup>1</sup>  |        |                                     |      | ±1   |      | %FS   |
| Noise (RMS)   |        |                                     |      | 100  |      | LSB   |

1. Calibration is required.

Table 3: Absolute Maximum Rating

| Parameter            | Symbol   | Min. | Max.          | Unit |
|----------------------|----------|------|---------------|------|
| Power supply voltage | VDD, VID | -0.3 | 6.5           | V    |
| Signal input voltage | VIS      | -0.3 | VDD/VID + 0.3 | V    |
| Overload force       | FMAX     | 0    | 20            | N    |
| Storage temperature  | TST      | -40  | +125          | °C   |
| ESD                  | HBM      | —    | ±2            | kV   |

## Block Diagram and Connection

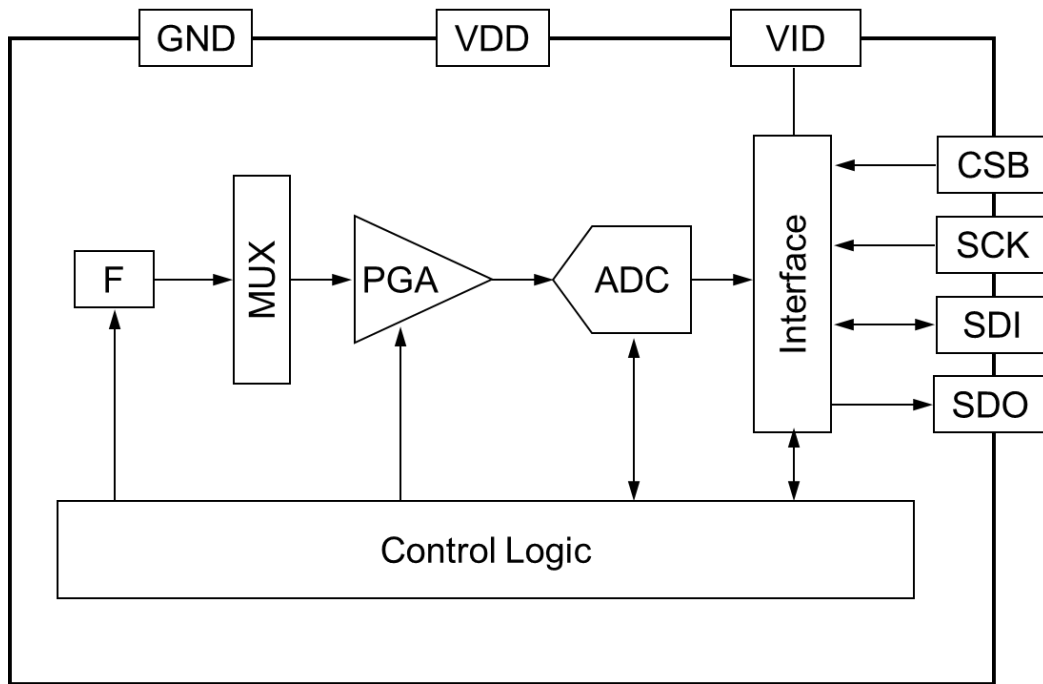


Figure 1: GMFPC101 Block Diagram

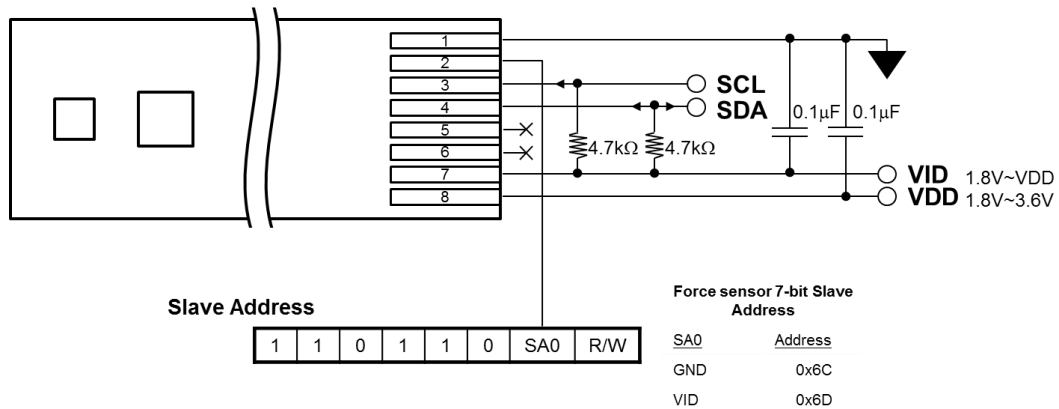


Figure 2: GMFPC101 I2C Connection Example

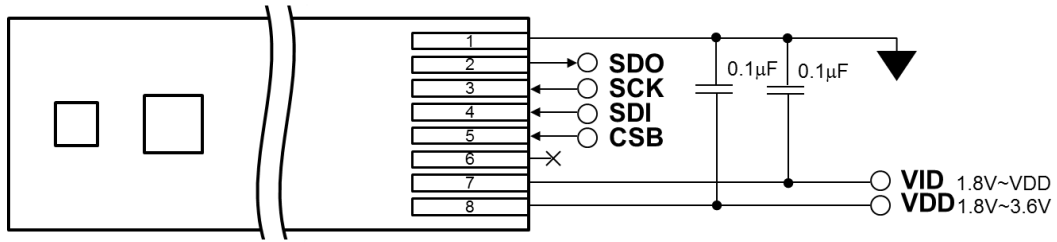


Figure 3: GMFPC101 SPI 4-Wire Connection Example

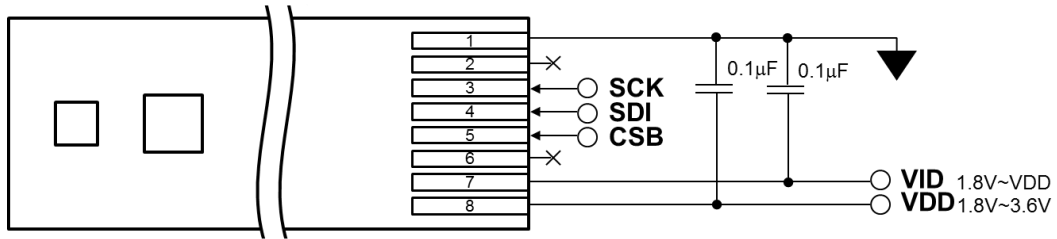


Figure 4: GMFPC101 SPI 3-Wire Connection Example

## Functional Description

### Power Management

GMFPC101 has two separate power supply pins: VDD and VID. VDD is the major power supply pin for all internal analog and digital functional blocks. VID provides a reference voltage level for the digital interface.

When the power is set on, power-on reset (POR) circuit will be active to reset the internal circuits and registers. After the POR sequence, all registers will be initialized to the default values and GMFPC101 will transit to standby mode.

### Reset Functions

GMFPC101 has two types of reset as summarized below:

- Power-on reset (POR): as described in the previous Power Management section.
- Soft reset: Set RESET register (00h) to 0x24 will trigger the device soft reset by resetting all register to default values.

### Initialization

GMFPC101 will automatically initialize to standby mode upon power-up after POR. It is recommended to set RESET register (00h) to 0x24 for device soft reset for initialization.

### Power Modes

GMFPC101 offers two power modes, standby and Forced mode, by setting the 30h[3:0] (Measure\_CTRL[3:0]) bits, see 30h register description for more detail.

The transitions between different modes are illustrated in Figure 5.

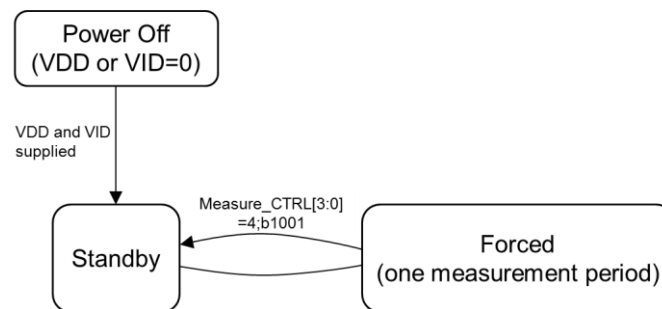


Figure 5: Mode transactions diagram

- Standby mode

GMFPC101 will enter standby mode after complete POR sequence. In this mode, data measurement stops and the power consumption is at the minimum. All registers, including PID and calibration parameters, are accessible.

- Forced mode

In the Forced mode, GMFPC101 will take one-time force measurement and returns to standby

mode automatically. The measurement results can then be obtained from the force data registers. Users need to set to the Forced mode again to have another force measurement. The timing diagram of the Forced mode is illustrated in the following Figure 6.

Before set to the Forced mode, make sure the A5h[1] (Raw) bit value is 1'b1 in order to have the raw force ADC output. Below summarized the single shot pressure conversion steps:

1. Make sure A5h[1] (Raw) is set. If not, set A5h = 0x02.
2. Set to the Forced mode by set 30h = 0x09.
3. Check 02h[0] (DRDY) bit and wait until its value is set. The data is available in the registers when DRDY = 1'b1.
4. Read the raw force ADC output from the force data registers (06h~08h).

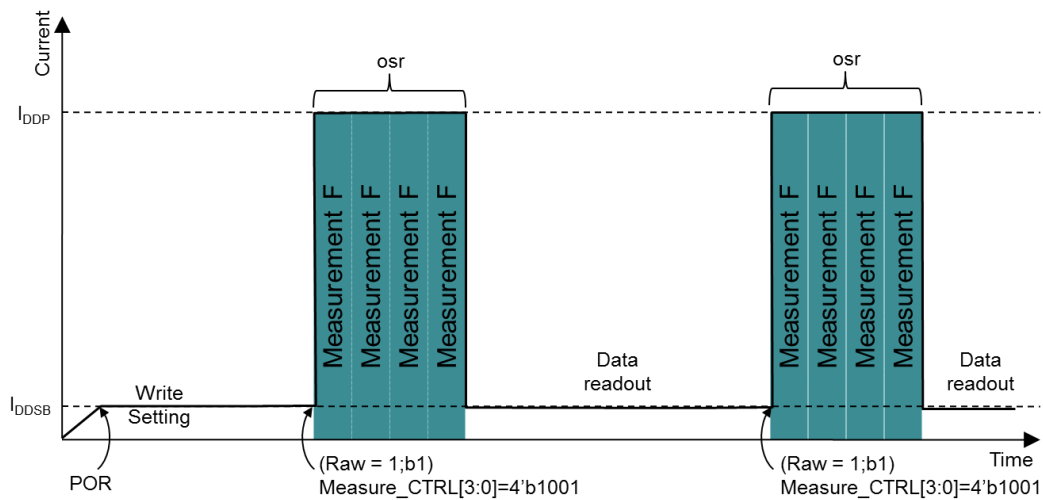


Figure 6: Forced mode timing diagram

## User Register Map

Table 4: User Register Map Table

| Addr. | Name    | bit7          | bit6  | bit5 | bit4 | bit3              | bit2     | bit1  | bit0  | Access | Default |
|-------|---------|---------------|-------|------|------|-------------------|----------|-------|-------|--------|---------|
| 00h   | RESET   | SPI4W         | R'ved | RST  | 0    | 0                 | RST      | R'ved | SPI4W | RW     | 0x00    |
| 01h   | PID     | PID[7:0]      |       |      |      |                   |          |       |       | R      | 0x00    |
| 02h   | STATUS  | Reserved      |       |      |      | 0                 | 0        | 0     | DRDY  | R      | NA      |
| 06h   | FORCEH  | Force [23:16] |       |      |      |                   |          |       |       | R      | NA      |
| 07h   | FORCEM  | Force [15:8]  |       |      |      |                   |          |       |       | R      | NA      |
| 08h   | FORCEL  | Force [7:0]   |       |      |      |                   |          |       |       | R      | NA      |
| 30h   | CMD     | Reserved      |       |      |      | Measure_CTRL[3:0] |          |       |       | RW     | 0x00    |
| A5h   | CONFIG1 | Reserved      |       |      |      |                   |          | Raw   | R'ved | RW     | 0x00    |
| A6h   | CONFIG2 | Reserved      |       |      |      |                   | OSR[2:0] |       |       | RW     | 0x00    |



## Description of Registers

### Register 00h: RESET Register

| Addr. | Name  | bit7  | bit6  | bit5 | bit4 | bit3 | bit2 | bit1  | bit0  | Access | Default |
|-------|-------|-------|-------|------|------|------|------|-------|-------|--------|---------|
| 00h   | RESET | SPI4W | R'ved | RST  | 0    | 0    | RST  | R'ved | SPI4W | RW     | 0x00    |

Set RESET register (00h) to 0x24 to trigger the device soft reset. All register values will be reset to default. The RST bits will automatically return to 1'b0 when the soft reset complete.

SPI4W bits control the 3-/4-wire SPI selection. Default 0x00 is 3-wire SPI interface. Set 0x81 to RESET register (00h) will switch to the 4-wire SPI.

### Register 01h: PID Register

| Addr. | Name | bit7     | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Access | Default |
|-------|------|----------|------|------|------|------|------|------|------|--------|---------|
| 01h   | PID  | PID[7:0] |      |      |      |      |      |      |      | R      | 0x00    |

PID is the product identification register and the value is fixed to 0x00. This register is available for reading after the device finished the power-on-reset.

### Register 02h: STATUS Register

| Addr. | Name   | bit7     | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Access | Default |
|-------|--------|----------|------|------|------|------|------|------|------|--------|---------|
| 02h   | STATUS | Reserved |      |      |      | 0    | 0    | 0    | DRDY | R      | NA      |

The DRDY bit will be set once the data conversion is complete. The output data is ready for reading from force data registers.

### Register 06h~08h: Force Data Registers

| Addr. | Name   | bit7          | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Access | Default |
|-------|--------|---------------|------|------|------|------|------|------|------|--------|---------|
| 06h   | FORCEH | Force [23:16] |      |      |      |      |      |      |      | R      | NA      |
| 07h   | FORCEM | Force [15:8]  |      |      |      |      |      |      |      | R      | NA      |
| 08h   | FORCEL | Force [7:0]   |      |      |      |      |      |      |      | R      | NA      |

The force data output is encoded to a 24-bit value and stored across three bytes. Data representation is 2's complement, i.e. MSB (bit 23) is the sign bit with 1'b1 representing negative value.

The force data output is raw force sensor ADC value.

## Register 30h: CMD Register

| Addr. | Name | bit7     | bit6 | bit5 | bit4 | bit3              | bit2 | bit1 | bit0 | Access | Default |
|-------|------|----------|------|------|------|-------------------|------|------|------|--------|---------|
| 30h   | CMD  | Reserved |      |      |      | Measure_CTRL[3:0] |      |      |      | RW     | NA      |

Measure\_CTRL[3:0] control the signal conversion mode. After each single shot signal conversion, GMFPC101 will return to standby mode. Available setting is summarized in the following table.

| Measure_CTRL[3:0] | Power Mode   |
|-------------------|--|
| 4'b1001           | Forced mode<br>Make a single shot force conversion |
| Others            | Reserved   |

## Register A5h: CONFIG1 Register

| Addr. | Name    | bit7     | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Access | Default |
|-------|---------|----------|------|------|------|------|------|------|------|--------|---------|
| A5h   | CONFIG1 | Reserved |      |      |      |      |      | Raw  | 0    | RW     | 0x00    |

Set Raw = 1'b1 before making a single shot force conversion. This will output raw force ADC value to the force data registers (06h~08h).

## Register A6h: CONFIG2 Register

| Addr. | Name    | bit7     | bit6 | bit5 | bit4 | bit3 | bit2     | bit1 | bit0 | Access | Default |
|-------|---------|----------|------|------|------|------|----------|------|------|--------|---------|
| A6h   | CONFIG2 | Reserved |      |      |      |      | OSR[2:0] |      |      | RW     | 0x00    |

OSR[2:0] selects the oversampling ratio for the force data conversion as summarized in the following table.

| OSR[2:0] | Conversion Time (ms) | Oversampling Ratio | Typical Resolution (ENOB) |
|----------|----------------------|--------------------|---------------------------|
| 3'b000   | 2.5                  | 1024               | 17.8                      |
| 3'b001   | 3.78                 | 2048               | 18.2                      |
| 3'b010   | 6.34                 | 4096               | 18.7                      |
| 3'b011   | 11.46                | 8192               | 19.1                      |
| 3'b100   | 1.54                 | 256                | 17                        |
| 3'b101   | 1.86                 | 512                | 17.3                      |
| 3'b110   | 21.7                 | 16384              | 19.4                      |
| 3'b111   | 42.18                | 32768              | 19.7                      |

## Digital Interface: I2C

### I2C Interface General Description

The I2C interface is compliant with standard and fast I2C standard. The devices support the 7-bit control functions and SDA and SCL facilitate communication between GMFPC101 and master with clock rate up to 400kHz.

The 7-bit device slave address can be selected by the SA0 pin as summarized in the below table.

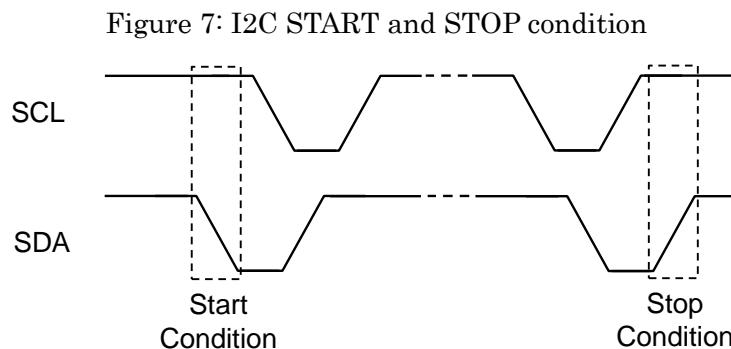
| SA0  | 7-bit Slave Address |
|------|---------------------|
| 1'b0 | 0x6C                |
| 1'b1 | 0x6D                |

The I2C bus takes master clock through SCL pin and exchanges serial data via SDA. SDA is a bidirectional (input/output) connection. Both are open-drain connection and must be connected externally to VID via a pull-up resistor. The I2C interface supports multiple read and write. When using multiple read/write, the internal I2C address pointer will automatically increase by 1 for the next access.

### I2C Access Format: Standard and Fast Mode

One data bit is transferred for each SCL cycle. The SDA must not change level when the SCL is high. The level changes in SDA while SCL is high are reserved control signals. The SDA and SCL remain high when I2C bus is idle.

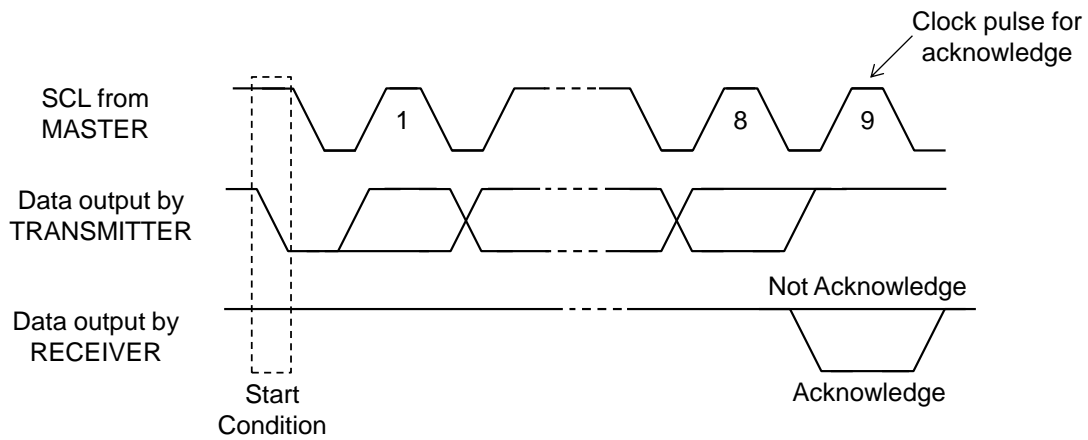
Data transfer begins by bus master indicating a start condition (ST) of a falling edge on SDA when SCL is high. The master terminates transmission and frees the bus by issuing a STOP condition (SP). Stop condition is a rising edge on SDA while SCL is high. The bus remains active if a repeated START (SR) condition is generated instead of a STOP condition. Figure 7 illustrates the START and STOP condition.



After a start condition (ST), the 7-bit slave address + RW bit must be sent by master. If the slave address does not match with GMFPC101, there is no acknowledge and the following data transfer will not affect GMFPC101. If the slave address corresponds to GMFPC101, it will acknowledge by pulling SDA to low and the SDA line should be let free by bus master to enable the data transfer. The master should let the SDA high (no pull down) and generate a high SCL

pulse for GMFPC101 acknowledge. Figure 8 illustrates the acknowledge signal sequence.

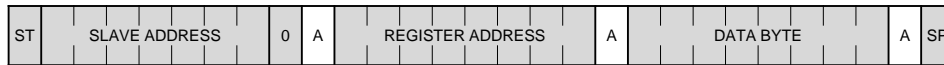
Figure 8: Acknowledge signal sequence



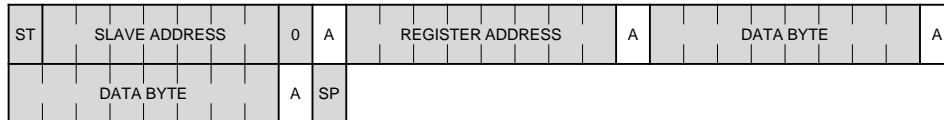
A write to GMFPC101 includes transmission of a START condition, the slave address with R/W bit=1'b0, one byte of data to specify the register address to write, subsequent one or more bytes of data, and finally a STOP condition. "Single Write" and "Multiple Write" in Figure 9 illustrates the frame format of single and multiple write to GMFPC101 respectively.

Figure 9: I2C access format: standard and fast mode

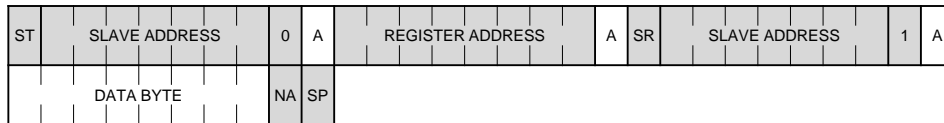
Single Write



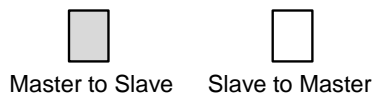
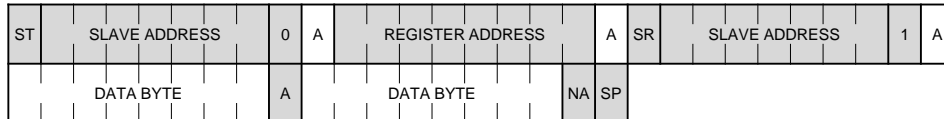
Multiple Write



Single Read



Multiple Read



A = acknowledge  
NA = not acknowledge  
ST = START condition  
SR = repeated START condition  
SP = STOP condition

A read from GMFPC101 starts with transmission of a START condition, the slave address with R/W bit=1'b0, and one byte of data to specify the register address to read. A repeated START

condition and the slave address with R/W bit=1'b1 are transmitted subsequently. The slave address with R/W bit=1'b1 initiates a read operation. GMFPC101 acknowledge receipt of the read operation command by pulling SDA low during the 9<sup>th</sup> SCL clock and begin transmitting the contents starting from the specified register address. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and the STOP condition. “Single Read” and “Multiple Read” in Figure 9 illustrates the frame format for reading single or multiple byte from GMFPC101.

## I2C Specifications

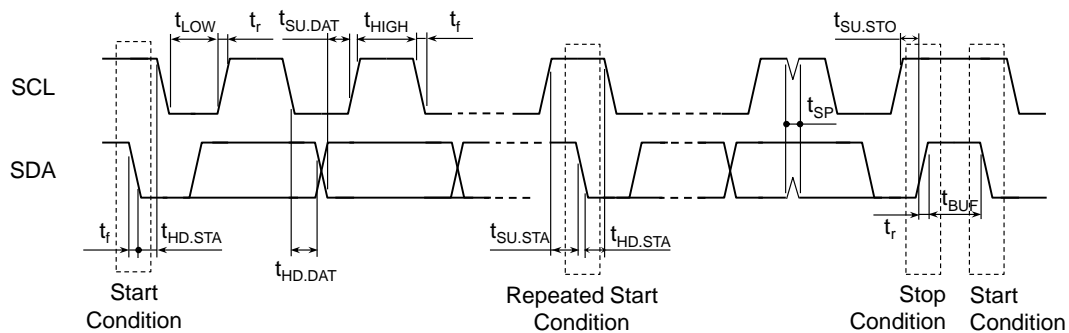
Table 5: I2C Timing Specification: Standard Mode

| Parameter           | Symbol       | Minimum | Typical | Maximum | Unit    |
|---------------------|--------------|---------|---------|---------|---------|
| SCL clock frequency | $f_{SCL}$    | —       | —       | 100     | kHz     |
| Clock low period    | $t_{LOW}$    | 4.7     | —       | —       | $\mu s$ |
| Clock high period   | $t_{HIGH}$   | 4       | —       | —       | $\mu s$ |
| Start hold time     | $t_{HD.STA}$ | 4       | —       | —       | $\mu s$ |
| Start setup time    | $t_{SU.STA}$ | 4.7     | —       | —       | $\mu s$ |
| Data-in hold time   | $t_{HD.DAT}$ | 0       | —       | —       | $\mu s$ |
| Data-in setup time  | $t_{SU.DAT}$ | 250     | —       | —       | ns      |
| Stop setup time     | $t_{SU.STO}$ | 4       | —       | —       | $\mu s$ |
| Rise time           | $t_r$        | —       | —       | 1       | $\mu s$ |
| Fall time           | $t_f$        | —       | —       | 0.3     | $\mu s$ |

Table 6: I2C Timing Specification: Fast Mode

| Parameter             | Symbol       | Minimum | Typical | Maximum | Unit    |
|-----------------------|--------------|---------|---------|---------|---------|
| SCL clock frequency   | $f_{SCL}$    | —       | —       | 400     | kHz     |
| Clock low period      | $t_{LOW}$    | 1.3     | —       | —       | $\mu s$ |
| Clock high period     | $t_{HIGH}$   | 0.6     | —       | —       | $\mu s$ |
| Bus free to new start | $t_{BUF}$    | 1.3     | —       | —       | $\mu s$ |
| Start hold time       | $t_{HD.STA}$ | 0.6     | —       | —       | $\mu s$ |
| Start setup time      | $t_{SU.STA}$ | 0.6     | —       | —       | $\mu s$ |
| Data-in hold time     | $t_{HD.DAT}$ | 0       | —       | —       | $\mu s$ |
| Data-in setup time    | $t_{SU.DAT}$ | 100     | —       | —       | ns      |
| Stop setup time       | $t_{SU.STO}$ | 0.6     | —       | —       | $\mu s$ |
| Rise time             | $t_r$        | —       | —       | 0.3     | $\mu s$ |
| Fall time             | $t_f$        | —       | —       | 0.3     | $\mu s$ |
| Spike width           | $t_{SP}$     | —       | —       | 50      | $\mu s$ |

Figure 10: I2C Timing Diagram: Standard and Fast Mode



## Digital Interface: SPI

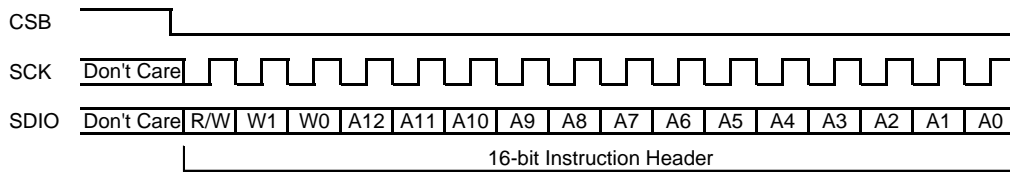
### SPI Interface General Description

Both 3-wire and 4-wire SPI interfaces are supported. The SPI4W bits of RESET register (00h) control such selection. See 00h register description for more detail.

The SPI transaction starts with the falling edge of CSB and the rising edge of SCK. The first phase of the transfer is the instruction phase of 16 bits, followed by multiple data bytes (every byte consists of 8 bits).

The first instruction phase is shown in the Figure 11. The instruction phase is divided into several bit fields.

Figure 11: SPI instruction phase bit field



The first bit field is the read/write indicator bit (R/W). When this bit is set, a read operation is requested. On the other hand when this bit is clear, it indicates a write operation.

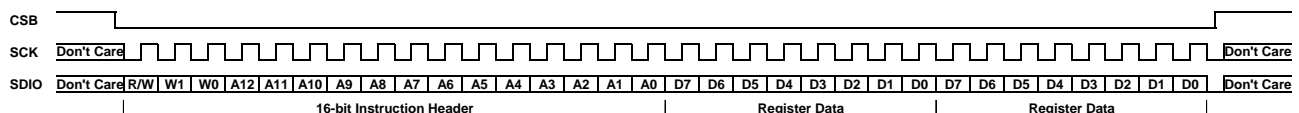
The second bit field consists of two bits, W1 and W0. They represent the number of data bytes to transfer for either read or write. If the number of bytes to transfer is three or less (W1:W0 = 2'00, 2'b01 or 2'b10), CSB can stall high on byte boundaries. Stalling on a non-byte boundary terminates the communication cycle. If W1:W0 = 2'b11, data can be transferred until CSB transit to high, and CSB is not allowed to stall during the whole streaming process. Table 7 summaries such behaviors for W1:W0 settings.

Table 7: W1/W0 settings

| W1:W0 | Description   | CSB stalling |
|-------|---|--------------|
| 2'b00 | 1 bytes of data can be transferred  | Optional     |
| 2'b01 | 2 bytes of data can be transferred  | Optional     |
| 2'b10 | 3 bytes of data can be transferred  | Optional     |
| 2'b11 | 4 or more bytes of data can be transferred.<br>CSB must be held low for the entire process. | No           |

Data follows the instruction phase. Multiple bytes can be transferred in one transaction determined by the W1:W0 bits. Every byte consists of 8 bits. Figure 12 illustrates the timing for transferring two bytes.

Figure 12: SPI access timing

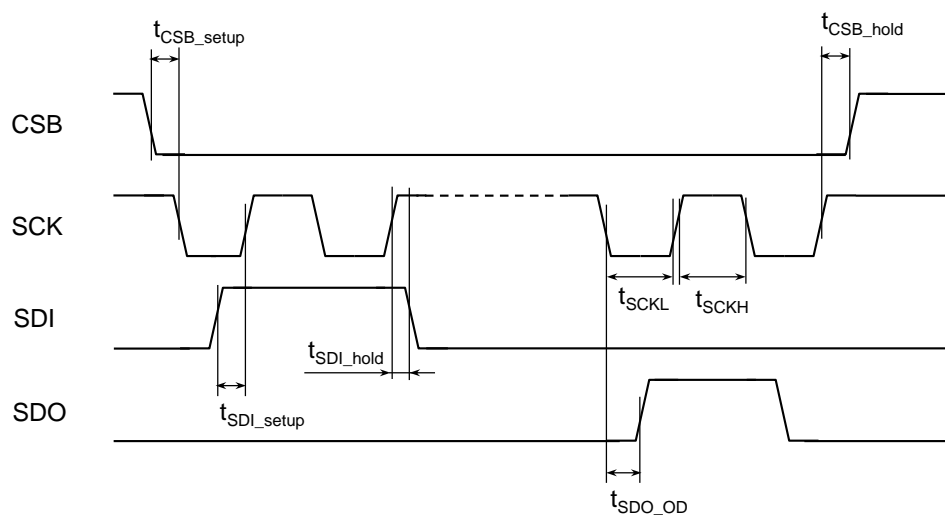


# SPI Specification

Table 8: SPI Timing Specification

| Parameter            | Symbol           | Minimum | Maximum                 | Unit |
|----------------------|------------------|---------|-------------------------|------|
| SCK clock frequency  | $f_{SCK}$        | —       | 10                      | MHz  |
| SCK clock low pulse  | $t_{SCKL}$       | 20      | —                       | ns   |
| SCK clock high pulse | $t_{SCKH}$       | 20      | —                       | ns   |
| SDI setup time       | $t_{SDI\_setup}$ | 20      | —                       | ns   |
| SDI hold time        | $t_{SDI\_hold}$  | 20      | —                       | ns   |
| SDO/SDI output delay | $t_{SDO\_OD}$    | —       | 30 (25pF)<br>40 (250pF) | ns   |
| CSB setup time       | $t_{CSB\_setup}$ | 20      | —                       | ns   |
| CSB hold time        | $t_{CSB\_hold}$  | 40      | —                       | ns   |

Figure 13: SPI Timing Diagram





## Package

### Outline Dimension

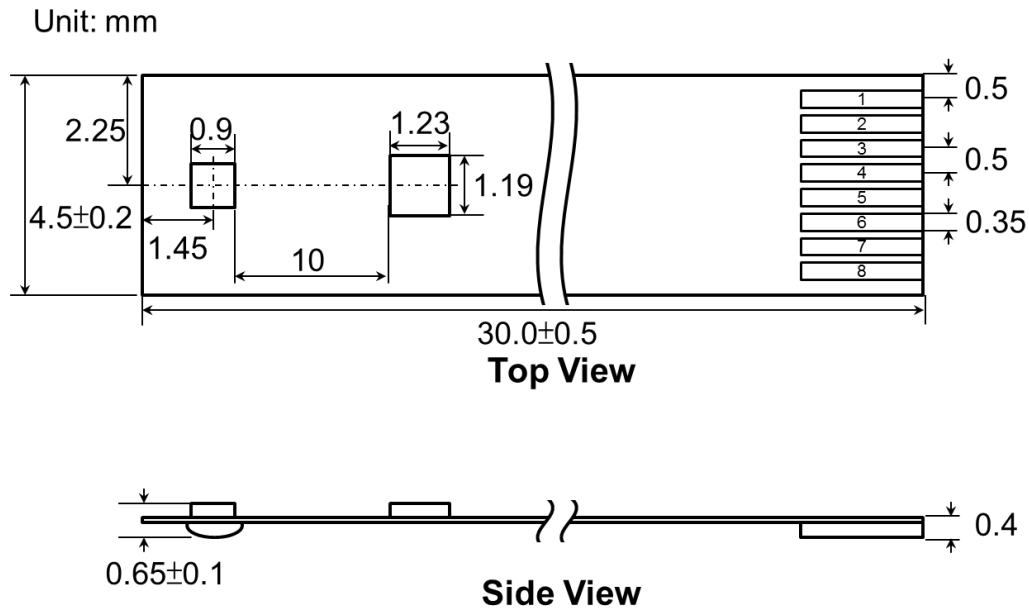


Figure 14: Package Outline Dimension

### RoHS Compliance

GMEMS FPC packaged sensors are compliant with Restrictions on Hazardous Substances (RoHS) and having lead-free terminations. Reflow profiles applicable to those processes can be used successfully for soldering the devices.

### Moisture Sensitivity Level

GMFPC101 package MSL rating is Level 3.