AMBA Bus Architecture

AHB-Lite Specification

Contents

Introduction (1)

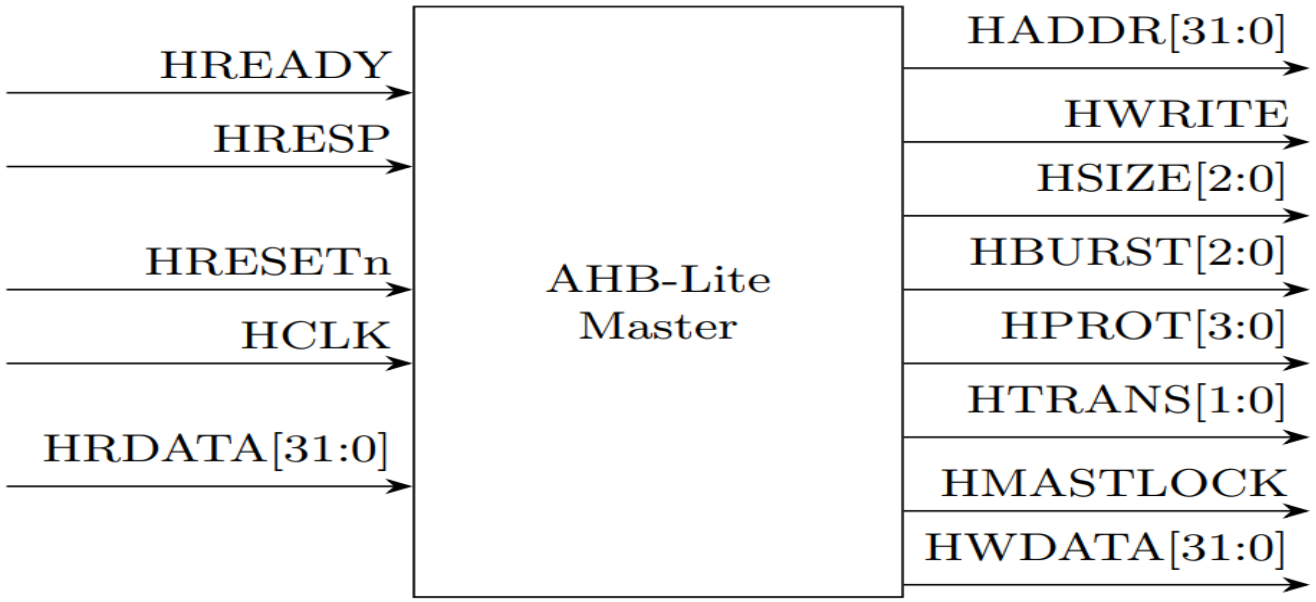
- AHB (Advanced High-performance Bus)
  - ARM IHI 0033A, AMBA 3 AHB-Lite Protocol v1.0 , ARM Ltd.
    - ✓ https://developer.arm.com/documentation/ihi0033/a
  - AMBA 2 introduced AHB to enable high-speed communication.
  - This protocol supports multiple bus masters and features pipelined transfers, burst operations, and split transactions in complex SoC designs.
- AHB-Lite
  - AHB-Lite serves as a simplified version of AHB for single-master systems.
    - ✓ By removing multi-master support, it reduces design complexity with high-performance benefits of AHB.
  - AHB-Lite is more common than AHB.
    - ✓ Modern SoCs and MCUs typically use AHB-Lite due to its simplicity and efficiency in single-master systems.
    - ✓ AHB-Lite is widely adopted in Cortex-M series, FPGA-based SoCs, and embedded applications.
    - ✓ In high-performance CPU clusters or server-class SoCs, AXI or CHI is preferred over AHB.

Introduction (2)

- Main components of an AHB-Lite system
  - The master initiates all read and write transactions.
    - ✓ It provides control signals such as HADDR, HTRANS, HWRITE, HSIZE, and receives data through HRDATA during read operations.
  - The slave responds to the master's requests.
    - ✓ It decodes the address, performs the required operation (read or write), and sends back data and response signals like HRDATA and HREADY.
  - The decoder selects the appropriate slave based on the address from the master.
    - ✓ It generates one-hot HSELx signals to activate the correct slave device.
  - The multiplexer (MUX) forwards response signals from the selected slave to the master.
    - ✓ It ensures that only the active slave’s HRDATA, HREADY, and HRESP are passed back to the master.

Introduction (3)

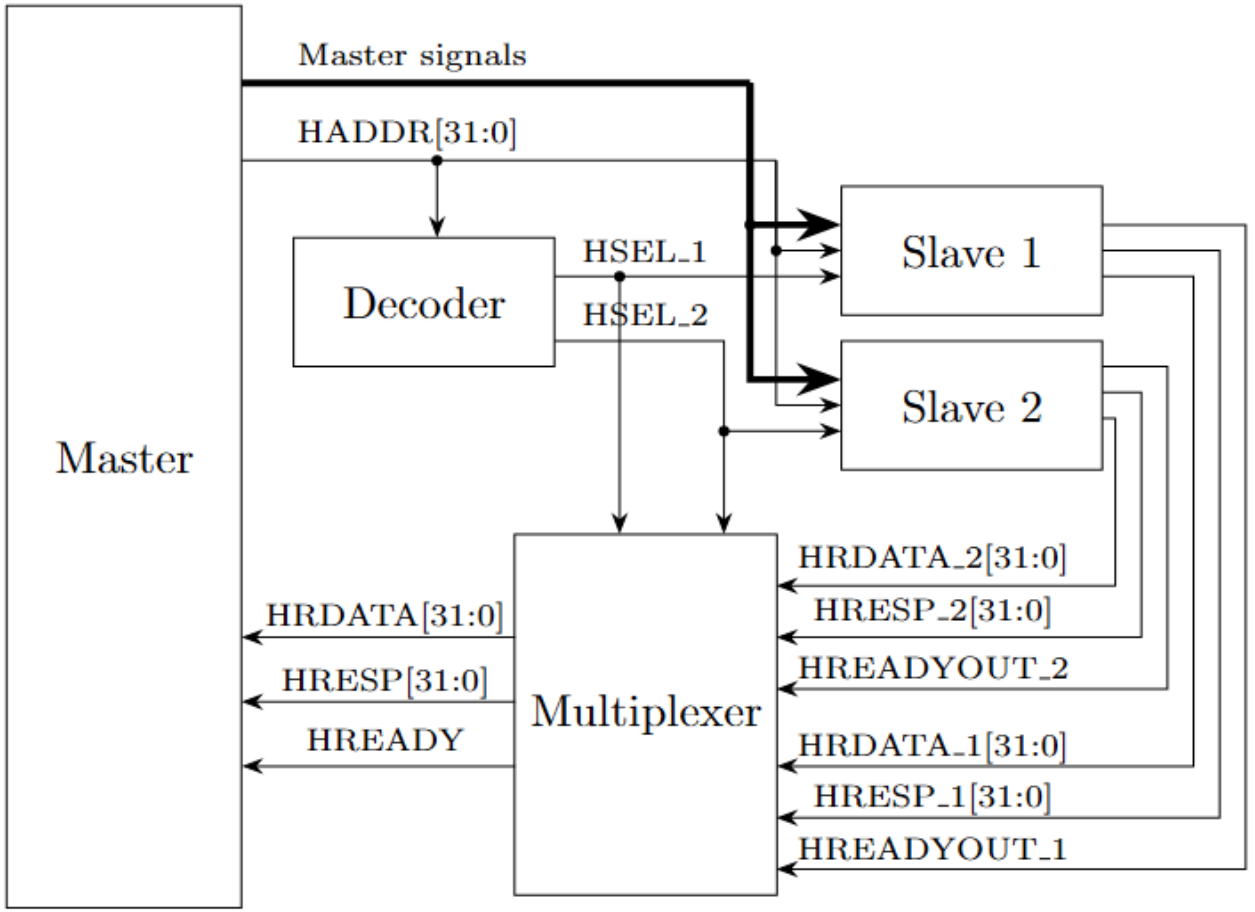
- Master output signals are shared across all slaves in the system.
  - HWRITE, HSIZE, HBURST, HPROT, HTRANS, HMASTERLOCK, and HWDATA.
- Response signals are sent from the currently selected slave
  - HREADY, HRESP, and HRDATA.



< AHB-Lite Master >

Introduction (4)

- An example of two slaves



Signal Descriptions (1)

- AHB-Lite signals use the 'H' prefix for clarity.
- There five functional signal categories:
  - Global
  - Master
  - Slave
  - Decoder
  - Multiplexor

- Global signals

Signal	Meaning	Description
HCLK	Clock	All transfers on the AHB-Lite are synchronized to the rising edge of PCLK.
HRESETn	Reset	The AHB-Lite reset signal is active LOW.

Signal Descriptions (2)

- Master signals

Signal	Meaning	Description
HADDR[31:0]	Address	Specifies the transfer target (memory or peripheral).
HBURST[2:0]	Burst type	Indicates if the transfer is single, incrementing burst, or wrapping burst.
HMASTLOCK	Locked transfer	Indicates a locked sequence of transfers that must not be interrupted.
HPROT[3:0]	Protection	Indicates the privilege level, security, bufferability, and cacheability.
HSIZE[2:0]	Transfer size	Indicates the size of the transfer: byte, halfword, word, etc.
HTRANS[1:0]	Transfer type	Indicates whether a transfer is idle, busy, non-sequential, or sequential.
HWDATA[31:0]	Write data	Sends data from master to slave during write operations.
HWRITE	Write control	Goes HIGH for write transfers, LOW for read transfers.

- Slave signals

Signal	Meaning	Description
HRDATA[31:0]	Read data	Sends data from slave to multiplexor during read operations.
HREADYOUT	Ready	Indicates that a transfer has finished.
HRESP	Status	Goes HIGH on an error condition (ERROR), and LOW otherwise (OKAY).

Signal Descriptions (3)

- Decoder signals

Signal	Meaning	Description
HSELx	Select	Indicates that the current transfer is directed to a specific slave selected by HSELx. The slave must also check HREADY to confirm the previous transfer has finished before responding. This HSELx signal is derived from a combinatorial decode of the address bus.

- Multiplexor signals

Signal	Meaning	Description
HRDATA[31:0]	Read data	Routes the selected slave's HRDATA to the master using the HSELx signal from the decoder.
HREADY	Ready	Goes HIGH when the transfer is complete. It routes to the master and all slaves.
HRESP	Status	Routes the selected slave's HRESP to the master using the HSELx signal from the decoder.

Signal Descriptions (4)

- Locked transfers
  - When the HMASTLOCK is HIGH, the current transfer sequence is locked and must be co mpleted without interruption.
  - This mechanism is typically used to protect critical operations, such as preserving a sem aphore during a read-modify-write (e.g., SWP instruction) to ensure atomicity.
- Protection
  - The HPROT conveys protection-related information about a bus access.
  - They are mainly used by modules that enforce access control or security policies.
  - These signals indicate whether the transfer is:
    - ✓ Instruction fetch / Data access
    - ✓ Privileged mode / User mode
    - ✓ Whether it is cacheable or bufferable
  - Many masters are not capable of generating accurate protection information.

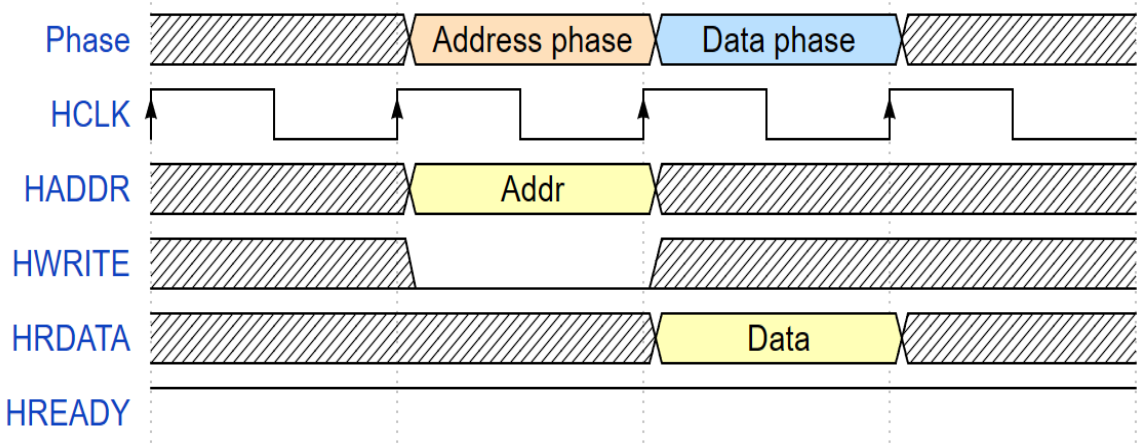
Contents

Basic Transfers (1)

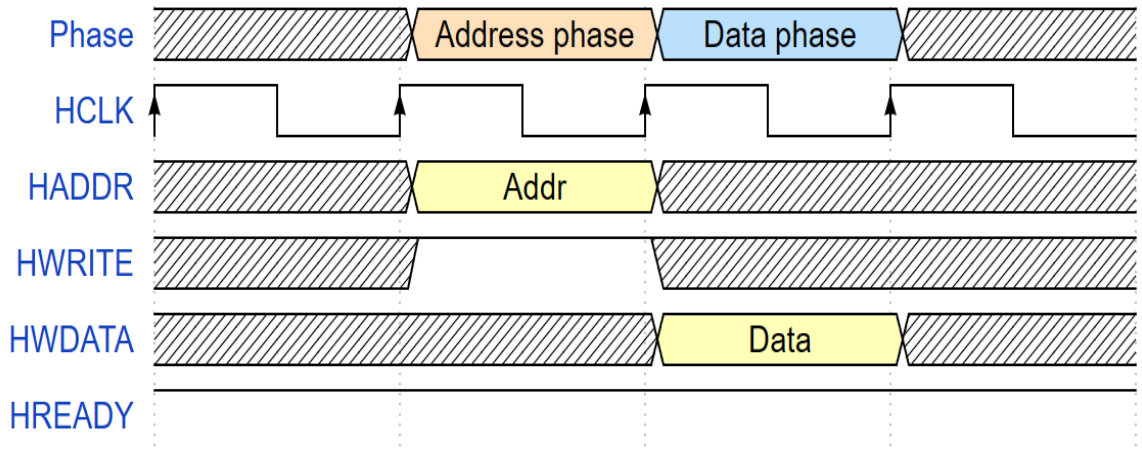
- An AHB-Lite transfer includes address phase and data phase.
- Address phase
  - It typically lasts for one HCLK cycle unless extended by a previous transfer.
  - The HADDR specifies the target address during this phase.
  - The HWRITE signal determines the transfer direction. If it is HIGH, it's a write transfer.
- Data phase
  - The HREADY is HIGH when the transfer is complete.
    - ✓ It may take multiple cycles controlled by the HREADY.
  - If it's a write transfer, the master places data on HWDATA[31:0].
  - If it's a read transfer, the slave returns data on HRDATA[31:0].
  - The HRESP is HIGH when an error has occurred during the transfer.
    - ✓ In this course, we assume HRESP is always LOW (OKAY) for simplicity.

Basic Transfers (2)

- Simple transfer with no wait state:
  - 1. The master places the address and control signals onto the bus immediately after the rising edge of HCLK.
  - 2. On the next rising edge, the slave captures these signals.
  - 3. Once captured, the slave begins driving the HREADY response, which the master samples on the third rising edge of HCLK.



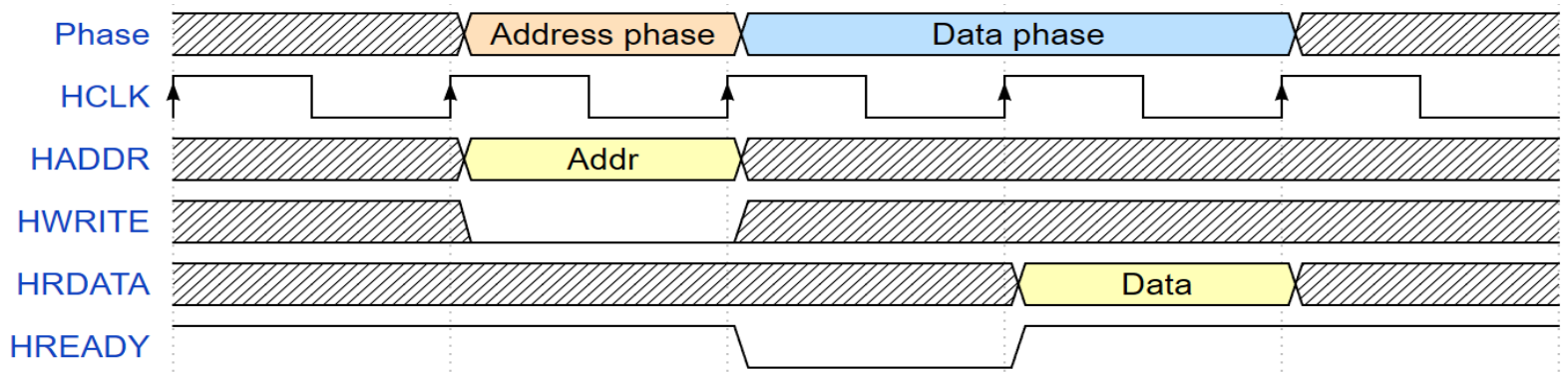
< Single Read Transfer without Wait >



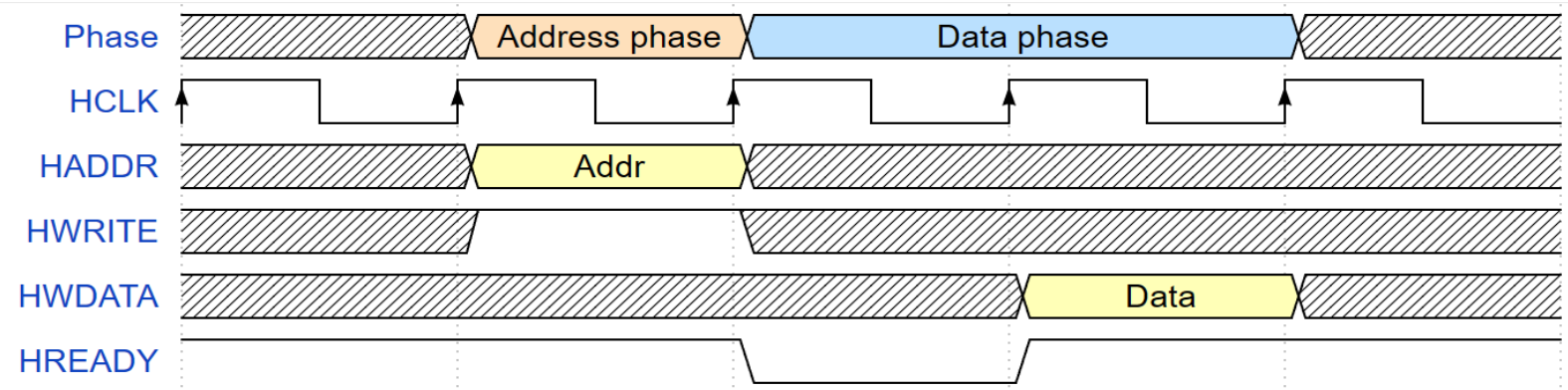
< Single Write Transfer without Wait >

Basic Transfers (3)

- Simple transfer with wait state:
  - If needed, a slave can insert wait states to extend the transfer and complete its response.



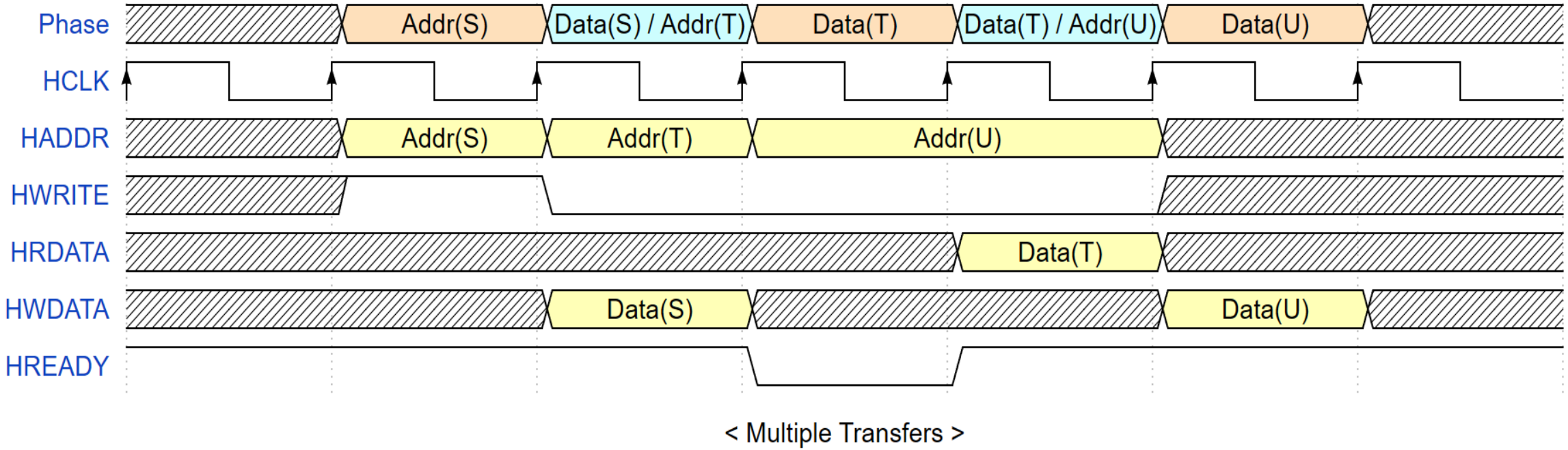
< Single Read Transfer with Wait >



< Single Write Transfer with Wait >

Basic Transfers (4)

- This sequence shows multiple AHB-Lite transfers: a write to address S, a read from address T, and another write to address U.
  - "Addr S" refers to the address phase of transfer S and "Data S" refers to its data phase.
  - Transfer T introduces one wait state, which delays its data phase.
    - ✓ The address phase of transfer U is also delayed, due to the pipelined nature of the bus.



< Multiple Transfers >

Burst Transfers (1)

- A burst transfer is a sequence of data transfers with a single address phase followed by multiple data phases.
  - It improves efficiency by reducing the need for repeated address decoding.
  - The key signals involved are HTRANS, HSIZE, and HBURST.
- A beat refers to a single data transfer within a burst.
  - In a burst of 4 beats with 4-byte data, the total transfer size is 16 bytes.
  - In WRAP mode, the wrap boundary is always aligned to total burst size.
- INCR vs WRAP
  - INCR (Incrementing burst) increases the address by the data size on each beat.
    - ✓ The address keeps growing without restriction.
  - WRAP (Wrapping burst) also increases the address, but wraps back to a boundary when it reaches the end of the burst window.

Burst Transfers (2)

- Ex 1) INCR
  - Data size per beat: 4 bytes
  - Burst length: 4 beats
  - Total transferred: 16 bytes
  - Starting address: 0x00 → 0x04 → 0x08 → 0x0C
- Ex 2) WRAP
  - Data size per beat: 8 bytes
  - Burst length: 4 beats
  - Total transferred: 32 bytes (Wrap boundary: 32-byte window)
  - Starting address: 0x10 → 0x18 → 0x00 → 0x08

Burst Transfers (3)

- The HSIZE indicates the size of a data transfer.
  - Beat size = 2^{HSIZE} bytes ≤ Width of the data bus
    - ✓ 1 bytes ~ 256 bytes
    - ✓ Example: HSIZE = 010 → 2^2 = 4 bytes (32 bits)
- The HBURST controls the burst type.

HBURST[2:0]	Type	Description
b000	SINGLE	Single burst
b001	INCR	Incrementing burst of undefined length
b010	WRAP4	4-beat wrapping burst
b011	INCR4	4-beat incrementing burst
b100	WRAP8	8-beat wrapping burst
b101	INCR8	8-beat incrementing burst
b110	WRAP16	16-beat wrapping burst
b111	INCR16	16-beat incrementing burst

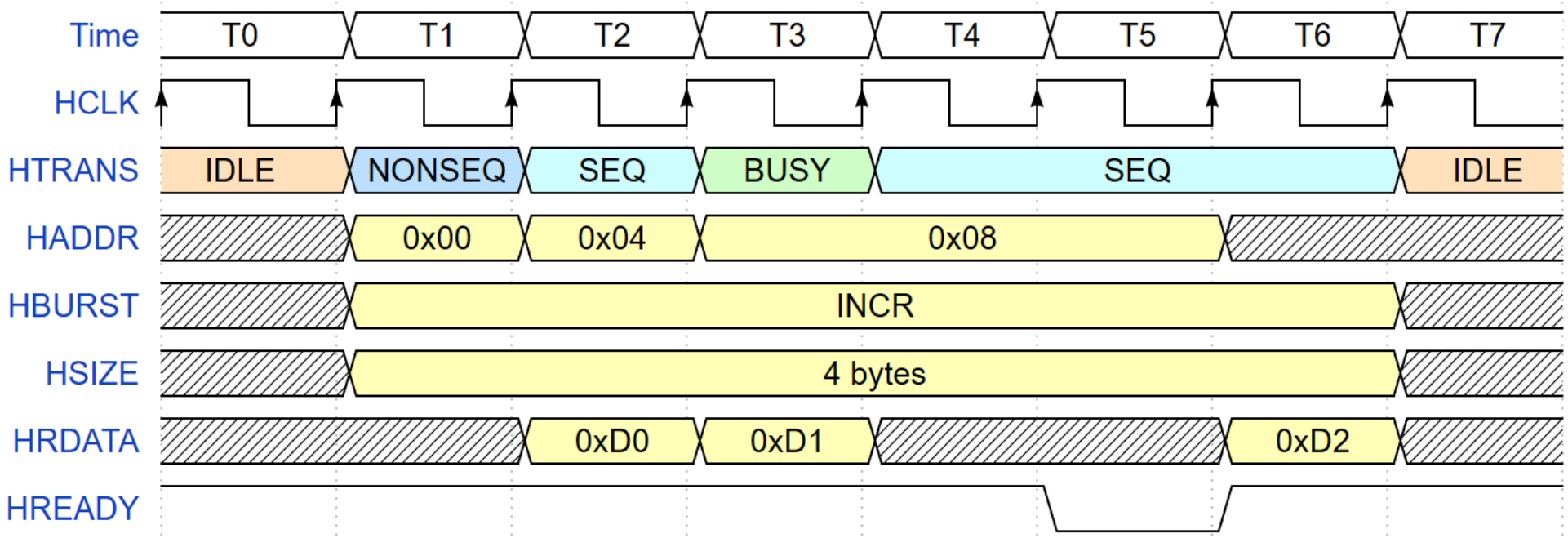
Burst Transfers (4)

- The HTRANS specifies the transfer as one of four types:
  - IDLE, BUSY, NONSEQ, or SEQ

HTRANS[1:0]	Type	Description
b00	IDLE	Signals that no data transfer occurs. Slaves must respond with an immediate OKAY response (zero wait states) and ignore the transfer.
b01	BUSY	Allows the master to insert wait cycles within a burst. A BUSY transfer is allowed as the last cycle only in undefined-length bursts. Master still drives valid address/control for next transfer. Slaves must respond with an immediate OKAY response (zero wait states) and ignore the transfer.
b10	NONSEQ	Used for a single standalone transfer or the first transfer in a burst. It indicates that the address and control signals have no relation to the previous transfer. Even a single transfer is treated as a burst of length one, and is therefore marked as NONSEQUENTIAL.
b11	SEQ	The subsequent transfers in a burst are classified as SEQUENTIAL. All control signals remain identical to those of the prior transfer. Each address is calculated by adding the transfer size (in bytes) specified by HSIZE[2:0]. For wrapping bursts, the address wraps around once it reaches the predefined boundary.

Burst Transfers (5)

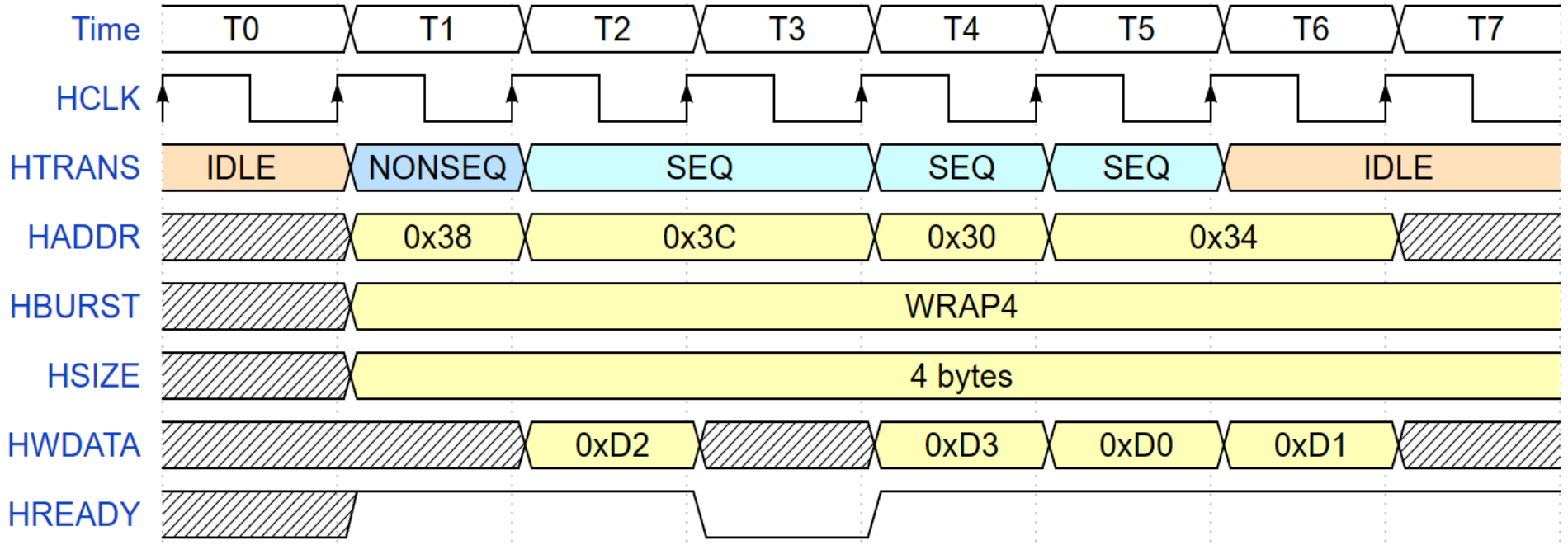
- INCR burst with 3-beat
  - The master sends read requests at T1, T2, and T5.
  - The slave returns data at T2, T3, and T6.
  - A BUSY cycle is inserted at T3, and a wait state delays the third response to T6.



< INCR Burst with 3-Beat >

Burst Transfers (6)

- WRAP4 burst
  - The master sends write requests at T1, T2, T4, and T5.
  - The master sends write data at T2, T4, T5, and T6.
  - A wait state delays the third request to T4.



< WRAP4 Burst >