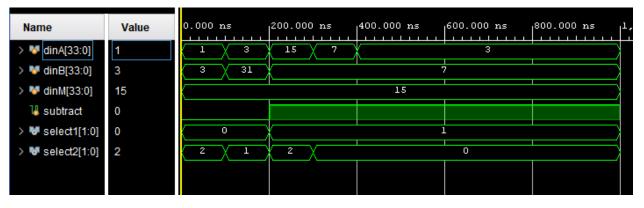
Grant Lance

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HA3 - Testing/Confirmation Doc

- To complete this lab, both maddsub_direct.v and maddsub_pipe.v use 3 different "blocks" or sections.
 - a. The input_check block: this reads subtract, dinA, dinB, and dinM.
 Using the values of these inputs the block sends the correct control signals to the next block, the DSP slices.
 - b. DSP slices/cores: this block uses the IP generator to create a DSP based adder that can be called by the top level of the design.
 - c. Output MUX: this multiplexer determines the output used based on the presence of carry1/carry2 and subtract.
- 2. input check.v



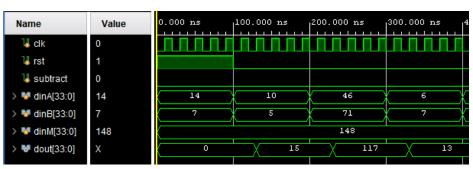
a. The screenshot above shows the functionality of input_check. The truth table below shows the expected output that matches the output above. The select1/select2 value determines the output of the DSP. The DSP code goes as follows: 2'b00 (add), 2'b01 (subtract), 2'b10 (input unchanged), and 2'b11 is unused. Note that the screenshot shows radixes in decimal.

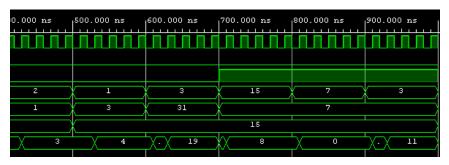
b.

		select1	select2
A + B >= M (subtract == 0)	True	2'b00	2'b00

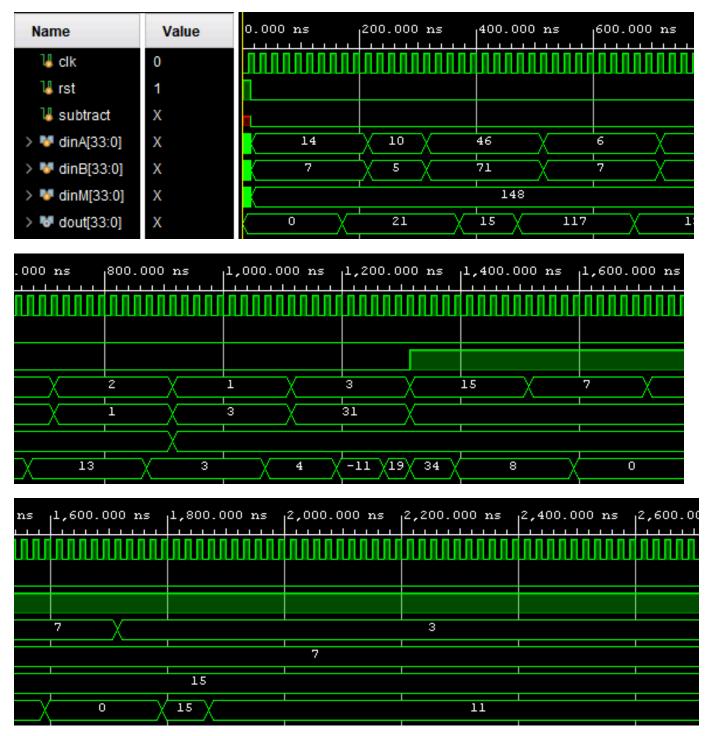
A + B < M (subtract == 0)	True	2'b00	2'b10
A - B <= 0 (subtract == 1)	True	2'b01	2'b00
A - B > 0 (subtract == 1)	True	2'b01	2'b10

3. maddsub_direct.v





- a. Above is the screenshot of tb_maddsub.v. The screenshot shows the radixes in decimal. Looking at the output plot, it can be seen that based on subtract and the values of dinA and dinB the output is the sum or difference of A and B with some mod M.
- 4. Maddsub_pipe.v



a. Above is the screenshot of tb_maddsub_pipe.v. The block performs as expected but is slower than maddsub_direct. There are some data collisions that do go away after a few clock cycles and everything makes it through the DSP. I cannot figure out how to configure the DSP so that the collisions do not happen at all.