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ECE 474 Spring 2024
Homework Assignment 5
1.1 Track 1 (474): Bus Arbiter State Machine

Using the code given during lab/recitation I modified the code to perform as requested: BBUSY will run no more than two cycles before transitioning to TIMEOUT, TIMEOUT will de-assert gnt and wait for rst_n to be de-asserted, after TIMEOUT will go to IDLE. To validate that the block is performing correctly, I created the truth table below. The decimal values of each case is as follows: IDLE (0), BBUSY (1), WAIT (2), BFREE (3), TIMEOUT (4).

Step	1	2	3	4
Test Case 1	0	1	2	3
Test Case 2	0	1	4	0
Test Case 3	0	1	3	n/a

Table 1 - Correct Case Order

Further, to validate that BBUSY is only occurring for a maximum of 2 cycles the count can be viewed to check that the block is functioning correctly. When the cycle count- measured by bbusy_counter- is 3, the block goes to case 4 (nxt_state = 4). Figure 1 shows the section of the simulation where the block correctly detects that it has cycled twice in BBUSY. At this point, busy_counter is 3 and nxt_state = 4. Here it can also be seen that tout is raised when the active state is 4. The same deduction can be made as the function of the TIMEOUT. At 140 ns, rst_n = 0. This caused the block to go from TIMEOUT to IDLE. At this time the bbusy_counter is reset to 0; nxt_state and state are also zero as expected.

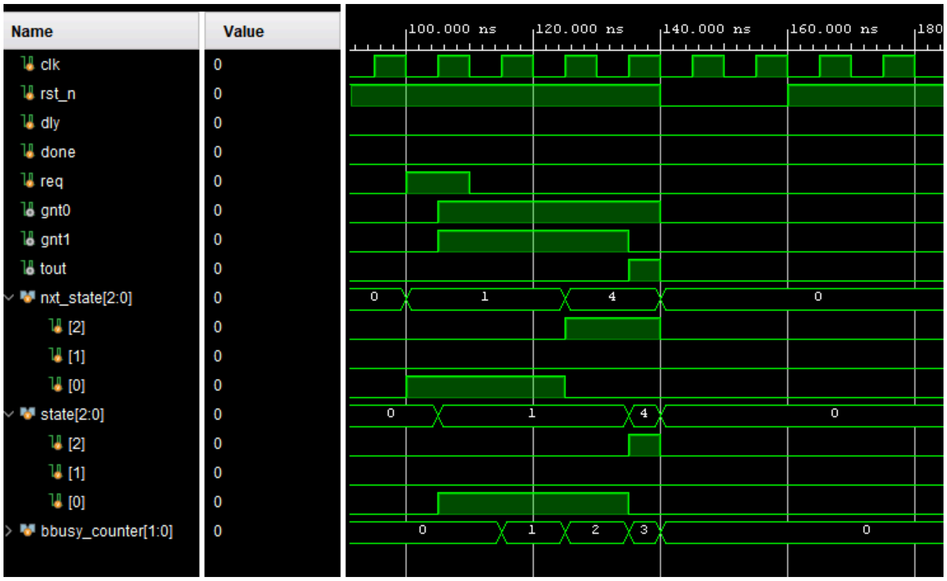


Fig 1 - Section of output that validates the added functionality

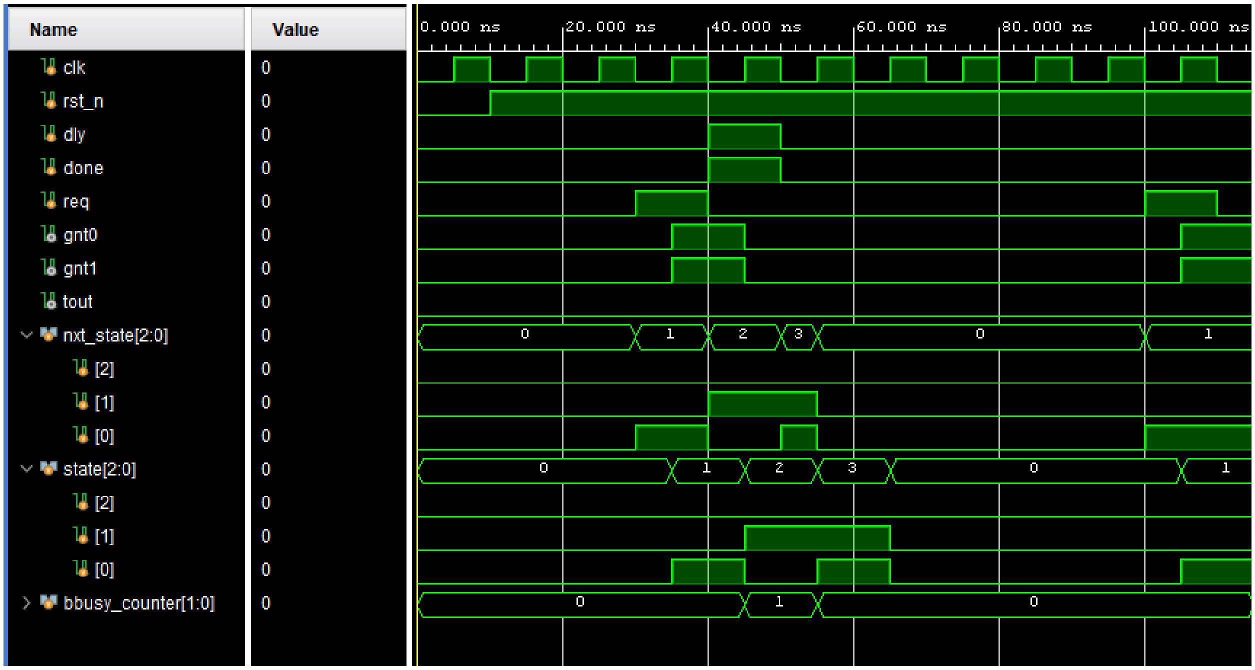


Fig 2 - First half simulation run

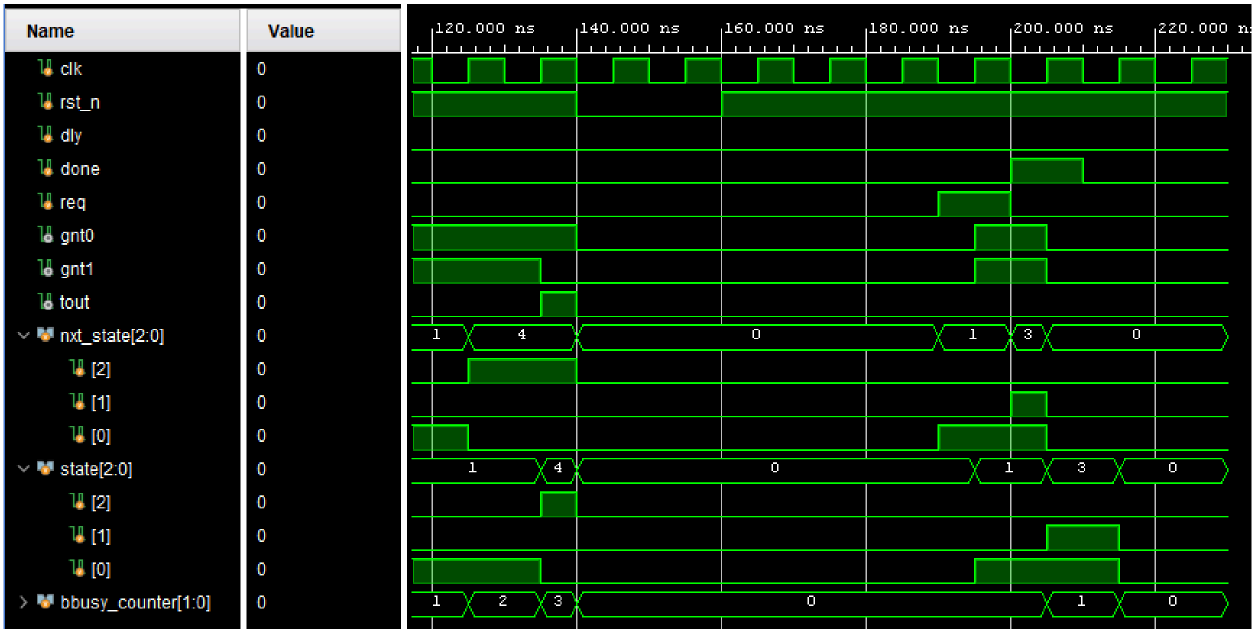
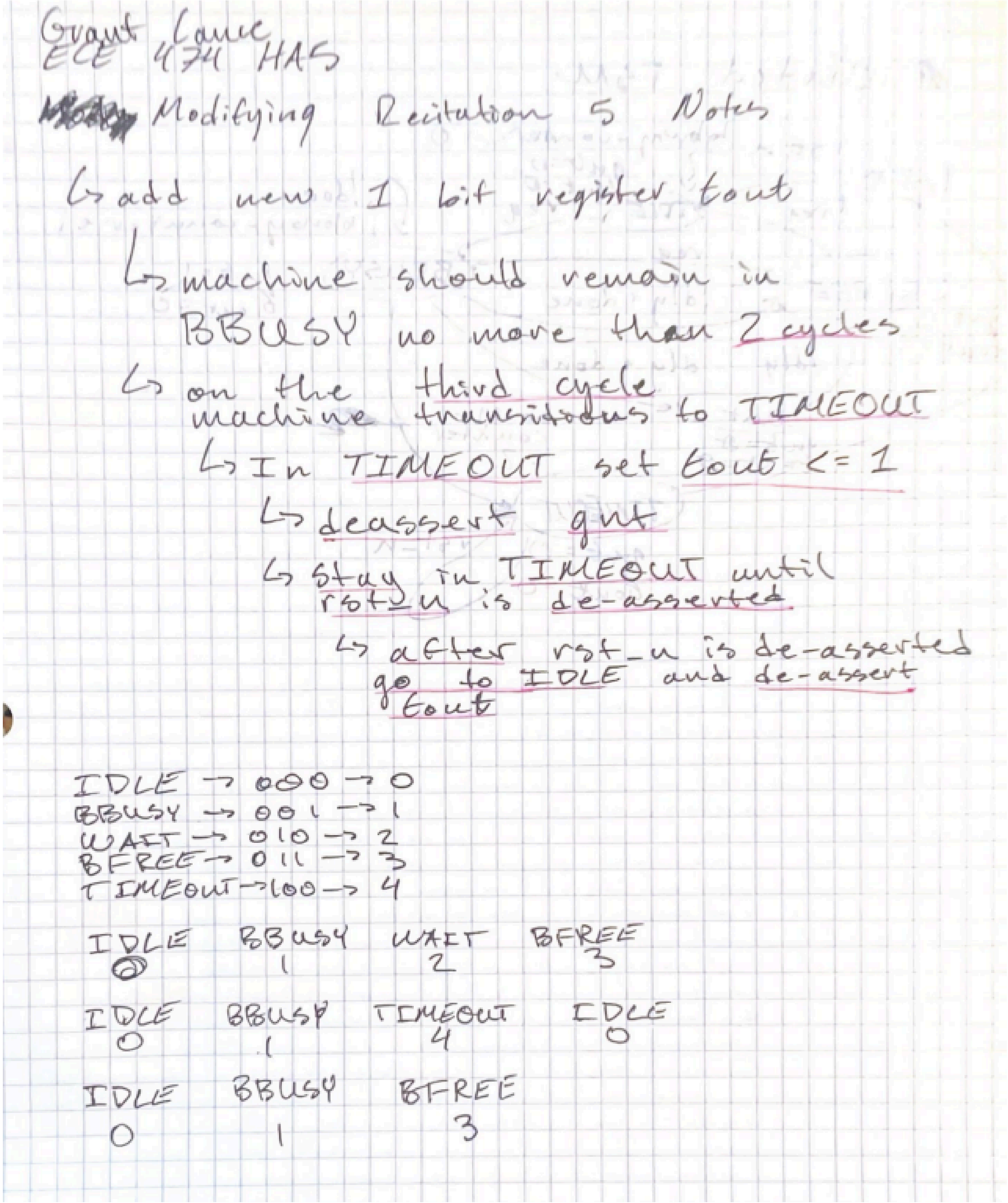


Fig 3 - second half simulation run

Above figures are just as a backup validation in case something happens to my project archive that causes it not to run. Note that both versions of the FSM are demoed in this code, but the nxt_state, state, and bbusy_counter values shown on the waveform are for arbiter1 (not the original arbiter from recitation). Below is the handwritten notes appendix. The second figure in the appendix is the updated FSM diagram. Another side note about the testbench. As Jun's worked perfectly already no changes were made, however I did change the name in the heading as I was unsure of the correct procedure as to not trigger the plagiarism check (I am also assuming we can use this code as it is provided). I would like to add that this is not my attempt to label Jun's work as my own, but rather abide by the naming conventions of the assignment/class.

Appendix



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Modifying Recitation 5 Notes

- ↳ add new 1 bit register tout
  - ↳ machine should remain in BBUSY no more than 2 cycles
  - ↳ on the third cycle machine transitions to TIMEOUT
    - ↳ In TIMEOUT set tout <= 1
      - ↳ deassert gnt
      - ↳ stay in TIMEOUT until rst_n is de-asserted.
        - ↳ after rst_n is de-asserted go to IDLE and de-assert tout

IDLE → 000 → 0
BBUSY → 001 → 1
WAIT → 010 → 2
BFREE → 011 → 3
TIMEOUT → 100 → 4

IDLE	BBUSY	WAIT	BFREE
0	1	2	3
IDLE	BBUSY	TIMEOUT	IDLE
0	1	4	0
IDLE	BBUSY	BFREE	
0	1	3	

Fig 1 - Notes page 1

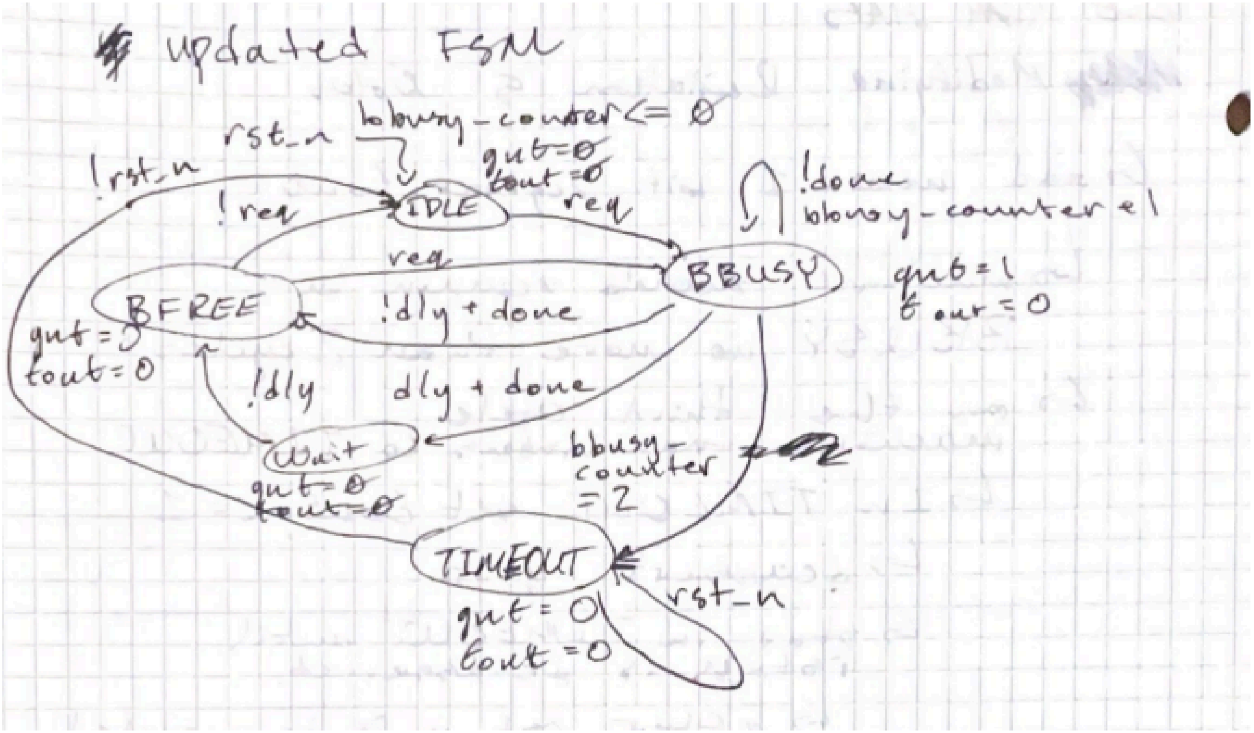

Fig 2 - Notes page 2