Student 1	
NAME	Zeyang Xu
ID	260923070
Student 2	
NAME	Kaicheng Wu
ID	260892789
Student 3 (if applicable)	
NAME	
ID	

Question 1 (1 mark)

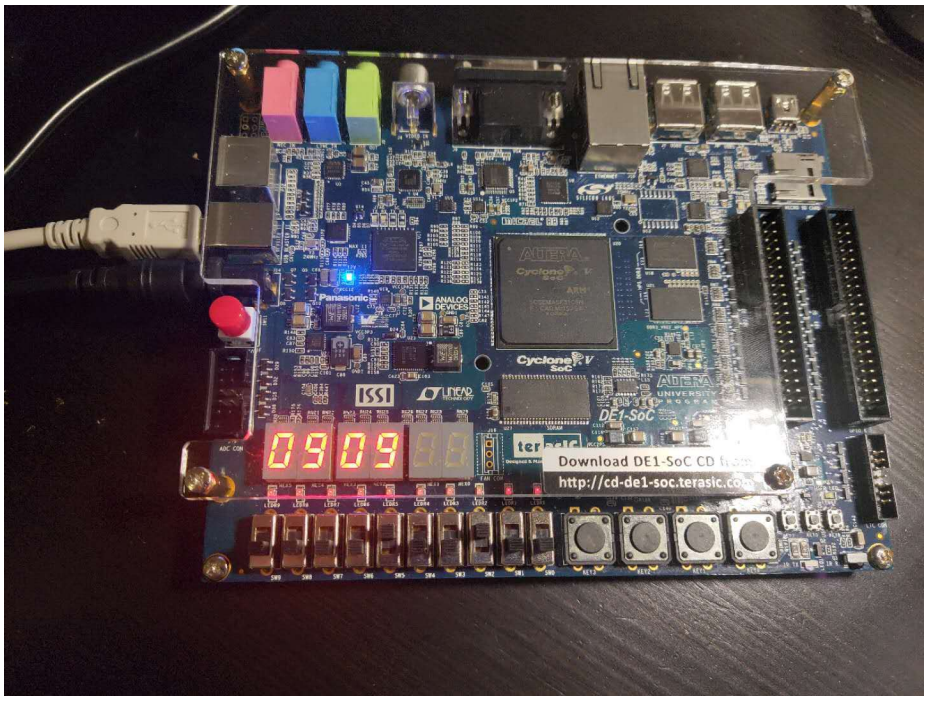
Provide the VHDL code that you wrote for the wrapper circuit.

```
library IEEE;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
use IEEE.std_logic_unsigned.all;
entity zeyang_xu_wrapper is
       Port(  A,B  : in std_logic_vector (3 downto 0);
                     decoded_A : out std_logic_vector (6 downto 0);
                     decoded_B : out std_logic_vector (6 downto 0);
                     decoded_AplusB: out std_logic_vector (13 downto 0));
end zeyang_xu_wrapper;
architecture BehaviorModel of zeyang_xu_wrapper is
component seven_segment_decoder_zeyang
port(  code                  : in std_logic_vector(3 downto 0);
                     segments_out : out std_logic_vector(6 downto 0));
end component;
component zeyang_xu_bcd_adder
       Port(A: in std_logic_vector(3 downto 0);
       B:              in std_logic_vector(3 downto 0);
       S:              out std_logic_vector(3 downto 0);
       C_out : out std_logic);
end component;
((((CODE CONTINUED IN THE NEXT TEXTBOX DUE TO LACK OF SPACE)))
```

```
signal carry: std_logic_vector(3 downto 0);


signal carry_temp: std_logic;

signal result: std_logic_vector(3 downto 0);

signal decode_carry: std_logic_vector(6 downto 0);

signal decode_result: std_logic_vector(6 downto 0);

begin

adder: zeyang_xu_bcd_adder port map (A => A, B=>B, S=>result, C_out=> carry_temp);

carry <= "000"&carry_temp;

decoderA: seven_segment_decoder_zeyang port map(code => A, segments_out => decoded_A);

decoderB: seven_segment_decoder_zeyang port map(code => B, segments_out => decoded_B);

decoder_carry:  seven_segment_decoder_zeyang port map(code => carry, segments_out
=>decode_carry);

decoder_result: seven_segment_decoder_zeyang port map(code => result, segments_out
=>decode_result);

decoded_AplusB <= std_logic_vector(unsigned(decode_carry & decode_result));

end BehaviorModel;
```

Question 2 (2 marks)

Show a representative photo of the board displaying the result of the addition of A and B, where A is the last (right- most) digit of the McGill ID number of one of the students in your group and B is the last (rightmost) digit of the McGill ID number of the other student in the group. Clearly indicate which 7-segment LEDs/ sliding switches are assigned to which inputs/outputs of the circuit on the photo.



A[3-0] is assigned to SW[9-6]

B[3-0] is assigned to SW[5-2]

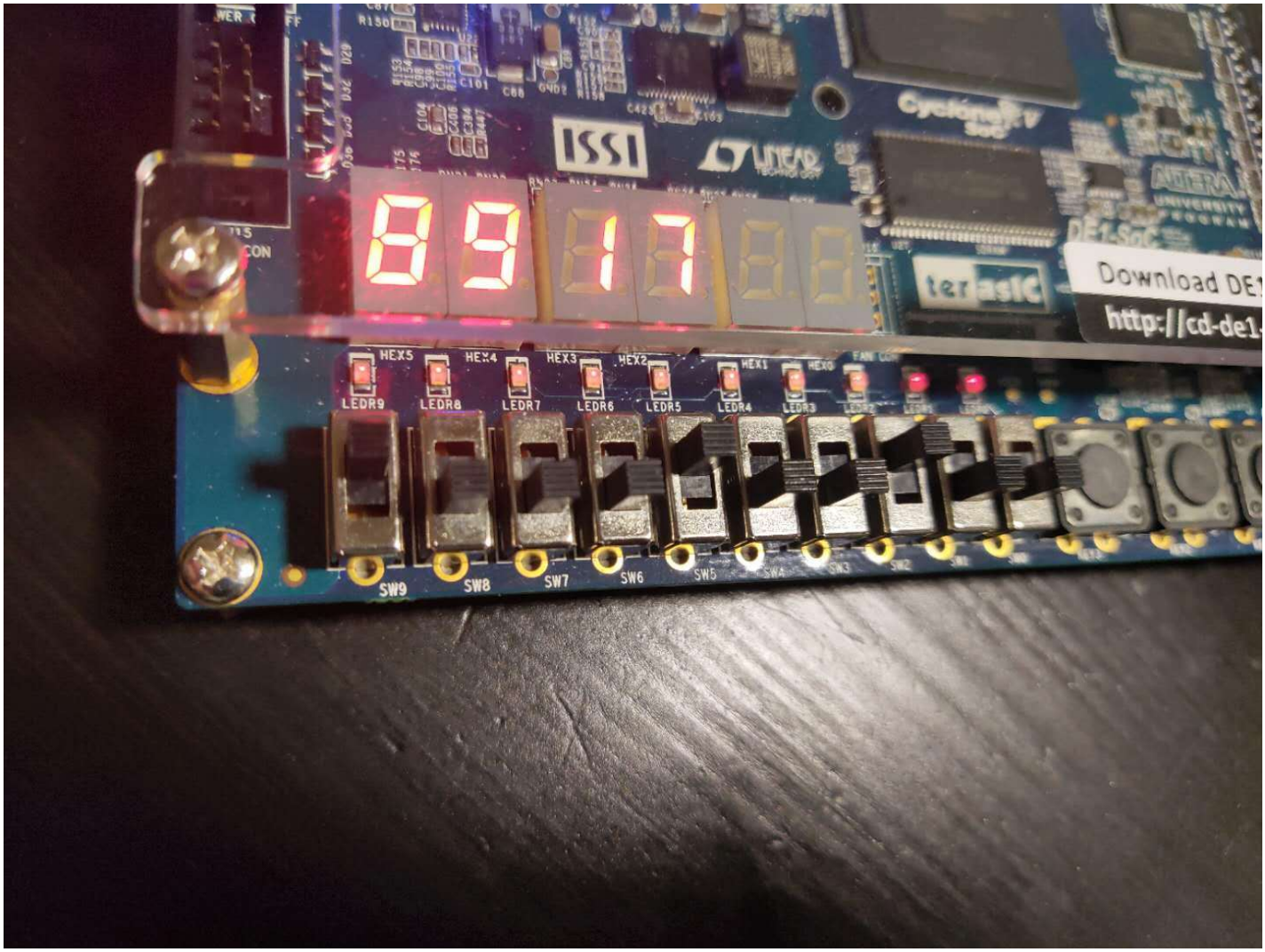
Decoded_A is assigned to HEX5

Decoded_B is assigned to HEX4

Decoded_AplusB[13-7] is assigned to HEX[3]

Decoded_AplusB[6-0] is assigned to HEX[2]

N.B: To demonstrate that it can actually calculate and display beyond 10, a second photo is also included showing 8+9 = 17.


HEX5
HEX4
HEX3
HEX2
HEX1
HEX0
LEDR9
LEDR8
LEDR7
LEDR6
LEDR5
LEDR4
LEDR3
SW9
SW8
SW7
SW6
SW5
terasic