Computer Organization and Architecture COSC 2425

Lecture - 10

Sept 21st, 2022

Acknowledgement: Slides from Edgar Gabriel & Kevin Long

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Chapter 3

Arithmetic for Computers

Questions

- 1. What operations can hardware perform? How to instruct computer to perform a certain operation? How are negative numbers/exponentials represented?
- 2. How do we perform addition, multiplication, division?
- 3. How do we improve the speed of the computer? Can we do things in parallel (compute while loading next data, etc.)
- 4. Where is data stored? How can we make it efficient?
- 5. Can we perform computations in parallel to improve performance?
- 6. How do we define performance?

Questions

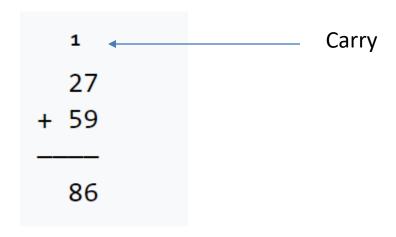
- 1. What operations can hardware perform? How to instruct computer to perform a certain operation? How are negative numbers/exponentials represented?
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Arithmetic for Computers

- Operations on integers
 - Addition and subtraction
 - Dealing with overflow
 - Multiplication and division

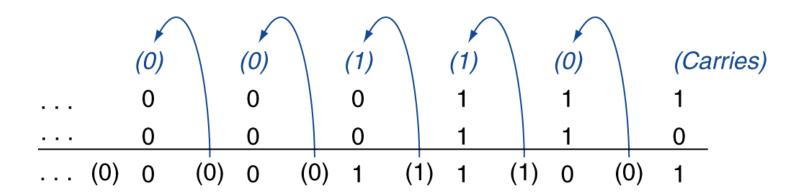
Addition and Subtraction

- Unsigned numbers:
- Addition in binary is same as addition in decimal system.



Addition and Subtraction

- Addition in binary is same as addition in decimal system.
- Addition of unsigned numbers
- Adding 6_{ten} to 7_{ten}



Adding 64-bit numbers

• Subtracting 6_{ten} from 7_{ten} directly

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- - Subtracting 6_{ten} from 7_{ten} using two's complement.

$$7 + (-6)$$

• Subtracting 6_{ten} from 7_{ten} directly

- - Subtracting 6_{ten} from 7_{ten} using two's complement. 7 + (-6)

Subtraction uses addition, the appropriate operand is negated.

Unsigned Integers

65 bits needed Results in an **overflow**.

- Signed integers, addition
- When can an overflow occur?

Operand 1	Operand 2	Overflow	Check
+ve	-ve		
-ve	+ve		

- Signed integers, addition
- When can an overflow occur?

Operand 1	Operand 2	Overflow	Check
+ve	-ve	No	
-ve	+ve	No	

-10 + 4 = -6Sum is never larger than one of the operands, and must fit in 64 bits.

- Signed integers, addition
- When can an overflow occur?

Operand 1	Operand 2	Overflow	Check
+ve	-ve	No	
-ve	+ve	No	
+ve	+ve		

2's Complement

- Lets consider a 4-bit representation of numbers, 16 combinations are possible
 - Let us consider 7 + 40111+ 0100

0000	0	
0001	1	
0010	2	
0011	3	
0100	4	
0101	5	
0110	6	
0111	7	
1000	-8	
1000	-8 -7	
1001	-7	
1001 1010	-7 -6	
1001 1010 1011	-7 -6 -5	
1001 1010 1011 1100	-7 -6 -5 -4	

2's Complement

- Lets consider a 4-bit representation of numbers, 16 combinations are possible
 - Let us consider 7 + 4
 0111
 + 0100
 1011

Adding two +ve numbers results in a negative number, then overflow has occurred

0
1
2
3
4
5
6
7
7 -8
, , , , , , , , , , , , , , , , , , ,
-8
-8 -7
-8 -7 -6
-8 -7 -6 -5
-8 -7 -6 -5 -4

- Signed integers, addition
- When can an overflow occur?

Operand 1	erand 1 Operand 2 Overflow		Check
+ve	-ve	No	
-ve	+ve	No	
+ve	+ve	Yes	-ve result

- Signed integers, addition
- When can an overflow occur?

Operand 1	Operand 2	Overflow	Check
+ve	-ve	No	
-ve	+ve	No	
+ve	+ve	Yes	-ve result
-ve	-ve		

2's Complement

 Lets consider a 4-bit representation of numbers, 16 combinations are possible

- Let us consider (-8) + (-7)

$$1000$$

$$+ 1001$$
Over flow bit
Sign bit

Adding two -ve numbers results in a positive number, then overflow has occurred

0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	-8
1000	-8 -7
1001	-7
1001	-7 -6
1001 1010 1011	-7 -6 -5
1001 1010 1011 1100	-7 -6 -5 -4
1001 1010 1011 1100 1101	-7 -6 -5 -4 -3

- Signed integers, addition
- When can an overflow occur?

Operand 1	erand 1 Operand 2 Overflow		Check
+ve	-ve	No	
-ve	+ve	No	
+ve	+ve	Yes	-ve result
-ve	-ve	Yes	+ve result

OVERFLOW RULE:

If two numbers are added, and they are both positive or both negative, then overflow occurs if and only if the result has the opposite sign.

No overflow can occur when adding numbers with different signs

2's Complement

 Lets consider a 4-bit representation of numbers, 16 combinations are possible

 Overflow can not occur if the two operands have different signs -> ignore overflow bit

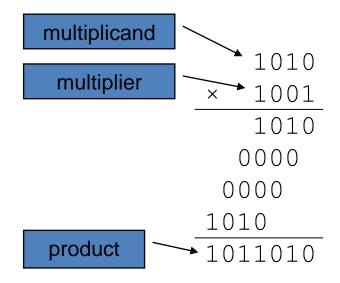
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	-8
1001	-7
1010	-6
1011	-5
1100	-4
1101	-3
	-2
1110	-2

Multiplication

Start with long-multiplication approach

Multiplication of binary number is similar to

decimal system



- Start with long-multiplication approach
- Multiplication of binary number is similar to decimal system

1111 ***** 1111

- Start with long-multiplication approach
- Multiplication of binary number is similar to decimal system

Length of product never greater sum of operand lengths

Operand 1 length \rightarrow 4

Operand 2 length \rightarrow 4

Result length ≤ 8

1111
* 1111
1111
1111
1111
1111
11100001

- Start with long-multiplication approach
- Multiplication of binary number is similar to decimal system
- 1. Length of product never greater sum of operand lengths

- Start with long-multiplication approach
- Multiplication of binary number is similar to decimal system
- 1. Length of product never greater sum of operand lengths

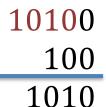
- Start with long-multiplication approach
- Multiplication of binary number is similar to decimal system
- 1. Length of product never greater sum of operand lengths
- 2. Multiplication:
 - 1. If multiplier bit is 1, simply copy the multiplicand

 $\begin{array}{r}
 1010 \\
 \hline
 1001 \\
 \hline
 1010
 \end{array}$

- Start with long-multiplication approach
- Multiplication of binary number is similar to decimal system
- 1. Length of product never greater sum of operand lengths
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 - 2. Shift multiplicand by 1 bit to left and fill zeros on right

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1	If multiplion	hit ic 1	cimply	convetha	multiplicand
⊥.	ii iiiuitipiiei	DIL 15 \perp ,	Sillibia	copy the	multiplicand

- 1. If multiplier bit is 0, fill with zeros
- 2. Shift multiplicand by 1 bit to left and fill zeros on right
- 3. Shift Multiplier 1 bit to the right
- 4. Repeat

10100
100
1010
00000

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- 2. Shift multiplicand by 1 bit to left and fill zeros on right
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- 4. Repeat

101000
1 <mark>0</mark>
1010

101000

00000

- Start with long-multiplication approach
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- 1. Length of product never greater sum of operand lengths
- 2. Multiplication:

1.	If multiplier bit is 1,	simply copy	the multiplicand
		1 / 1 /	•

1.	If multipl	ier bit is 0), fill with	zeros
			,	

- 2. Shift multiplicand by 1 bit to left and fill zeros on right
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- 4. Repeat

10	110000
	10
	1010
	00000

- Start with long-multiplication approach
- Multiplication of binary number is similar to decimal system
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1.	If multiplier	bit is 1.	simply	copy the	multiplicand
- •	ii iiiaicipiici	Σ	31111619	copy the	marcipilicania

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1010000 1 1010

00000

- Start with long-multiplication approach
- Multiplication of binary number is similar to decimal system
- 1. Length of product never greater sum of operand lengths
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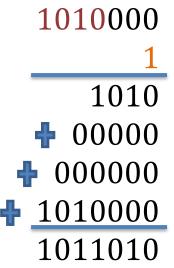
1.	If multiplier	bit is 1,	simply	copy the	multiplicand
		<i>_,</i>	· · · · · · · · · · · · · · · · · · ·	July 3	

1.	If multiplier	bit is 0, fi	ll with zeros
		,	

- 2. Shift multiplicand by 1 bit to left and fill zeros on right
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- 4. Repeat

1010000
1
1010
00000
000000
1010000

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- Start with long-multiplication approach
- Multiplication of binary number is similar to decimal system

Length of product never greater sum of operand lengths If the integers are represented using 4 btis,

To design the multiplication hardware, lets consider the multiplicand and the result to be 8 bits long.

Multiplicand: 1010

Multiplier: 1001

Multiplicand: 1010

Multiplier: 1001

Initialize multiplicand register with 8 bits, consisting of leading zeros

Multiplicand register 0000 1010

Multiplicand: 1010

Multiplier: 1001

Initialize multiplicand register

 Initialize product register with 8 bits, consisting of all zeros Multiplicand register 0000 1010

Multiplicand: 1010

Multiplier: 1001

- Initialize multiplicand register
- Initialize product register
- Initialize multiplier register, 4 bits

Multiplicand register 0000 1010

Multiplier register 1001

Multiplicand: 1010

Multiplier: 1001

Initialize multiplicand register

HW Shift left

- Initialize product register
- Initialize multiplier register, 4 bits

Multiplicand register 0000 1010

Shift left Multiplier register 1001

Multiplicand: 1010

Multiplier: 1001

Initialize multiplicand register

HW Shift left

- Initialize product register
- Initialize multiplier register, 4 bits
 - HW Shift right

Multiplicand register 0000 1010

Shift left right Multiplier register 1001

Shift

- Iteration 1
 - Check if multiplier bit is 0/1

Multiplicand register 0000 1010

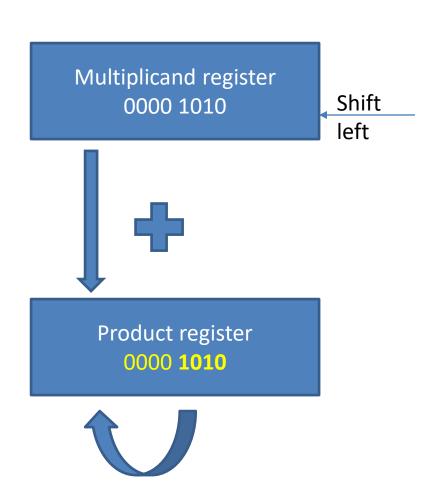
Shift left Multiplier register

Shift

right

Iteration 1

- Check if multiplier bit is 0/1
- If 1 add multiplicand to product register
- Else do nothing



Shift right

Multiplier register

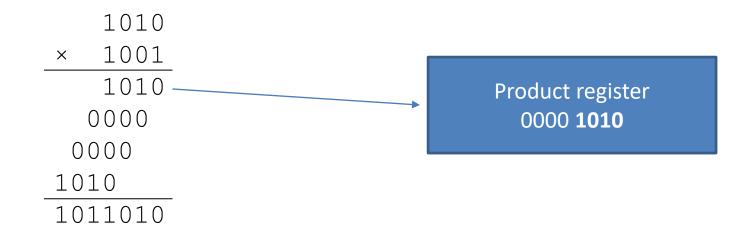
1001

Iteration 1

- Check if multiplier bit is 0/1
- If 1 add multiplicand to product register
- Else do nothing

Multiplicand register 0000 1010

Shift left Shift right Multiplier register 1001



Iteration 1

- Check if multiplier bit is 0/1
 - If 1 add multiplicand to product register
 - Else do nothing
- Shift multiplicand to left by 1 bit

Multiplicand register 0000 1010

Shift left Shift right

Multiplier register

1001

• Iteration 1

- Check if multiplier bit is 0/1
 - If 1 add multiplicand to product register
 - Else do nothing
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Multiplicand register 0001 0100

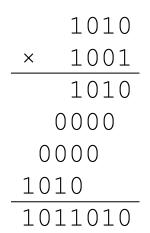
Shift left Shift right

Multiplier register

1001

Iteration 1

- Check if multiplier bit is 0/1
 - If 1 add multiplicand to product register
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Multiplicand register 0001 0100

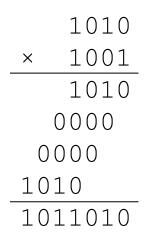
Shift left Shift right

Multiplier register

1001

Iteration 1

- Check if multiplier bit is 0/1
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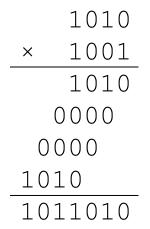
Multiplicand register 0001 0100

Shift left right
Multiplier register
0100

Shift

Iteration 1

- Check if multiplier bit is 0/1
 - · If 1 add multiplicand to product register
 - Else do nothing
- Shift multiplicand to left by 1 bit
- Shift multiplier 1 bit to the right
- Repeat 4 times (total)



Multiplicand register 0001 0100

Shift left Multiplier register 0100

Shift

right

Iteration 2

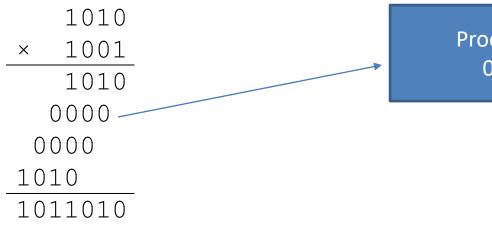
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- Repeat 4 times (total)

Multiplicand register 0001 0100

Shift left Shift right

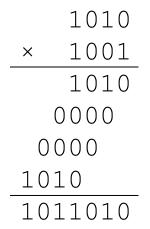
Multiplier register

0100



Iteration 2

- Check if multiplier bit is 0/1
 - · If 1 add multiplicand to product register
 - Else do nothing
- Shift multiplicand to left by 1 bit
- Shift multiplier 1 bit to the right
- Repeat 4 times (total)



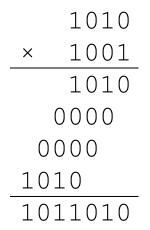
Multiplicand register 0010 1000

Shift left right Multiplier register 010**0**

Shift

Iteration 2

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- Repeat 4 times (total)



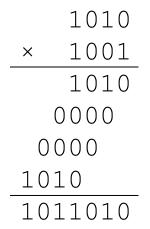
Multiplicand register 0010 1000

Shift left right Multiplier register 0010

Shift

Iteration 2

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Multiplicand register 0010 1000

Shift left right Multiplier register 0010

Shift

Iteration 3

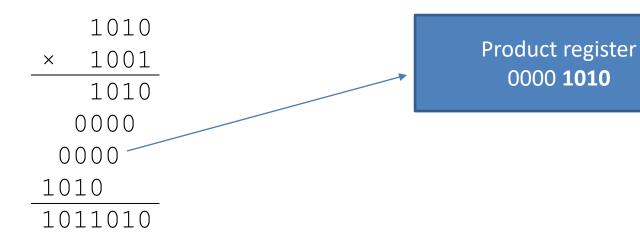
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Multiplicand register 0010 1000

Shift left Shift right

Multiplier register

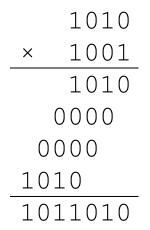
0010



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Iteration 3

- Check if multiplier bit is 0/1
 - · If 1 add multiplicand to product register
 - Else do nothing
- Shift multiplicand to left by 1 bit
- Shift multiplier 1 bit to the right
- Repeat 4 times (total)



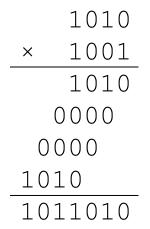
Multiplicand register 0101 0000

Shift left right Multiplier register

Shift

Iteration 3

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- Repeat 4 times (total)



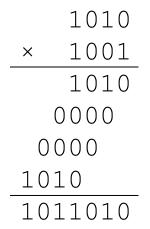
Multiplicand register 0101 0000

Shift left right Multiplier register

Shift

Iteration 3

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 - If 1 add multiplicand to product register
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- Shift multiplicand to left by 1 bit
- Shift multiplier 1 bit to the right
- Repeat 4 times (total)



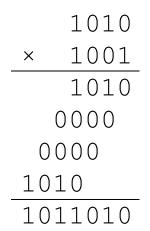
Multiplicand register 0101 0000

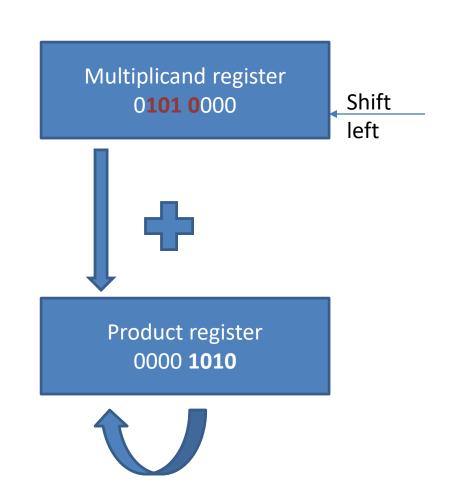
Shift left right Multiplier register 0001

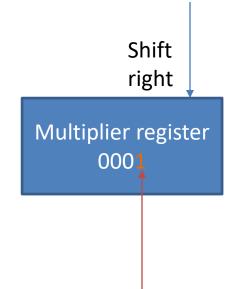
Shift

Iteration 4

- Check if multiplier bit is 0/1
 - If 1 add multiplicand to product register
 - Else do nothing
- Shift multiplicand to left by 1 bit
- Shift multiplier 1 bit to the right
- Repeat 4 times (total)







Iteration 4

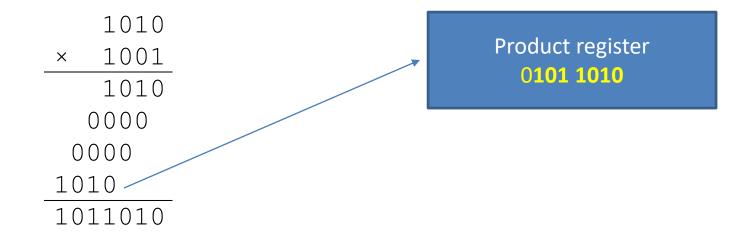
- Check if multiplier bit is 0/1
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- Shift multiplier 1 bit to the right
- Repeat 4 times (total)

Multiplicand register 0101 0000

Shift left Shift right

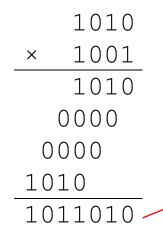
Multiplier register

0001



Iteration 4

- Check if multiplier bit is 0/1
 - If 1 add multiplicand to product register
 - Else do nothing
- Shift multiplicand to left by 1 bit
- Shift multiplier 1 bit to the right
- Repeat 4 times (total)
- Exit



Multiplicand register 0101 0000

Shift left Multiplier register 0001

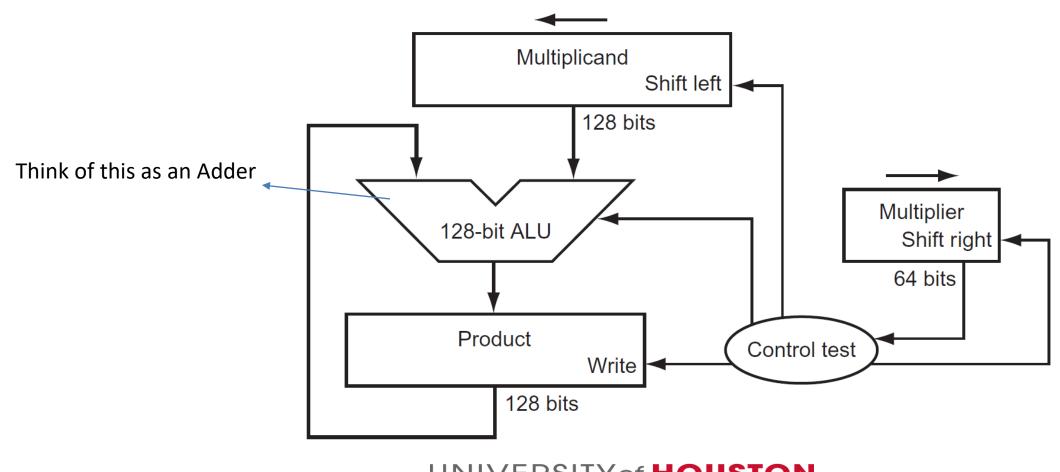
Shift

right

Start Multiplier0 = 1 Multiplier0 = 0 1. Test Multiplier0 1a. Add multiplicand to product and place the result in Product register 2. Shift the Multiplicand register left 1 bit 3. Shift the Multiplier register right 1 bit No: < 64 repetitions repetition? Yes: 64 repetitions Done

Multiplication Flowchart



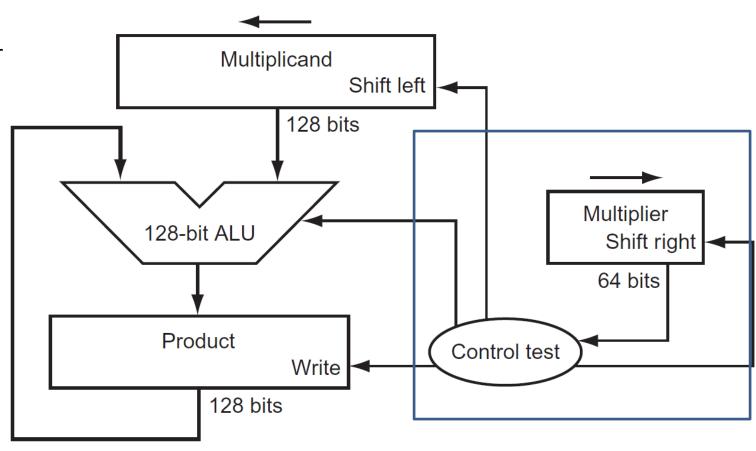


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Check if multiplier bit is 0/1

If 1 add multiplicand to product register Else do nothing

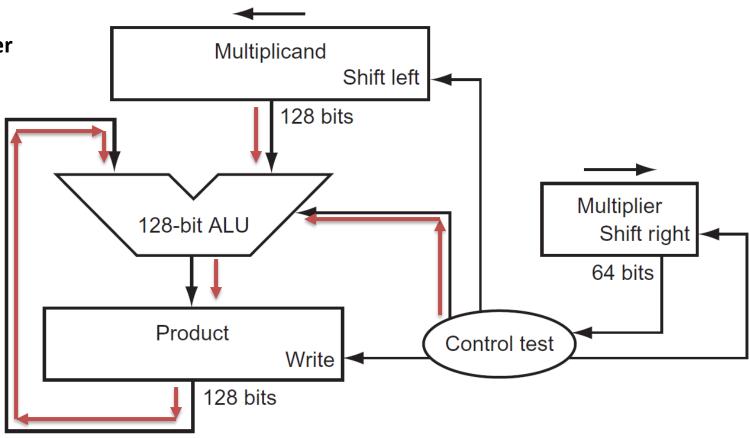
Shift multiplicand 1 bit to left
Shift multiplier 1 bit to the right
Repeat 32 times (total)



Check if multiplier bit is 0/1

If 1 add multiplicand to product register Else do nothing

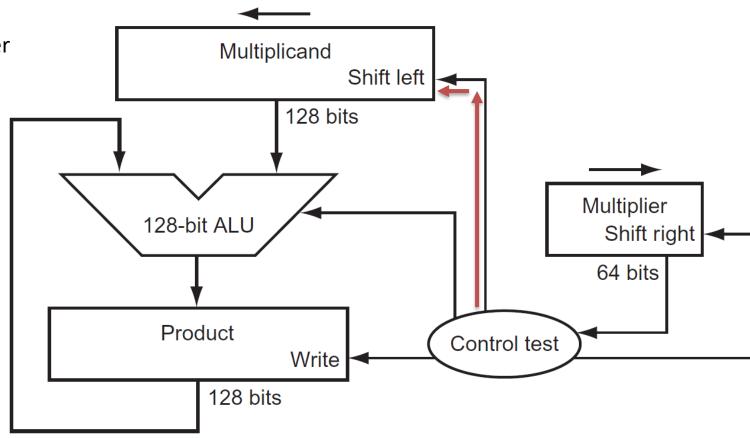
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Shift multiplier 1 bit to the right
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Repeat 32 times (total)

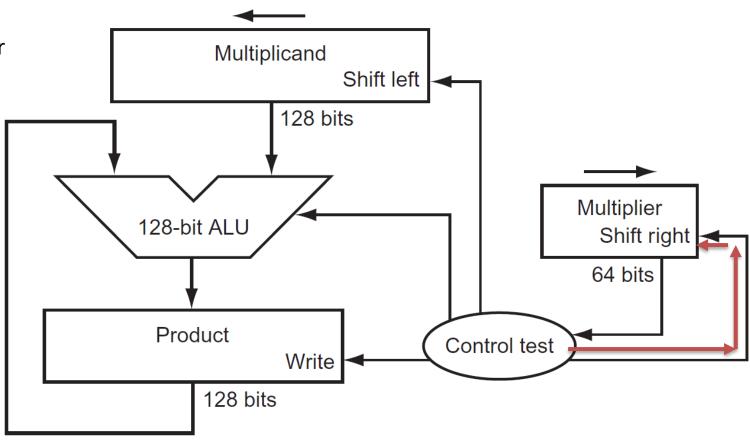


Multiplication Hardware

Check if multiplier bit is 0/1

If 1 add multiplicand to product register Else do nothing

Shift multiplicand 1 bit to left **Shift multiplier 1 bit to the right**Repeat 32 times (total)



Signed Multiplication

Signed Multiplication

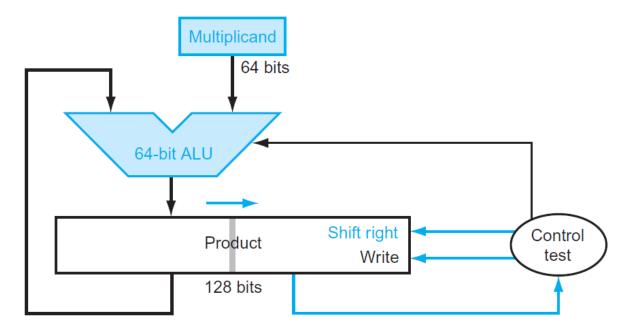
 Convert to Multiplicand and Multiplier to positive and remember the sign

Multiplicand	Multiplier	Result
-ve	+ve	-ve
+ve	-ve	-ve
+ve	+ve	+ve
-ve	-ve	+ve

If multiplicand and multiplier signs disagree, then the result is negative.

Optimized Multiplier

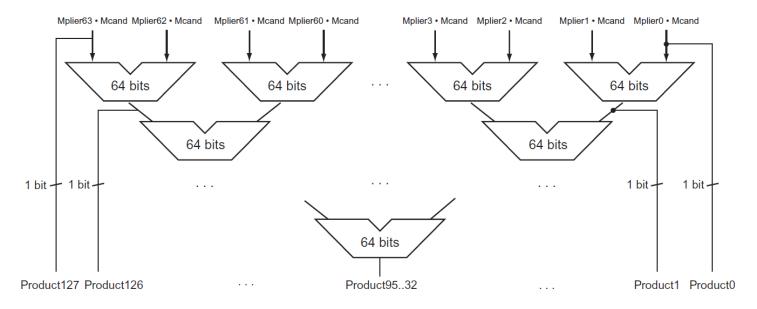
Perform steps in parallel: add/shift



- One cycle per partial-product addition
 - That's ok, if frequency of multiplications is low

Faster Multiplier

- Uses multiple adders
 - Cost/performance tradeoff



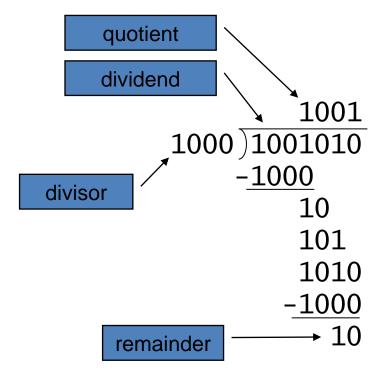
- Can be pipelined
 - Several multiplication performed in parallel

LEGv8 Multiplication

- Three multiply instructions:
 - MUL: multiply
 - Gives the lower 64 bits of the product
 - SMULH: signed multiply high
 - Gives the upper 64 bits of the product, assuming the operands are signed
 - UMULH: unsigned multiply high
 - Gives the upper 64 bits of the product, assuming the operands are unsigned

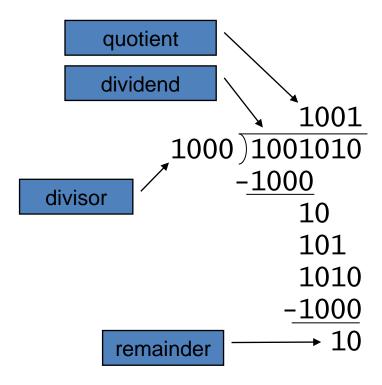
Instructions

Туре	Name
Arithmetic	ADD, SUB, MUL
Data transfer	LDUR, STUR
Arithmetic Immediate	ADDI, SUBI, ORRI, ANDI, EORI, MUL, SMULH, UMULH
Logical Operations	LSL, LSR, AND, ORR, EOR
Branches	B, CBZ, CBNZ, B.Cond
Set Condition Flag	ADDS, ADDIS, SUBS, SUBIS, ANDS, ANDIS

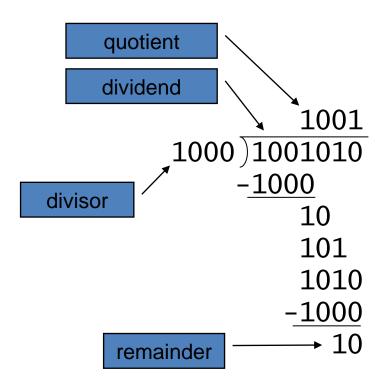


n-bit operands yield *n*-bit quotient and remainder

1. *n*-bit operands yield *n*-bit quotient and remainder

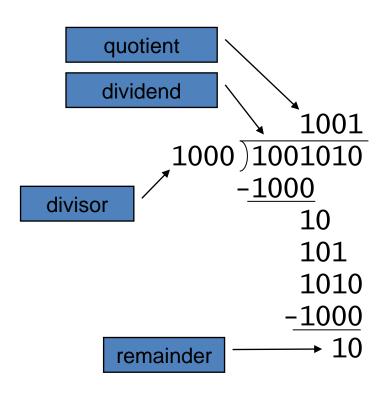


- n-bit operands yield n-bit quotient and remainder
- 2. Divisor goes in dividend either 0 times or 1 times.



- n-bit operands yield n-bit quotient and remainder
- 2. Divisor goes in dividend either 0 times or 1 times.
 - 1. If dividend-divisor ≥ 0 , then divisor goes 1 time
 - 2. Else divisor goes 0 times.

To design the division hardware, lets consider the dividend and the quotient to be 8 bits long, the divisor is 4 bits long.



Divisor register

1000 0000

Dividend: 1001010

• Divisor: 1000

Initialize Divisor register, with the divisor value in the left most significant bits

1001 1000)1001010 -1000 10 101 1010 -1000 10 UNIVERSITY of HOUSTON

Dividend: 1001010

Divisor: 1000

Divisor register 1000 0000

Initialize Divisor register, with the divisor value in the right most significant bits

Initialize remainder register, with the value of the dividend

Dividend: 1001010

Divisor: 1000

Initialize Divisor register, with the divisor value in the right most significant bits

- Initialize remainder register, with the value of the dividend
- Initialize Quotient register, 4 bits, with zeros

Divisor register 1000 0000

Remainder register 0100 1010

Quotient register 0000

Dividend: 1001010

Divisor: 1000

Initialize Divisor register, with the divisor value in the right most significant bits

- HW to shift right
- Initialize remainder register, with the value of the dividend
- Initialize Quotient register, 4 bits, with zeros
 - Shift left

Divisor register 1000 0000

Shift right Shift left Quotient register 0000

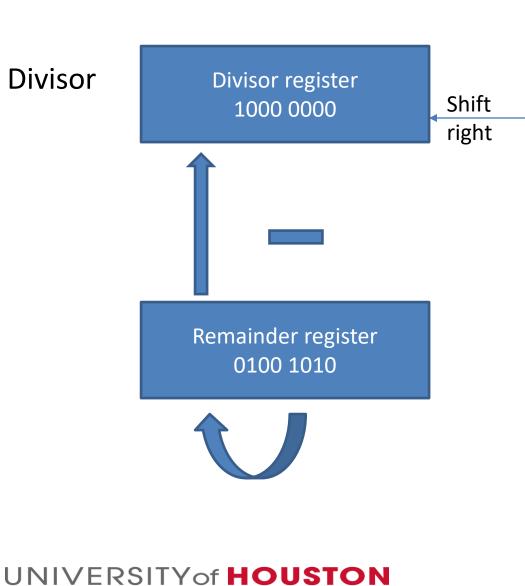
Remainder register 0100 1010

Iteration 1

(Dividend)

- 1. Remainder = Remainder Divisor
 - 1. If remainder < 0

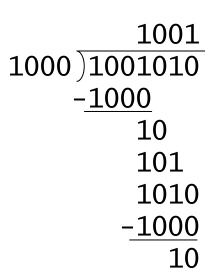
 $\begin{array}{r}
1001 \\
1000)1001010 \\
-\underline{1000} \\
10 \\
101 \\
1010 \\
-\underline{1000} \\
10
\end{array}$

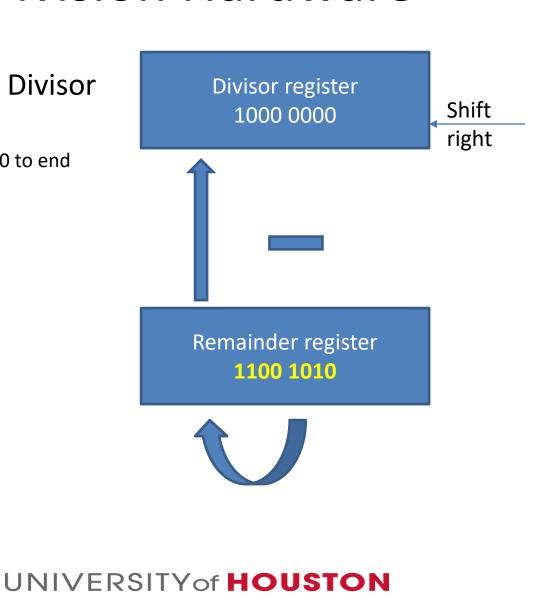


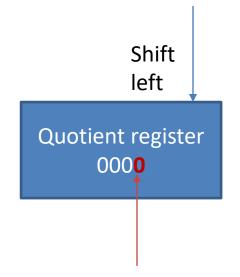
Shift left Quotient register 0000

Iteration 1

- 1. Remainder = Remainder Divisor
 - 1. If remainder < 0,
 - 1. Shift quotient to left, and add 0 to end







Iteration 1

- Remainder = Remainder Divisor
 - If remainder < 0,
 - Shift quotient to left, and add 0 to end
 - Add the remainder back to divisor, and restore value

Divisor register 1000 0000

Shift right



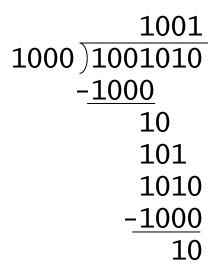


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Shift left Quotient register 0000

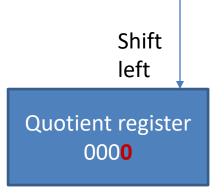
Iteration 1

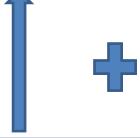
- 1. Remainder = Remainder Divisor
 - 1. If remainder < 0,
 - 1. Shift quotient to left, and add 0 to end
 - 2. Add the remainder back to divisor, and restore value
- 2. Shift Divisor to the right by 1 bit



Divisor register 1000 0000

Shift right



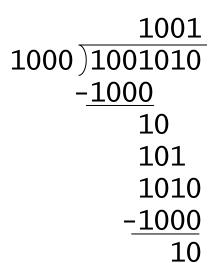


Remainder register 0100 1010



Iteration 1

- 1. Remainder = Remainder Divisor
 - 1. If remainder < 0,
 - 1. Shift quotient to left, and add 0 to end
 - 2. Add the remainder back to divisor, and restore value
- 2. Shift Divisor to the right by 1 bit



Divisor register 0100 0000

Shift right Shift left

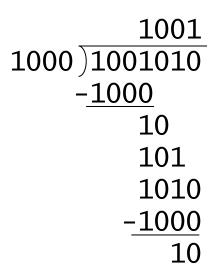
Quotient register
0000

Remainder register 0100 1010



Iteration 1

- 1. Remainder = Remainder Divisor
 - 1. If remainder < 0,
 - 1. Shift quotient to left, and add 0 to end
 - 2. Add the remainder back to divisor, and restore value
- 2. Shift Divisor to the right by 1 bit
- 3. Repeat 5 times total



Divisor register 0100 0000

Shift right Shift left Quotient register 0000

Remainder register 0100 1010



Shift

right

Division Hardware

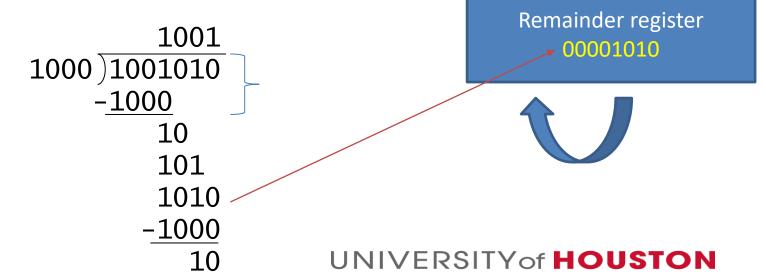
Divisor register

0100 0000

Iteration 2

1. Remainder = Remainder - Divisor

- 1. If remainder < 0,
 - 1. Shift quotient to left, and add 0 to end
 - 2. Add the remainder back to divisor, and restore value
- 2. Shift Divisor to the right by 1 bit
- 3. Repeat 5 times total



Shift left Quotient register 0000

Iteration 2

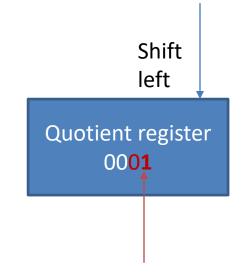
- 1. Remainder = Remainder Divisor
 - 1. If remainder < 0,
 - 1. Shift quotient to left, and add 0 to end
 - 2. Add the remainder back to divisor, and restore value
 - 2. If remainder > 0,
 - 1. Shift quotient to left, and add 1 to end
- 2. Shift Divisor to the right by 1 bit
- 3. Repeat 5 times 1001 1000)1001010 -1000 10 101 1010 -1000

Divisor register 0100 0000

Shift right

Remainder register 00001010





Iteration 2

- 1. Remainder = Remainder Divisor
 - 1. If remainder < 0,
 - 1. Shift quotient to left, and add 0 to end
 - 2. Add the remainder back to devisor, and restore value
 - 2. If remainder > 0,
 - 1. Shift quotient to left, and add 1 to end
- 2. Shift Divisor to the right by 1 bit
- 3. Repeat 5 times 1001 1000)1001010 -1000 10 101 1010 -1000

Divisor register 0010 0000

Shift right Quotient register 00**01**

Shift

Remainder register 00001010



Iteration 3

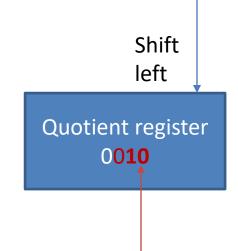
- 1. Remainder = Remainder Divisor
 - 1. If remainder < 0,
 - 1. Shift quotient to left, and add 0 to end
 - 2. Add the remainder back to devisor, and restore value
 - 2. If remainder > 0,
 - 1. Shift quotient to left, and add 1 to end
- 2. Shift Divisor to the right by 1 bit
- 3. Repeat 5 times 1001 1000)1001010 -1000 10 101 1010 -1000

Divisor register 0001 0000

Shift right

Remainder register 00001010





Iteration 4

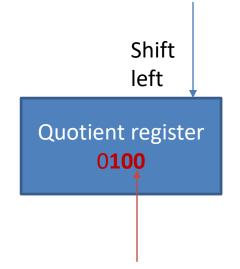
- 1. Remainder = Remainder Divisor
 - 1. If remainder < 0,
 - 1. Shift quotient to left, and add 0 to end
 - 2. Add the remainder back to devisor, and restore value
 - 2. If remainder > 0,
 - 1. Shift quotient to left, and add 1 to end
- 2. Shift Divisor to the right by 1 bit
- 3. Repeat 5 times 1001 1000)1001010 -1000 10 101 1010 -1000

Divisor register 0000 **1000**

Shift right

Remainder register 00001010





Iteration 5

1. Remainder = Remainder - Divisor

- 1. If remainder < 0,
 - 1. Shift quotient to left, and add 0 to end
 - 2. Add the remainder back to devisor, and restore value
- 2. If remainder > 0,
 - 1. Shift quotient to left, and add 1 to end

2. Shift Divisor to the right by 1 bit

3. Repeat 5 times 1001 1000)1001010 -1000 10 101 1010 -1000

Divisor register 0000 **1000**

Shift right

Remainder register 00000010



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Shift left

Quotient register **1001**

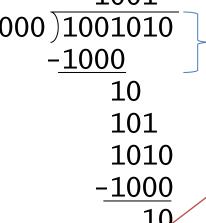
Shift

right

Division Hardware

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- 1. Remainder = Remainder Divisor
 - 1. If remainder < 0,
 - 1. Shift quotient to left, and add 0 to end
 - 2. Add the remainder back to devisor, and restore value
 - 2. If remainder > 0,
 - 1. Shift quotient to left, and add 1 to end
- 2. Shift Divisor to the right by 1 bit
- 3. Repeat 5 times 1001 1000 1001010



Remainder register 00000010

Divisor register

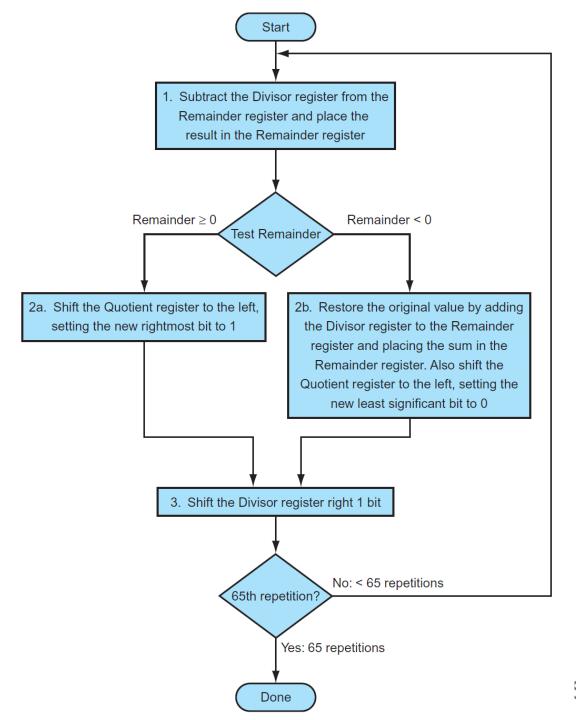
0000 1000

Quotient register

Shift

left

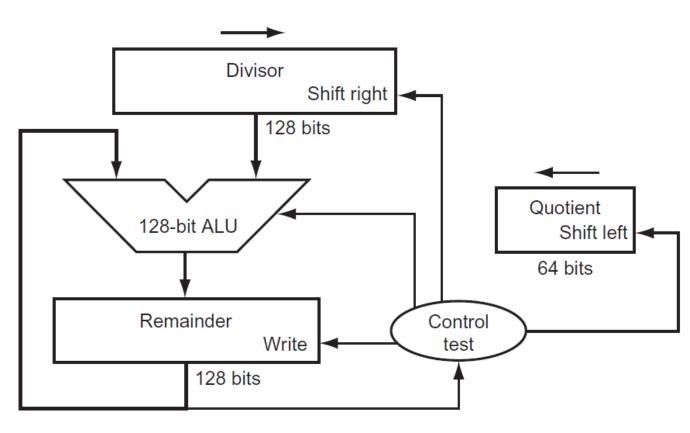
_ 1001



Division Flowchart

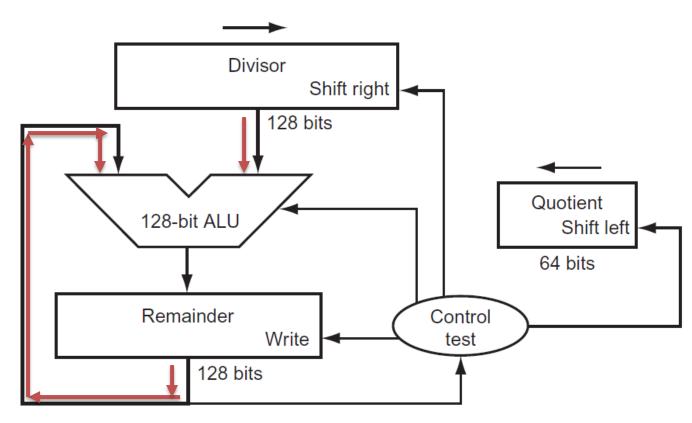


- 1. Remainder = Remainder Divisor
 - 1. If remainder < 0,
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 - 2. If remainder > 0,
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- 2. Shift Divisor to the right by 1 bit
- 3. Repeat 5 times

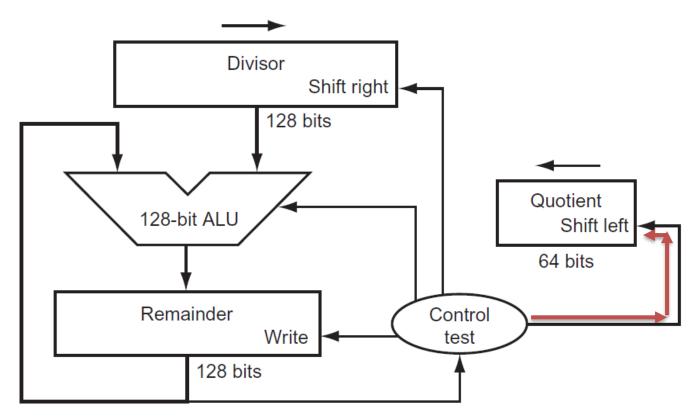


1. Remainder = Remainder - Divisor

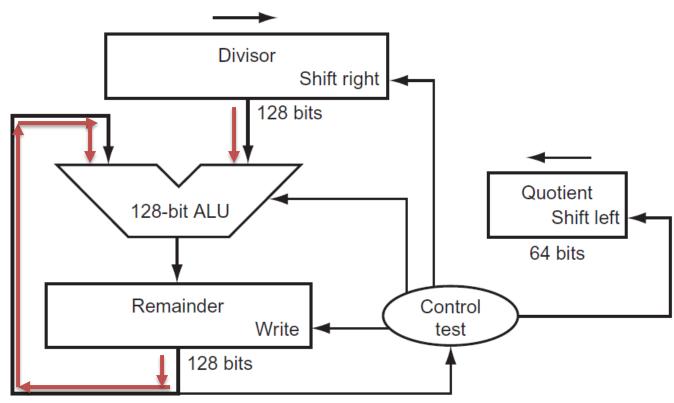
- 1. If remainder < 0,
 - 1. Shift quotient to left, and add 0 to end
 - 2. Add the remainder back to devisor, and restore value
- 2. If remainder > 0,
 - 1. Shift quotient to left, and add 1 to end
- 2. Shift Divisor to the right by 1 bit
- 3. Repeat 5 times



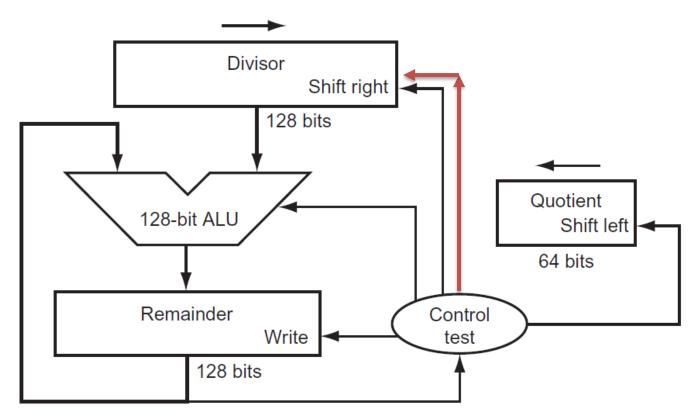
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- 2. Shift Divisor to the right by 1 bit
- 3. Repeat 5 times



Signed Division

Convert to Dividend and Divisor to positive and remember the sign

Dividend	Divisor	Quotient
-ve	+ve	-ve
+ve	-ve	-ve
+ve	+ve	+ve
-ve	-ve	+ve

If Dividend and Divisor signs disagree, then the quotient is negative.

Remainder has the same sign as dividend

Faster Division

- Can't use parallel hardware as in multiplier
 - Subtraction is conditional on sign of remainder
- Faster dividers (e.g. SRT division) generate multiple quotient bits per step
 - Still require multiple steps

LEGv8 Division

- Two divide instructions:
 - SDIV: Signed divide
 - UDIV: unsigned divide

Instructions

Туре	Name
Arithmetic	ADD, SUB, MUL
Data transfer	LDUR, STUR
Arithmetic Immediate	ADDI, SUBI, ORRI, ANDI, EORI, MUL, SMULH, UMULH, SDIV, UDIV
Logical Operations	LSL, LSR, AND, ORR, EOR
Branches	B, CBZ, CBNZ, B.Cond
Set Condition Flag	ADDS, ADDIS, SUBS, SUBIS, ANDS, ANDIS

Floating Point numbers