Synthesis Report

Fri Jul 24 15:26:49 2020

```
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.09 secs

--> Parameter xsthdpdir set to xst
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.09 secs

--> Reading design: cordic.prj
TABLE OF CONTENTS
  1) Synthesis Options Summary
  2) HDL Parsing
  3) HDL Elaboration
  4) HDL Synthesis
       4.1) HDL Synthesis Report
  5) Advanced HDL Synthesis
       5.1) Advanced HDL Synthesis Report
  6) Low Level Synthesis
  7) Partition Report
  8) Design Summary
       8.1) Primitive and Black Box Usage
       8.2) Device utilization summary
       8.3) Partition Resource Summary
       8.4) Timing Report
            8.4.1) Clock Information
            8.4.2) Asynchronous Control Signals Information
            8.4.3) Timing Summary
            8.4.4) Timing Details
            8.4.5) Cross Clock Domains Report
=========================================================================
*                     Synthesis Options Summary                         *
=========================================================================
---- Source Parameters
Input File Name                    : "cordic.prj"
Ignore Synthesis Constraint File   : NO
---- Target Parameters
Output File Name                   : "cordic"
Output Format                      : NGC
Target Device                      : xc7a100t-3-csg324
---- Source Options
Top Module Name                    : cordic
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No
---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 32
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES
---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5
=========================================================================
=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Analyzing Verilog file "C:\Users\Tarlan\Desktop\DSD\CORDIC\verilog\cordic_stage.v" into library work
Parsing module .
Analyzing Verilog file "C:\Users\Tarlan\Desktop\DSD\CORDIC\verilog\cordic_top.v" into library work
```

```
Parsing module .
=========================================================================
*                          HDL Elaboration                              *
=========================================================================
Elaborating module .
WARNING:HDLCompiler:413 - "C:\Users\Tarlan\Desktop\DSD\CORDIC\verilog\cordic_top.v" Line 39: Result of 33-bit expression is truncated to fit
WARNING:HDLCompiler:413 - "C:\Users\Tarlan\Desktop\DSD\CORDIC\verilog\cordic_top.v" Line 41: Result of 33-bit expression is truncated to fit
Elaborating module .
WARNING:HDLCompiler:413 - "C:\Users\Tarlan\Desktop\DSD\CORDIC\verilog\cordic_stage.v" Line 19: Result of 4-bit expression is truncated to fi
=========================================================================
*                           HDL Synthesis                               *
=========================================================================
Synthesizing Unit .
    Related source file is "C:\Users\Tarlan\Desktop\DSD\CORDIC\verilog\cordic_top.v".
INFO:Xst:3210 - "C:\Users\Tarlan\Desktop\DSD\CORDIC\verilog\cordic_top.v" line 129: Output port  of the instance  is unconnected or connecte
    Found 16-bit register for signal .
    Found 16-bit register for signal .
    Found 16-bit register for signal .
    Found 16-bit register for signal .
    Found 16-bit register for signal .
    Found 1-bit register for signal .
    Found 15-bit subtractor for signal  created at line 82.
    Found 16-bit subtractor for signal  created at line 89.
    Found 15-bit comparator lessequal for signal  created at line 70
    Summary:
        inferred   2 Adder/Subtractor(s).
        inferred  81 D-type flip-flop(s).
        inferred   1 Comparator(s).
        inferred  16 Multiplexer(s).
Unit  synthesized.
Synthesizing Unit .
    Related source file is "".
    Found 42-bit adder for signal  created at line 0.
    Found 42-bit adder for signal  created at line 0.
    Found 41-bit adder for signal  created at line 0.
    Found 41-bit adder for signal  created at line 0.
    Found 40-bit adder for signal  created at line 0.
    Found 40-bit adder for signal  created at line 0.
    Found 39-bit adder for signal  created at line 0.
    Found 39-bit adder for signal  created at line 0.
    Found 38-bit adder for signal  created at line 0.
    Found 38-bit adder for signal  created at line 0.
    Found 37-bit adder for signal  created at line 0.
    Found 37-bit adder for signal  created at line 0.
    Found 36-bit adder for signal  created at line 0.
    Found 36-bit adder for signal  created at line 0.
    Found 35-bit adder for signal  created at line 0.
    Found 35-bit adder for signal  created at line 0.
    Found 34-bit adder for signal  created at line 0.
    Found 34-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 33-bit adder for signal  created at line 0.
    Found 42-bit comparator lessequal for signal  created at line 0
    Found 41-bit comparator lessequal for signal  created at line 0
```

```
    Found 40-bit comparator lessequal for signal  created at line 0
    Found 39-bit comparator lessequal for signal  created at line 0
    Found 38-bit comparator lessequal for signal  created at line 0
    Found 37-bit comparator lessequal for signal  created at line 0
    Found 36-bit comparator lessequal for signal  created at line 0
    Found 35-bit comparator lessequal for signal  created at line 0
    Found 34-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Found 33-bit comparator lessequal for signal  created at line 0
    Summary:
        inferred  66 Adder/Subtractor(s).
        inferred  34 Comparator(s).
        inferred 993 Multiplexer(s).
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:\Users\Tarlan\Desktop\DSD\CORDIC\verilog\cordic_stage.v".
    Found 16-bit register for signal .
    Found 16-bit register for signal .
    Found 16-bit register for signal .
    Found 1-bit register for signal .
    Found 16-bit subtractor for signal  created at line 80.
    Found 15-bit subtractor for signal  created at line 114.
    Found 15-bit subtractor for signal  created at line 115.
    Found 15-bit subtractor for signal  created at line 120.
    Found 15-bit subtractor for signal  created at line 121.
    Found 15-bit subtractor for signal  created at line 126.
    Found 15-bit subtractor for signal  created at line 127.
    Found 3-bit adder for signal  created at line 19.
    Found 15-bit adder for signal  created at line 116.
    Found 15-bit adder for signal  created at line 122.
    Found 15-bit adder for signal  created at line 128.
    Found 15-bit shifter logical right for signal  created at line 115
    Found 15-bit shifter logical right for signal  created at line 122
WARNING:Xst:737 - Found 1-bit latch for signal >. Latches may be generated from incomplete case or if statements. We do not recommend the us
WARNING:Xst:737 - Found 1-bit latch for signal >. Latches may be generated from incomplete case or if statements. We do not recommend the us
WARNING:Xst:737 - Found 1-bit latch for signal >. Latches may be generated from incomplete case or if statements. We do not recommend the us
WARNING:Xst:737 - Found 1-bit latch for signal >. Latches may be generated from incomplete case or if statements. We do not recommend the us
WARNING:Xst:737 - Found 1-bit latch for signal >. Latches may be generated from incomplete case or if statements. We do not recommend the us
WARNING:Xst:737 - Found 1-bit latch for signal >. Latches may be generated from incomplete case or if statements. We do not recommend the us
WARNING:Xst:737 - Found 1-bit latch for signal >. Latches may be generated from incomplete case or if statements. We do not recommend the us
WARNING:Xst:737 - Found 1-bit latch for signal >. Latches may be generated from incomplete case or if statements. We do not recommend the us
WARNING:Xst:737 - Found 1-bit latch for signal >. Latches may be generated from incomplete case or if statements. We do not recommend the us
    Found 15-bit comparator greater for signal  created at line 113
    Found 15-bit comparator greater for signal  created at line 119
    Found 15-bit comparator greater for signal  created at line 125
    Summary:
        inferred  11 Adder/Subtractor(s).
        inferred  49 D-type flip-flop(s).
        inferred   9 Latch(s).
        inferred   3 Comparator(s).
        inferred  18 Multiplexer(s).
        inferred   2 Combinational logic shifter(s).
Unit  synthesized.
=========================================================================
HDL Synthesis Report
Macro Statistics
# Adders/Subtractors                                   : 222
 15-bit adder                                          : 24
 15-bit subtractor                                     : 49
 16-bit subtractor                                     : 9
 3-bit adder                                           : 8
 33-bit adder                                          : 96
 34-bit adder                                          : 4
 35-bit adder                                          : 4
 36-bit adder                                          : 4
 37-bit adder                                          : 4
 38-bit adder                                          : 4
 39-bit adder                                          : 4
 40-bit adder                                          : 4
 41-bit adder                                          : 4
 42-bit adder                                          : 4
# Registers                                            : 38
 1-bit register                                        : 9
 16-bit register                                       : 29
# Latches                                              : 72
 1-bit latch                                           : 72
# Comparators                                          : 93
```

```
 15-bit comparator greater                             : 24
 15-bit comparator lessequal                           : 1
 33-bit comparator lessequal                           : 50
 34-bit comparator lessequal                           : 2
 35-bit comparator lessequal                           : 2
 36-bit comparator lessequal                           : 2
 37-bit comparator lessequal                           : 2
 38-bit comparator lessequal                           : 2
 39-bit comparator lessequal                           : 2
 40-bit comparator lessequal                           : 2
 41-bit comparator lessequal                           : 2
 42-bit comparator lessequal                           : 2
# Multiplexers                                         : 2146
 1-bit 2-to-1 multiplexer                              : 1984
 16-bit 2-to-1 multiplexer                             : 156
 33-bit 2-to-1 multiplexer                             : 6
# Logic shifters                                       : 16
 15-bit shifter logical right                          : 16
# Xors                                                 : 8
 1-bit xor2                                            : 8
=========================================================================
=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================
INFO:Xst:2261 - The FF/Latch  in Unit  is equivalent to the following 4 FFs/Latches, which will be removed :
INFO:Xst:2261 - The FF/Latch  in Unit  is equivalent to the following 3 FFs/Latches, which will be removed :
WARNING:Xst:1710 - FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be trimmed during the optimization
WARNING:Xst:1710 - FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be trimmed during the optimization
WARNING:Xst:1710 - FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be trimmed during the optimization
WARNING:Xst:1710 - FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be trimmed during the optimization
WARNING:Xst:1710 - FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be trimmed during the optimization
WARNING:Xst:1710 - FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be trimmed during the optimization
WARNING:Xst:1710 - FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be trimmed during the optimization
WARNING:Xst:1710 - FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be trimmed during the optimization
WARNING:Xst:1710 - FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be trimmed during the optimization
=========================================================================
Advanced HDL Synthesis Report
Macro Statistics
# Adders/Subtractors                                   : 155
 15-bit adder                                          : 24
 15-bit subtractor                                     : 49
 16-bit subtractor                                     : 9
 3-bit adder                                           : 7
 33-bit adder carry in                                 : 66
# Registers                                            : 473
 Flip-Flops                                            : 473
# Comparators                                          : 93
 15-bit comparator greater                             : 24
 15-bit comparator lessequal                           : 1
 33-bit comparator lessequal                           : 50
 34-bit comparator lessequal                           : 2
 35-bit comparator lessequal                           : 2
 36-bit comparator lessequal                           : 2
 37-bit comparator lessequal                           : 2
 38-bit comparator lessequal                           : 2
 39-bit comparator lessequal                           : 2
 40-bit comparator lessequal                           : 2
 41-bit comparator lessequal                           : 2
 42-bit comparator lessequal                           : 2
# Multiplexers                                         : 2176
 1-bit 2-to-1 multiplexer                              : 2016
 16-bit 2-to-1 multiplexer                             : 154
 33-bit 2-to-1 multiplexer                             : 6
# Logic shifters                                       : 16
 15-bit shifter logical right                          : 16
# Xors                                                 : 8
 1-bit xor2                                            : 8
=========================================================================
=========================================================================
*                         Low Level Synthesis                           *
=========================================================================
WARNING:Xst:1710 - FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be trimmed during the optimization
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1710 - FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be trimmed during the optimization
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
```

```
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 1 in block . This FF/Latch will be
Optimizing unit  ...
Optimizing unit  ...
INFO:Xst:2261 - The FF/Latch  in Unit  is equivalent to the following FF/Latch, which will be removed :
Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block cordic, actual ratio is 6.
Final Macro Processing ...
=========================================================================
Final Register Report
Macro Statistics
# Registers                                            : 472
 Flip-Flops                                            : 472
=========================================================================
=========================================================================
*                            Partition Report                           *
=========================================================================
Partition Implementation Status
-------------------------------
  No Partitions were found in this design.
-------------------------------
=========================================================================
*                             Design Summary                            *
=========================================================================
Top Level Output File Name         : cordic.ngc
Primitive and Black Box Usage:
------------------------------
# BELS                             : 8084
#      GND                         : 1
#      INV                         : 488
#      LUT1                        : 265
#      LUT2                        : 641
#      LUT3                        : 404
#      LUT4                        : 427
#      LUT5                        : 1486
#      LUT6                        : 202
#      MUXCY                       : 2227
#      MUXF7                       : 9
#      VCC                         : 1
#      XORCY                       : 1933
# FlipFlops/Latches                : 472
#      FDC                         : 471
#      FDE                         : 1
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 82
#      IBUF                        : 50
#      OBUF                        : 32
Device utilization summary:
---------------------------
Selected Device : 7a100tcsg324-3
Slice Logic Utilization:
 Number of Slice Registers:             472  out of  126800     0%
 Number of Slice LUTs:                 3913  out of  63400     6%
    Number used as Logic:              3913  out of  63400     6%
Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:   3943
   Number with an unused Flip Flop:    3471  out of   3943    88%
```

```
   Number with an unused LUT:             30  out of   3943     0%
   Number of fully used LUT-FF pairs:    442  out of   3943    11%
   Number of unique control sets:          2
IO Utilization:
 Number of IOs:                           83
 Number of bonded IOBs:                   83  out of    210    39%
Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                 1  out of     32     3%
---------------------------
Partition Resource Summary:
---------------------------
  No Partitions were found in this design.
---------------------------
=========================================================================
Timing Report
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.
Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clock                              | BUFGP                  | 472   |
-----------------------------------+------------------------+-------+
Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design
Timing Summary:
---------------
Speed Grade: -3
   Minimum period: 29.558ns (Maximum Frequency: 33.831MHz)
   Minimum input arrival time before clock: 2.875ns
   Maximum output required time after clock: 0.640ns
   Maximum combinational path delay: No path found
Timing Details:
---------------
All values displayed in nanoseconds (ns)
=========================================================================
Timing constraint: Default period analysis for Clock 'clock'
  Clock period: 29.558ns (frequency: 33.831MHz)
  Total number of paths / destination ports: 23840060485194827000000000000 / 423
-------------------------------------------------------------------------
Delay:               29.558ns (Levels of Logic = 96)
  Source:            stages[7].s0/y_out_6 (FF)
  Destination:       y_or_size_out_0 (FF)
  Source Clock:      clock rising
  Destination Clock: clock rising
  Data Path: stages[7].s0/y_out_6 to y_or_size_out_0
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q             6   0.361   0.534  stages[7].s0/y_out_6 (stages[7].s0/y_out_6)
     LUT4:I1->O           1   0.097   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<14>_lut<0> (holdery[24]_PWR_1_o_div_6/Mcompar_o<14>_lut<0>
     MUXCY:S->O           1   0.353   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<14>_cy<0> (holdery[24]_PWR_1_o_div_6/Mcompar_o<14>_cy<0>)
     MUXCY:CI->O          1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<14>_cy<1> (holdery[24]_PWR_1_o_div_6/Mcompar_o<14>_cy<1>)
     MUXCY:CI->O          1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<14>_cy<2> (holdery[24]_PWR_1_o_div_6/Mcompar_o<14>_cy<2>)
     MUXCY:CI->O          1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<14>_cy<3> (holdery[24]_PWR_1_o_div_6/Mcompar_o<14>_cy<3>)
     MUXCY:CI->O          1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<14>_cy<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<14>_cy<4>)
     MUXCY:CI->O          1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<14>_cy<5> (holdery[24]_PWR_1_o_div_6/Mcompar_o<14>_cy<5>)
     MUXCY:CI->O         97   0.253   0.496  holdery[24]_PWR_1_o_div_6/Mcompar_o<14>_cy<6> (n0086<14>)
     LUT2:I0->O           2   0.097   0.688  holdery[24]_PWR_1_o_div_6/Mmux_a[0]_a[32]_MUX_1080_o1211 (holdery[24]_PWR_1_o_div_6/a[29]_a[32
     LUT5:I0->O           0   0.097   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<13>_lutdi5 (holdery[24]_PWR_1_o_div_6/Mcompar_o<13>_lutdi5
     MUXCY:DI->O          1   0.337   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<13>_cy<5> (holdery[24]_PWR_1_o_div_6/Mcompar_o<13>_cy<5>)
     MUXCY:CI->O         73   0.253   0.408  holdery[24]_PWR_1_o_div_6/Mcompar_o<13>_cy<6> (n0086<13>)
     LUT5:I4->O           5   0.097   0.702  holdery[24]_PWR_1_o_div_6/Mmux_a[0]_a[32]_MUX_1113_o1131 (holdery[24]_PWR_1_o_div_6/a[21]_a[32
     LUT5:I0->O           1   0.097   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<12>_lut<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<12>_lut<4>
     MUXCY:S->O           1   0.353   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<12>_cy<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<12>_cy<4>)
     MUXCY:CI->O          1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<12>_cy<5> (holdery[24]_PWR_1_o_div_6/Mcompar_o<12>_cy<5>)
     MUXCY:CI->O         79   0.253   0.409  holdery[24]_PWR_1_o_div_6/Mcompar_o<12>_cy<6> (n0086<12>)
     LUT3:I2->O           3   0.097   0.693  holdery[24]_PWR_1_o_div_6/Mmux_a[0]_a[32]_MUX_1146_o1121 (holdery[24]_PWR_1_o_div_6/a[20]_a[32
     LUT5:I0->O           1   0.097   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<11>_lut<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<11>_lut<4>
     MUXCY:S->O           1   0.353   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<11>_cy<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<11>_cy<4>)
     MUXCY:CI->O          1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<11>_cy<5> (holdery[24]_PWR_1_o_div_6/Mcompar_o<11>_cy<5>)
     MUXCY:CI->O         72   0.253   0.408  holdery[24]_PWR_1_o_div_6/Mcompar_o<11>_cy<6> (n0086<11>)
     LUT3:I2->O           4   0.097   0.697  holdery[24]_PWR_1_o_div_6/Mmux_a[0]_a[32]_MUX_1179_o1101 (holdery[24]_PWR_1_o_div_6/a[19]_a[32
     LUT5:I0->O           1   0.097   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<10>_lut<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<10>_lut<4>
     MUXCY:S->O           1   0.353   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<10>_cy<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<10>_cy<4>)
     MUXCY:CI->O          1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<10>_cy<5> (holdery[24]_PWR_1_o_div_6/Mcompar_o<10>_cy<5>)
     MUXCY:CI->O          1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<10>_cy<6> (holdery[24]_PWR_1_o_div_6/Mcompar_o<10>_cy<6>)
     MUXCY:CI->O         86   0.253   0.410  holdery[24]_PWR_1_o_div_6/Mcompar_o<10>_cy<7> (n0086<10>)
     LUT3:I2->O           3   0.097   0.693  holdery[24]_PWR_1_o_div_6/Mmux_a[0]_a[32]_MUX_1212_o191 (holdery[24]_PWR_1_o_div_6/a[18]_a[32]
     LUT5:I0->O           1   0.097   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<9>_lut<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<9>_lut<4>)
     MUXCY:S->O           1   0.353   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<9>_cy<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<9>_cy<4>)
     MUXCY:CI->O          1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<9>_cy<5> (holdery[24]_PWR_1_o_div_6/Mcompar_o<9>_cy<5>)
     MUXCY:CI->O          1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<9>_cy<6> (holdery[24]_PWR_1_o_div_6/Mcompar_o<9>_cy<6>)
     MUXCY:CI->O         77   0.253   0.409  holdery[24]_PWR_1_o_div_6/Mcompar_o<9>_cy<7> (n0086<9>)
     LUT3:I2->O           4   0.097   0.697  holdery[24]_PWR_1_o_div_6/Mmux_a[0]_a[32]_MUX_1245_o181 (holdery[24]_PWR_1_o_div_6/a[17]_a[32]
     LUT5:I0->O           1   0.097   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<8>_lut<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<8>_lut<4>)
     MUXCY:S->O           1   0.353   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<8>_cy<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<8>_cy<4>)
     MUXCY:CI->O          1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<8>_cy<5> (holdery[24]_PWR_1_o_div_6/Mcompar_o<8>_cy<5>)
     MUXCY:CI->O          1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<8>_cy<6> (holdery[24]_PWR_1_o_div_6/Mcompar_o<8>_cy<6>)
     MUXCY:CI->O         94   0.253   0.412  holdery[24]_PWR_1_o_div_6/Mcompar_o<8>_cy<7> (n0086<8>)
     LUT3:I2->O           3   0.097   0.693  holdery[24]_PWR_1_o_div_6/Mmux_a[0]_a[32]_MUX_1278_o171 (holdery[24]_PWR_1_o_div_6/a[16]_a[32]
     LUT5:I0->O           1   0.097   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<7>_lut<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<7>_lut<4>)
     MUXCY:S->O           1   0.353   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<7>_cy<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<7>_cy<4>)
     MUXCY:CI->O          1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<7>_cy<5> (holdery[24]_PWR_1_o_div_6/Mcompar_o<7>_cy<5>)
     MUXCY:CI->O          1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<7>_cy<6> (holdery[24]_PWR_1_o_div_6/Mcompar_o<7>_cy<6>)
     MUXCY:CI->O         85   0.253   0.410  holdery[24]_PWR_1_o_div_6/Mcompar_o<7>_cy<7> (holdery[24]_PWR_1_o_div_6/Mcompar_o<6>_lutdi)
     LUT3:I2->O           4   0.097   0.697  holdery[24]_PWR_1_o_div_6/Mmux_a[0]_a[32]_MUX_1311_o161 (holdery[24]_PWR_1_o_div_6/a[15]_a[32]
```

```
    LUT5:I0->O            1   0.097   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<6>_lut<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<6>_lut<4>)
    MUXCY:S->O            1   0.353   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<6>_cy<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<6>_cy<4>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<6>_cy<5> (holdery[24]_PWR_1_o_div_6/Mcompar_o<6>_cy<5>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<6>_cy<6> (holdery[24]_PWR_1_o_div_6/Mcompar_o<6>_cy<6>)
    MUXCY:CI->O         106   0.253   0.413  holdery[24]_PWR_1_o_div_6/Mcompar_o<6>_cy<7> (holdery[24]_PWR_1_o_div_6/Mcompar_o<5>_lutdi)
    LUT3:I2->O            3   0.097   0.693  holdery[24]_PWR_1_o_div_6/Mmux_a[0]_a[32]_MUX_1344_o151 (holdery[24]_PWR_1_o_div_6/a[14]_a[32]
    LUT5:I0->O            1   0.097   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<5>_lut<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<5>_lut<4>)
    MUXCY:S->O            1   0.353   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<5>_cy<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<5>_cy<4>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<5>_cy<5> (holdery[24]_PWR_1_o_div_6/Mcompar_o<5>_cy<5>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<5>_cy<6> (holdery[24]_PWR_1_o_div_6/Mcompar_o<5>_cy<6>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<5>_cy<7> (holdery[24]_PWR_1_o_div_6/Mcompar_o<5>_cy<7>)
    MUXCY:CI->O          92   0.253   0.411  holdery[24]_PWR_1_o_div_6/Mcompar_o<5>_cy<8> (holdery[24]_PWR_1_o_div_6/Mcompar_o<4>_lutdi)
    LUT3:I2->O            4   0.097   0.697  holdery[24]_PWR_1_o_div_6/Mmux_a[0]_a[32]_MUX_1377_o141 (holdery[24]_PWR_1_o_div_6/a[13]_a[32]
    LUT5:I0->O            1   0.097   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<4>_lut<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<4>_lut<4>)
    MUXCY:S->O            1   0.353   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<4>_cy<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<4>_cy<4>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<4>_cy<5> (holdery[24]_PWR_1_o_div_6/Mcompar_o<4>_cy<5>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<4>_cy<6> (holdery[24]_PWR_1_o_div_6/Mcompar_o<4>_cy<6>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<4>_cy<7> (holdery[24]_PWR_1_o_div_6/Mcompar_o<4>_cy<7>)
    MUXCY:CI->O         113   0.253   0.414  holdery[24]_PWR_1_o_div_6/Mcompar_o<4>_cy<8> (holdery[24]_PWR_1_o_div_6/Mcompar_o<3>_lutdi)
    LUT3:I2->O            4   0.097   0.697  holdery[24]_PWR_1_o_div_6/Mmux_a[0]_a[32]_MUX_1410_o133 (holdery[24]_PWR_1_o_div_6/a[12]_a[32]
    LUT5:I0->O            1   0.097   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<3>_lut<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<3>_lut<4>)
    MUXCY:S->O            1   0.353   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<3>_cy<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<3>_cy<4>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<3>_cy<5> (holdery[24]_PWR_1_o_div_6/Mcompar_o<3>_cy<5>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<3>_cy<6> (holdery[24]_PWR_1_o_div_6/Mcompar_o<3>_cy<6>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<3>_cy<7> (holdery[24]_PWR_1_o_div_6/Mcompar_o<3>_cy<7>)
    MUXCY:CI->O         117   0.253   0.415  holdery[24]_PWR_1_o_div_6/Mcompar_o<3>_cy<8> (holdery[24]_PWR_1_o_div_6/Mcompar_o<2>_lutdi)
    LUT3:I2->O            3   0.097   0.693  holdery[24]_PWR_1_o_div_6/Mmux_n273334 (holdery[24]_PWR_1_o_div_6/n2733<11>)
    LUT5:I0->O            1   0.097   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<2>_lut<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<2>_lut<4>)
    MUXCY:S->O            1   0.353   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<2>_cy<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<2>_cy<4>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<2>_cy<5> (holdery[24]_PWR_1_o_div_6/Mcompar_o<2>_cy<5>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<2>_cy<6> (holdery[24]_PWR_1_o_div_6/Mcompar_o<2>_cy<6>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<2>_cy<7> (holdery[24]_PWR_1_o_div_6/Mcompar_o<2>_cy<7>)
    MUXCY:CI->O          94   0.253   0.412  holdery[24]_PWR_1_o_div_6/Mcompar_o<2>_cy<8> (holdery[24]_PWR_1_o_div_6/Mcompar_o<1>_lutdi)
    LUT3:I2->O            2   0.097   0.688  holdery[24]_PWR_1_o_div_6/Mmux_n273723 (holdery[24]_PWR_1_o_div_6/n2737<10>)
    LUT5:I0->O            1   0.097   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<1>_lut<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<1>_lut<4>)
    MUXCY:S->O            1   0.353   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<1>_cy<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<1>_cy<4>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<1>_cy<5> (holdery[24]_PWR_1_o_div_6/Mcompar_o<1>_cy<5>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<1>_cy<6> (holdery[24]_PWR_1_o_div_6/Mcompar_o<1>_cy<6>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<1>_cy<7> (holdery[24]_PWR_1_o_div_6/Mcompar_o<1>_cy<7>)
    MUXCY:CI->O          33   0.253   0.402  holdery[24]_PWR_1_o_div_6/Mcompar_o<1>_cy<8> (holdery[24]_PWR_1_o_div_6/Mcompar_o<0>_lutdi)
    LUT5:I4->O            2   0.097   0.688  holdery[24]_PWR_1_o_div_6/Mmux_n2604331 (holdery[24]_PWR_1_o_div_6/n2604<9>)
    LUT5:I0->O            1   0.097   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<0>_lut<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<0>_lut<4>)
    MUXCY:S->O            1   0.353   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<0>_cy<4> (holdery[24]_PWR_1_o_div_6/Mcompar_o<0>_cy<4>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<0>_cy<5> (holdery[24]_PWR_1_o_div_6/Mcompar_o<0>_cy<5>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<0>_cy<6> (holdery[24]_PWR_1_o_div_6/Mcompar_o<0>_cy<6>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<0>_cy<7> (holdery[24]_PWR_1_o_div_6/Mcompar_o<0>_cy<7>)
    MUXCY:CI->O           1   0.023   0.000  holdery[24]_PWR_1_o_div_6/Mcompar_o<0>_cy<8> (holdery[24]_PWR_1_o_div_6/Mcompar_o<0>_cy<8>)
    MUXCY:CI->O           1   0.253   0.295  holdery[24]_PWR_1_o_div_6/Mcompar_o<0>_cy<9> (n0086<0>)
    LUT3:I2->O            1   0.097   0.000  mux1611 (outx[15]_outy[15]_mux_9_OUT<0>)
    FDC:D                     0.008          y_or_size_out_0
    ----------------------------------------
    Total                    29.558ns (13.181ns logic, 16.377ns route)
                                      (44.6% logic, 55.4% route)

==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clock'
  Total number of paths / destination ports: 1583 / 521
--------------------------------------------------------------------------
Offset:              2.875ns (Levels of Logic = 5)
  Source:            rotate_amount<14> (PAD)
  Destination:       z_in_4 (FF)
  Destination Clock: clock rising
  Data Path: rotate_amount<14> to z_in_4
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             4   0.001   0.707  rotate_amount_14_IBUF (rotate_amount_14_IBUF)
     LUT6:I0->O            1   0.097   0.683  rotate_amount[14]_GND_1_o_LessThan_12_o21 (rotate_amount[14]_GND_1_o_LessThan_12_o2)
     LUT5:I0->O           47   0.097   0.792  rotate_amount[14]_GND_1_o_LessThan_12_o23 (rotate_amount[14]_GND_1_o_LessThan_12_o)
     LUT5:I0->O            1   0.097   0.295  Mmux_PWR_1_o_rotate_amount[15]_mux_25_OUT111 (Mmux_PWR_1_o_rotate_amount[15]_mux_25_OUT11)
     LUT3:I2->O            1   0.097   0.000  Mmux_PWR_1_o_rotate_amount[15]_mux_25_OUT112 (PWR_1_o_rotate_amount[15]_mux_25_OUT<4>)
     FDC:D                     0.008          z_in_4
    ----------------------------------------
    Total                     2.875ns (0.397ns logic, 2.478ns route)
                                      (13.8% logic, 86.2% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clock'
  Total number of paths / destination ports: 32 / 32
--------------------------------------------------------------------------
Offset:              0.640ns (Levels of Logic = 1)
  Source:            x_or_phase_out_15 (FF)
  Destination:       x_or_phase_out<15> (PAD)
  Source Clock:      clock rising
  Data Path: x_or_phase_out_15 to x_or_phase_out<15>
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q              1   0.361   0.279  x_or_phase_out_15 (x_or_phase_out_15)
     OBUF:I->O                 0.000          x_or_phase_out_15_OBUF (x_or_phase_out<15>)
    ----------------------------------------
    Total                     0.640ns (0.361ns logic, 0.279ns route)
                                      (56.4% logic, 43.6% route)

==========================================================================
Cross Clock Domains Report:
--------------------------
Clock to Setup on destination clock clock
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clock          |   29.558|         |         |         |
```

```
--------------+---------+---------+---------+----------+
=========================================================================
Total REAL time to Xst completion: 25.00 secs
Total CPU time to Xst completion: 25.19 secs

-->
Total memory usage is 4647840 kilobytes
Number of errors   :    0 (   0 filtered)
Number of warnings :   93 (   0 filtered)
Number of infos    :    4 (   0 filtered)
```