Map Report

Sun Aug 2 12:22:26 2020

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Release 14.7 Map P.20131013 (nt64)
Xilinx Mapping Report File for Design 'cordic'
Design Information
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Command Line   : map -intstyle ise -p xc7a100t-csg324-3 -w -logic_opt off -ol
high -t 1 -xt 0 -register_duplication off -r 4 -mt off -ir off -pr off -lc off
-power off -o cordic_map.ncd cordic.ngd cordic.pcf
Target Device  : xc7a100t
Target Package : csg324
Target Speed   : -3
Mapper Version : artix7 -- $Revision: 1.55 $
Mapped Date    : Sun Aug 02 12:19:11 2020
Design Summary
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Number of errors:      0
Number of warnings:   85
Slice Logic Utilization:
  Number of Slice Registers:                   472 out of 126,800    1%
    Number used as Flip Flops:                 472
    Number used as Latches:                      0
    Number used as Latch-thrus:                  0
    Number used as AND/OR logics:                0
  Number of Slice LUTs:                      3,611 out of  63,400    5%
    Number used as logic:                    3,429 out of  63,400    5%
      Number using O6 output only:           2,274
      Number using O5 output only:              97
      Number using O5 and O6:                1,058
      Number used as ROM:                        0
    Number used as Memory:                       0 out of  19,000    0%
    Number used exclusively as route-thrus:    182
      Number with same-slice register load:      0
      Number with same-slice carry load:       182
      Number with other load:                    0
Slice Logic Distribution:
  Number of occupied Slices:                   986 out of  15,850    6%
  Number of LUT Flip Flop pairs used:        3,618
    Number with an unused Flip Flop:         3,177 out of   3,618   87%
    Number with an unused LUT:                   7 out of   3,618    1%
    Number of fully used LUT-FF pairs:         434 out of   3,618   11%
    Number of unique control sets:               2
    Number of slice register sites lost
      to control set restrictions:               8 out of 126,800    1%
  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.
  OVERMAPPING of BRAM resources should be ignored if the design is
  over-mapped for a non-BRAM resource or if placement fails.
IO Utilization:
  Number of bonded IOBs:                        83 out of     210   39%
Specific Feature Utilization:
  Number of RAMB36E1/FIFO36E1s:                  0 out of     135    0%
  Number of RAMB18E1/FIFO18E1s:                  0 out of     270    0%
  Number of BUFG/BUFGCTRLs:                      1 out of      32    3%
    Number used as BUFGs:                        1
    Number used as BUFGCTRLs:                    0
  Number of IDELAYE2/IDELAYE2_FINEDELAYs:        0 out of     300    0%
  Number of ILOGICE2/ILOGICE3/ISERDESE2s:        0 out of     300    0%
  Number of ODELAYE2/ODELAYE2_FINEDELAYs:        0
  Number of OLOGICE2/OLOGICE3/OSERDESE2s:        0 out of     300    0%
  Number of PHASER_IN/PHASER_IN_PHYs:            0 out of      24    0%
  Number of PHASER_OUT/PHASER_OUT_PHYs:          0 out of      24    0%
  Number of BSCANs:                              0 out of       4    0%
  Number of BUFHCEs:                             0 out of      96    0%
  Number of BUFRs:                               0 out of      24    0%
  Number of CAPTUREs:                            0 out of       1    0%
  Number of DNA_PORTs:                           0 out of       1    0%
  Number of DSP48E1s:                            0 out of     240    0%
  Number of EFUSE_USRs:                          0 out of       1    0%
  Number of FRAME_ECCs:                          0 out of       1    0%
  Number of IBUFDS_GTE2s:                        0 out of       4    0%
  Number of ICAPs:                               0 out of       2    0%
  Number of IDELAYCTRLs:                         0 out of       6    0%
  Number of IN_FIFOs:                            0 out of      24    0%
  Number of MMCME2_ADVs:                         0 out of       6    0%
  Number of OUT_FIFOs:                           0 out of      24    0%
  Number of PCIE_2_1s:                           0 out of       1    0%
  Number of PHASER_REFs:                         0 out of       6    0%
  Number of PHY_CONTROLs:                        0 out of       6    0%
  Number of PLLE2_ADVs:                          0 out of       6    0%
  Number of STARTUPs:                            0 out of       1    0%
  Number of XADCs:                               0 out of       1    0%
Average Fanout of Non-Clock Nets:                3.68
Peak Memory Usage:  5082 MB
Total REAL time to MAP completion:  1 mins 32 secs
Total CPU time to MAP completion:   1 mins 31 secs
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Section 1 - Errors
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Section 2 - Warnings
--------------------
WARNING:LIT:701 - PAD symbol "clock" has an undefined IOSTANDARD.
WARNING:LIT:702 - PAD symbol "clock" is not constrained (LOC) to a specific
   location.
WARNING:PhysDesignRules:2452 - The IOB reset is either not constrained (LOC) to
   a specific location and/or has an undefined I/O Standard (IOSTANDARD). This
   condition may seriously affect the device and will be an error in bitstream
   creation. It should be corrected by properly specifying the pin location and
   I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB op_mode is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB rotate_amount<7> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB rotate_amount<8> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB rotate_amount<5> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB rotate_amount<6> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB rotate_amount<9> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB rotate_amount<0> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB rotate_amount<3> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB rotate_amount<4> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB rotate_amount<1> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB rotate_amount<2> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB y_or_size_out<9> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
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WARNING:PhysDesignRules:2452 - The IOB y_or_size_out<5> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
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   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB y_or_size_out<2> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
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   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB y_or_size_out<1> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB y_or_size_out<4> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
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   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
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   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB y_or_size_out<0> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB y_coordinate<8> is either not constrained
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WARNING:PhysDesignRules:2452 - The IOB y_coordinate<5> is either not constrained
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   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_or_phase_out<11> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_or_phase_out<12> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_or_phase_out<13> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_or_phase_out<14> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB y_coordinate<9> is either not constrained
   (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB y_coordinate<0> is either not constrained
   (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_or_phase_out<10> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
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   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB y_coordinate<2> is either not constrained
   (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB y_coordinate<1> is either not constrained
   (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_or_phase_out<15> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
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   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_coordinate<8> is either not constrained
   (LOC) to a specific location and/or has an undefined I/O Standard
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WARNING:PhysDesignRules:2452 - The IOB x_coordinate<7> is either not constrained
   (LOC) to a specific location and/or has an undefined I/O Standard
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   error in bitstream creation. It should be corrected by properly specifying
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WARNING:PhysDesignRules:2452 - The IOB x_coordinate<6> is either not constrained
   (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
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WARNING:PhysDesignRules:2452 - The IOB x_coordinate<5> is either not constrained
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WARNING:PhysDesignRules:2452 - The IOB x_coordinate<0> is either not constrained
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WARNING:PhysDesignRules:2452 - The IOB x_coordinate<4> is either not constrained
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WARNING:PhysDesignRules:2452 - The IOB x_coordinate<3> is either not constrained
   (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_coordinate<2> is either not constrained
   (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_coordinate<1> is either not constrained
   (LOC) to a specific location and/or has an undefined I/O Standard
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   error in bitstream creation. It should be corrected by properly specifying
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WARNING:PhysDesignRules:2452 - The IOB y_coordinate<15> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
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   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB y_coordinate<13> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
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WARNING:PhysDesignRules:2452 - The IOB y_coordinate<14> is either not
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   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB y_coordinate<11> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB y_coordinate<12> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB y_coordinate<10> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB rotate_amount<15> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
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   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB rotate_amount<11> is either not
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   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB clock is either not constrained (LOC) to
   a specific location and/or has an undefined I/O Standard (IOSTANDARD). This
   condition may seriously affect the device and will be an error in bitstream
   creation. It should be corrected by properly specifying the pin location and
   I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB y_or_size_out<15> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
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   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB y_or_size_out<13> is either not
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WARNING:PhysDesignRules:2452 - The IOB y_or_size_out<11> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
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   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_coordinate<11> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_coordinate<12> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_coordinate<10> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_or_phase_out<0> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_or_phase_out<4> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_or_phase_out<3> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_or_phase_out<2> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_or_phase_out<1> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
```

```
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_or_phase_out<8> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_or_phase_out<7> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_or_phase_out<6> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_or_phase_out<5> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB x_or_phase_out<9> is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
Section 3 - Informational
-------------------------
INFO:LIT:244 - All of the single ended outputs in this design are using slew
   rate limited output drivers. The delay on speed critical single ended outputs
   can be dramatically reduced by designating them as fast outputs.
INFO:Pack:1716 - Initializing temperature to 85.000 Celsius. (default - Range:
   0.000 to 85.000 Celsius)
INFO:Pack:1720 - Initializing voltage to 0.950 Volts. (default - Range: 0.950 to
   1.050 Volts)
INFO:Map:215 - The Interim Design Summary has been generated in the MAP Report
   (.mrp).
INFO:Pack:1650 - Map created a placed design.
Section 4 - Removed Logic Summary
---------------------------------
   2 block(s) optimized away
Section 5 - Removed Logic
-------------------------
Optimized Block(s):
TYPE            BLOCK
GND             XST_GND
VCC             XST_VCC
To enable printing of redundant blocks removed and signals merged, set the
detailed map report option and rerun map.
Section 6 - IOB Properties
--------------------------
```

IOB Name	Type	Direction	IO Standard	Diff Term	Drive Strength	Slew Rate	Reg (s)	Resist
clock	IOB	INPUT	LVCMOS18					
op_mode	IOB	INPUT	LVCMOS18					
reset	IOB	INPUT	LVCMOS18					
rotate_amount<0>	IOB	INPUT	LVCMOS18					
rotate_amount<1>	IOB	INPUT	LVCMOS18					
rotate_amount<2>	IOB	INPUT	LVCMOS18					
rotate_amount<3>	IOB	INPUT	LVCMOS18					
rotate_amount<4>	IOB	INPUT	LVCMOS18					
rotate_amount<5>	IOB	INPUT	LVCMOS18					
rotate_amount<6>	IOB	INPUT	LVCMOS18					
rotate_amount<7>	IOB	INPUT	LVCMOS18					
rotate_amount<8>	IOB	INPUT	LVCMOS18					
rotate_amount<9>	IOB	INPUT	LVCMOS18					
rotate_amount<10>	IOB	INPUT	LVCMOS18					
rotate_amount<11>	IOB	INPUT	LVCMOS18					
rotate_amount<12>	IOB	INPUT	LVCMOS18					
rotate_amount<13>	IOB	INPUT	LVCMOS18					
rotate_amount<14>	IOB	INPUT	LVCMOS18					
rotate_amount<15>	IOB	INPUT	LVCMOS18					
x_coordinate<0>	IOB	INPUT	LVCMOS18					
x_coordinate<1>	IOB	INPUT	LVCMOS18					
x_coordinate<2>	IOB	INPUT	LVCMOS18					
x_coordinate<3>	IOB	INPUT	LVCMOS18					
x_coordinate<4>	IOB	INPUT	LVCMOS18					
x_coordinate<5>	IOB	INPUT	LVCMOS18					
x_coordinate<6>	IOB	INPUT	LVCMOS18					
x_coordinate<7>	IOB	INPUT	LVCMOS18					
x_coordinate<8>	IOB	INPUT	LVCMOS18					
x_coordinate<9>	IOB	INPUT	LVCMOS18					
x_coordinate<10>	IOB	INPUT	LVCMOS18					
x_coordinate<11>	IOB	INPUT	LVCMOS18					
x_coordinate<12>	IOB	INPUT	LVCMOS18					
x_coordinate<13>	IOB	INPUT	LVCMOS18					
x_coordinate<14>	IOB	INPUT	LVCMOS18					
x_coordinate<15>	IOB	INPUT	LVCMOS18					
x_or_phase_out<0>	IOB	OUTPUT	LVCMOS18		12	SLOW		
x_or_phase_out<1>	IOB	OUTPUT	LVCMOS18		12	SLOW		
x_or_phase_out<2>	IOB	OUTPUT	LVCMOS18		12	SLOW		
x_or_phase_out<3>	IOB	OUTPUT	LVCMOS18		12	SLOW		
x_or_phase_out<4>	IOB	OUTPUT	LVCMOS18		12	SLOW		
x_or_phase_out<5>	IOB	OUTPUT	LVCMOS18		12	SLOW		
x_or_phase_out<6>	IOB	OUTPUT	LVCMOS18		12	SLOW		
x_or_phase_out<7>	IOB	OUTPUT	LVCMOS18		12	SLOW		

x_or_phase_out<8>	IOB	OUTPUT	LVCMOS18		12	SLOW	
x_or_phase_out<9>	IOB	OUTPUT	LVCMOS18		12	SLOW	
x_or_phase_out<10>	IOB	OUTPUT	LVCMOS18		12	SLOW	
x_or_phase_out<11>	IOB	OUTPUT	LVCMOS18		12	SLOW	
x_or_phase_out<12>	IOB	OUTPUT	LVCMOS18		12	SLOW	
x_or_phase_out<13>	IOB	OUTPUT	LVCMOS18		12	SLOW	
x_or_phase_out<14>	IOB	OUTPUT	LVCMOS18		12	SLOW	
x_or_phase_out<15>	IOB	OUTPUT	LVCMOS18		12	SLOW	
y_coordinate<0>	IOB	INPUT	LVCMOS18				
y_coordinate<1>	IOB	INPUT	LVCMOS18				
y_coordinate<2>	IOB	INPUT	LVCMOS18				
y_coordinate<3>	IOB	INPUT	LVCMOS18				
y_coordinate<4>	IOB	INPUT	LVCMOS18				
y_coordinate<5>	IOB	INPUT	LVCMOS18				
y_coordinate<6>	IOB	INPUT	LVCMOS18				
y_coordinate<7>	IOB	INPUT	LVCMOS18				
y_coordinate<8>	IOB	INPUT	LVCMOS18				
y_coordinate<9>	IOB	INPUT	LVCMOS18				
y_coordinate<10>	IOB	INPUT	LVCMOS18				
y_coordinate<11>	IOB	INPUT	LVCMOS18				
y_coordinate<12>	IOB	INPUT	LVCMOS18				
y_coordinate<13>	IOB	INPUT	LVCMOS18				
y_coordinate<14>	IOB	INPUT	LVCMOS18				
y_coordinate<15>	IOB	INPUT	LVCMOS18				
y_or_size_out<0>	IOB	OUTPUT	LVCMOS18		12	SLOW	
y_or_size_out<1>	IOB	OUTPUT	LVCMOS18		12	SLOW	
y_or_size_out<2>	IOB	OUTPUT	LVCMOS18		12	SLOW	
y_or_size_out<3>	IOB	OUTPUT	LVCMOS18		12	SLOW	
y_or_size_out<4>	IOB	OUTPUT	LVCMOS18		12	SLOW	
y_or_size_out<5>	IOB	OUTPUT	LVCMOS18		12	SLOW	
y_or_size_out<6>	IOB	OUTPUT	LVCMOS18		12	SLOW	
y_or_size_out<7>	IOB	OUTPUT	LVCMOS18		12	SLOW	
y_or_size_out<8>	IOB	OUTPUT	LVCMOS18		12	SLOW	
y_or_size_out<9>	IOB	OUTPUT	LVCMOS18		12	SLOW	
y_or_size_out<10>	IOB	OUTPUT	LVCMOS18		12	SLOW	
y_or_size_out<11>	IOB	OUTPUT	LVCMOS18		12	SLOW	
y_or_size_out<12>	IOB	OUTPUT	LVCMOS18		12	SLOW	
y_or_size_out<13>	IOB	OUTPUT	LVCMOS18		12	SLOW	
y_or_size_out<14>	IOB	OUTPUT	LVCMOS18		12	SLOW	
y_or_size_out<15>	IOB	OUTPUT	LVCMOS18		12	SLOW	

Section 7 - RPMs

Section 8 - Guide Report

Guide not run on this design.
Section 9 - Area Group and Partition Summary

Partition Implementation Status

  No Partitions were found in this design.

Area Group Information

  No area groups were found in this design.

Section 10 - Timing Report

A logic-level (pre-route) timing report can be generated by using Xilinx static timing analysis tools, Timing Analyzer (GUI) or TRCE (command line), with the mapped NCD and PCF files. Please note that this timing report will be generated using estimated delay information. For accurate numbers, please generate a timing report with the post Place and Route NCD file.
For more information about the Timing Analyzer, consult the Xilinx Timing Analyzer Reference Manual; for more information about TRCE, consult the Xilinx Command Line Tools User Guide "TRACE" chapter.
Section 11 - Configuration String Details

Use the "-detail" map option to print out Configuration Strings
Section 12 - Control Set Information

Use the "-detail" map option to print out Control Set Information.
Section 13 - Utilization by Hierarchy

Use the "-detail" map option to print out the Utilization by Hierarchy section.