Week 3 : Assignment 3

The due date for submitting this assignment has passed.

Due on 2021-08-25, 23:59 IST.

Assignment submitted on 2021-08-14, 20:22 IST

1) Which of the following statement(s) is/are true about the Verilog description styles? *1 point*

a. Dataflow modeling style is mainly used to describe combinational circuits.
b. Dataflow modeling style is mainly used to describe sequential circuits.
c. Behavioral modeling style is mainly used to describe sequential circuits.
d. Behavioral modeling style is mainly used to describe combinational circuits
e. None of the above.

HINT: (If options a, b, c and d are all false, select option e as the answer.)

- [x] a.
- [ ] b.
- [x] c.
- [ ] d.
- [ ] e.

Yes, the answer is correct.
Score: 1
Accepted Answers:
a.
c.

2) Consider the continuous assignment expression of the form *0 points*

assign target = expression

Which of the following(s) is/are valid target of such assignment expression?

a. A scalar net type variable.
b. A scalar net type or register type variable.
c. A vector of register type variable.
d. A constant part-select of a vector net type variable.
e. All of the above.

HINT: (If options a, b, c and d are all valid, select option e as the answer.)

- [x] a.
- [ ] b.
- [ ] c.
- [x] d.
- [ ] e.

Yes, the answer is correct.
Score: 0
Accepted Answers:
a.
d.

3) Which of the following(s) is/are valid procedural statements? *1 point*

a. Blocking assignment statement.
b. Non-blocking assignment statement.
c. Continuous assignment statement.
d. Conditional statement.
e. All of the above.

HINT: (If options a, b, c and d are all valid, select option e as the answer.)

- [x] a.
- [x] b.
- [ ] c.
- [x] d.
- [ ] e.

Yes, the answer is correct.
Score: 1
Accepted Answers:
a.
b.
d.

4) Consider the Verilog code segment: *1 point*

```
reg w, x, y;
reg [1:0] z;
wire [3:0] f;
assign f[2] = w ? x: z[y];
```

Which of the followings hardware components will be generated by a synthesis tool?

a. A decoder and a 2-to-1 multiplexer.
b. A decoder and two 2-to-1 multiplexers.
c. Only two 2-to-1 multiplexers.
d. None of the above.

HINT: (If options a, b and c are all incorrect, select option d as the answer.)

- ( ) a.
- ( ) b.
- (•) c.
- ( ) d.

Yes, the answer is correct.
Score: 1
Accepted Answers:
c.

5) Which of the following statement(s) is/are true about procedural blocks? *1 point*

a. The initial block is non-synthesizable and is normally used in testbenches.
b. Both initial and always block are synthesizable.
c. The always block is synthesizable and may result a combinational circuit.
d. None of the above.

HINT: (If options a, b and c are all false, select option d as the answer.)

- [x] a.
- [ ] b.
- [x] c.
- [ ] d.

Yes, the answer is correct.
Score: 1
Accepted Answers:
a.
c.

6) In which of the following case(s) a synthesis tool infers a sequential circuit from the description of an always block? *1 point*

a. Every branch of a conditional statement must define all outputs.
b. Every branch of a case statement must define all outputs.
c. Some branches of case statement have defined outputs.
d. Some branches of conditional statements have defined outputs.
e. None of the above.

HINT: (If options a, b, c and d are all incorrect, select option e as the answer.)

- [ ] a.
- [x] b.
- [ ] c.
- [ ] d.
- [ ] e.

No, the answer is incorrect.
Score: 0
Accepted Answers:
c.
d.

7) Which of the following(s) is/are true about event expressions of always blocks? *1 point*

a. A +ve edge sensitive always block executes at signal transition from 0 to z.
b. A +ve edge sensitive always block executes at signal transition from 1 to z.
c. A –ve edge sensitive always block executes at signal transition from z to 0.
d. A –ve edge sensitive always block executes at signal transition from z to 1.
e. All of the above.

HINT: (If options a, b, c and d are all true, select option e as the answer.)

- [x] a.
- [ ] b.
- [x] c.
- [ ] d.
- [ ] e.

Yes, the answer is correct.
Score: 1
Accepted Answers:
a.
c.

8) Which of the following statement(s) is/are true about the following Verilog module? *1 point*

```
module fun (f, a, b, clk);
  input a, b, clk;
  output f;
  reg f, t1, t2;
  always @(posedge clk or b)
    begin
      t1 = a & clk;
      t2 = f & b;
      f = t1 | t2;
    end
endmodule
```

a. The module realizes a synchronous storage cell for storing only logic 1.
b. The module realizes a positive edge triggered D flip-flop.
c. The input port b acts as an asynchronous active low reset signal when input a is also kept low.
d. None of the above.

HINT: (If options a, b and c are all false, select option d as the answer.)

- [x] a.
- [x] b.
- [x] c.
- [ ] d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
a.
c.

9) Given the following Verilog code:

```
integer x, y;
reg clk;
```

```
always #5 clk = ~clk;
initial
  begin
    #5 clk = 1'b0; x = 0;
    #70 $finish;
  end
initial
  begin
    #5 y = 17;
    forever
      #8  x = x + y;
  end
```

The final value of x will be _____.

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Hint

Yes, the answer is correct.
Score: 1

Accepted Answers:
(Type: Numeric) 136

1 point

10) Which of the following statement(s) is/are true about the following Verilog module? *1 point*

```
module fun (f, a, b, c, d);
  input a, b, c, d;
  output reg f;
  always @(*)
    begin
      f = 1'b0;
      casex ({a, b, c, d})
        4'b11xx, 4'bx10x, 4'b1x00: f = 1'b1;
      endcase
    end
endmodule
```

a. The module realizes a sequential circuit and variable f infers a D-latch during synthesis.
b. The module realizes a pure combinational circuit.
c. For the input $\{a, b, c, d\} = 4'b1000$, the function will provide an output logic 1 during simulation.
d. None of the above.

HINT: (If options a, b and c are all false, select option d as the answer.)

- [ ] a.
- [ ] b.
- [x] c.
- [ ] d.

Partially Correct.
Score: 0.5

Accepted Answers:
b.
c.

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