Week 1 : Assignment 1

The due date for submitting this assignment has passed.

Due on 2021-08-18, 23:59 IST.

Assignment submitted on 2021-08-18, 16:31 IST

1) Which of the following statements is (are) true with respect to Moore's law? *1 point*

a. Area of a chip will grow exponentially with time.
b. Number of transistors in a chip will grow exponentially with time.
c. Energy dissipation in a chip will grow exponentially with time.
d. All of these.

a.
b.
c.
d.

Yes, the answer is correct.
Score: 1
Accepted Answers:
b.

2) For realizing the following function using 4-input LUTs, how many LUTs will be required? *1 point*

F = A.B'.C + B'.D+ E'.F' + F.G,H' + I'.J'

a. 2
b. 3
c. 4
d. 5

a.
b.
c.
d.

Yes, the answer is correct.
Score: 1
Accepted Answers:
b.

3) Which of the following represents behavioral specification of a function? *1 point*

a. A netlist consisting of AND, OR and NOT gates.
b. The Verilog specification: assign F = (A & B) | (C & D);
c. The truth table description of the function.
d. A realization using a network of 2-to-1 multiplexers.

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
b.
c.

4) Which of the following represents structural representation of a function? *1 point*

a. A netlist of basic gates (AND, OR, NOT).
b. A netlist of multiplexers.
c. F = A'.B + B.C.D'
d. A Verilog specification using "assign" statement.

a.
b.
c.
d.

Partially Correct.
Score: 0.5
Accepted Answers:
a.
b.

5) Which of the following ordering is correct with respect to circuit speed (slowest to fastest)? *1 point*

a. Gate Array, FPGA, Standard Cell, Full Custom
b. FPGA, Standard Cell, Gate Array, Full Custom
c. Standard Cell, FPGA, Gate Array, Full CUstom
d. FPGA, Gate Array, Standard Cell, Full Custom

a.
b.
c.
d.

Yes, the answer is correct.
Score: 1
Accepted Answers:
d.

6) Which of the following provides fastest design turnaround time? *1 point*

a. Gate Array

b. FPGA
c. Standard Cell
d. Full Custom

- ○ a.
- ◉ b.
- ○ c.
- ○ d.

Yes, the answer is correct.
Score: 1
Accepted Answers:
b.

7) Which of the following statement(s) is/are true for FPGA design style? *1 point*

a. A LUT containing a 16x1 RAM and can be used to realize a 4-variable function.
b. A LUT containing a 16x1 RAM and can be used to realize a 5-variable function.
c. A 5-variable AND function, f = ABCDE can be realized using only 2 LUTs.
d. None of these.

- ☑ a.
- ☐ b.
- ☑ c.
- ☐ d.

Yes, the answer is correct.
Score: 1
Accepted Answers:
a.
c.

8) Which of the following statements is/are true? *1 point*

a. FPGA design style requires separate floorplanning and placement stages.
b. Standard Cell design style requires separate floorplanning and placement stages.
c. Full Custom design style requires separate floorplanning and placement stages.
d. For Standard Cell design style, floorplanning and placement can be done together.

- ☐ a.
- ☑ b.
- ☑ c.
- ☐ d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
c.
d.

9) Why do we use test benches in Verilog? *1 point*

a. To verify the functionality of a Verilog module by applying test inputs.
b. To check for syntax errors in a Verilog module.
c. To verify whether a given Verilog module is synthesizable.
d. All of these.

- ◉ a.
- ○ b.
- ○ c.
- ○ d.

Yes, the answer is correct.
Score: 1
Accepted Answers:
a.

10) What function do the following Verilog module implement? *1 point*

```
module mycircuit (f, a, b, c);
  input a,b,c;  output f,
  wire w1, w2;
  nand Gate1 (w1,a,b);
  or   Gate2 (w2,b,c);
  nor  Gate3 (f,w1,w2);
endmodule
```

a. f = a'.c
b. f = a.b.c'
c. f = (a + c)'
d. f = b.c'
e. None of these

- ○ a.
- ○ b.
- ○ c.
- ○ d.
- ◉ e.

Yes, the answer is correct.
Score: 1
Accepted Answers:
e.

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