Week 2 : Assignment 2

The due date for submitting this assignment has passed.

Due on 2021-08-18, 23:59 IST.

Assignment submitted on 2021-08-02, 21:58 IST

1) Which of the following statement(s) is/are true about the following Verilog module? *1 point*

```
module fun (f, x, y);
        input x, y;
        output f;
        assign f = x | y;
endmodule
```

a. Represents a behavioral description of a logical OR operation.
b. Represents a structural description of a logical OR operation.
c. Represents a hierarchical description of a logical OR operation.
d. Synthesis of the module always realizes f using a single OR gate.

- [ ] a.
- [x] b.
- [ ] c.
- [x] d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
a.

2) Which of the following statement(s) is/are true regarding synthesis of Verilog modules? *1 point*

a. A reg type variable is always used to define sequential circuits.
b. Net type variables are specifically used to define combinational circuits.
c. Synthesis of reg type variables may lead to storage cells.
d. All of these.

HINT: (If options a, b and c are all true, select option d as the answer.)

- [ ] a.
- [ ] b.
- [ ] c.
- [x] d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
c.

3) Given the following Verilog code:

```
module fun (f, a, b, c, d);
     input a, b, c, d;
     output f;
     wire t1, t2;
     and g1 (t1, a, c);
     xor g2 (t2, b, d);
     or  g3 (f, t1, t2);
endmodule
```

Initializing all input variables `a`, `b`, `c` and `d` with logic values `0`, `1`, `x` and `z`, the logic state of output variable `f` will be _____ after simulation.

x

Hint

Yes, the answer is correct.
Score: 1

Accepted Answers:
(Type: String) x

1 point

4) Which of the following statements is/are false? *1 point*

a. The "assign" statement always generates a combinational circuit.
b. The "always" block can generate combinational or sequential circuit.
c. The "always" block always generates a sequential circuit.
d. The "assign" statement can generate combinational or sequential circuit.

- [ ] a.
- [ ] b.
- [x] c.
- [x] d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
a.
c.

5) Which of the following statement(s) is/are true about primitive gates? *1 point*

a. Specified delay during instantiation of primitive gates can be used for simulation and it is also converted to hardware logic.
b. All the primitive gates can be instantiated with any number of input and output ports except for NOT and BUF.
c. An output port of a primitive gate must be connected to a net and output signal can be declared as wire or register.

d. Both register and wire type variables can be used to connect to the Input ports of a primitive gate during instantiating.

HINT: (N/A.)

- [ ] a.
- [x] b.
- [x] c.
- [x] d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
c.
d.

6) Given the following code segment:

```
`timescale 10ns/100ps
module fun (f, a, b);
     input a, b;
     output f;
     and #2.429 g1 (f, a, b);
endmodule
```

The AND gate delay of #2.429 will be interpreted as _____ ps.

24300.0

Hint

Yes, the answer is correct.
Score: 1

Accepted Answers:
(Type: Numeric) 24300

1 point

7) Consider the following Verilog module:

```
module fun (f, a, b, c);
     input a, b, c;
     output f;
     wand f;
     assign f = a ^ b;
     assign f = b | c;
endmodule
```

Initializing a, b and c with logic values 0, 0 and 1 respectively, the logic value at output port f will be _____.

0

Hint

Yes, the answer is correct.
Score: 1

Accepted Answers:
(Type: Numeric) 0

1 point

8) During instantiating a module inside another module, _____ association allows listing of instantiated module parameters in arbitrary order to minimize connectivity error.

port

Hint

No, the answer is incorrect.
Score: 0

Accepted Answers:
(Type: String) Explicit

1 point

1 point

9) Given the following Verilog code:

```
module fun (f, a, b, c, d);
     input a, b, c, d;
     output f;
     reg f, e;
     always @ ( a or b or c or d)
     begin
          if (!a && !b)
               e = c;
          f = e | ~f;
     end
endmodule
```

What a synthesis tool will generate for variable e and f?

a. Variable e and f both will be realized as storage cells.
b. Variable e will be synthesized as wire and f will be realized as storage cell.
c. Variable e will be synthesized as storage cell and f will be realized as wire.
d. Variable e and f both will be realized as wire.

HINT: (N/A.)

- [ ] a.
- [x] b.
- [ ] c.
- [ ] d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
a.

10) Given the following Verilog code:

```
module fun (f, a, b, c, d);
     input a, b, c, d;
     output f;
     wire [0:7] a, b, c, d;
     reg [0:15] e, f;
     always @ ( a or b or c or d)
     begin
          e = {a & b, c ^ d};
          f ={{2{e[6:9]}}, b[0:3], c[4:7]};
     end
endmodule
```

A test simulation of the module initializing input variables a, b, c and d with 8'h1a, 8'hb3, 8'h47 and 8'h6e in respective order, will provide _____ (in hexadecimal) as output f. Symbol x can be used to specify an unknown hexadecimal digit.

16'h88b7

Hint

Yes, the answer is correct.
Score: 0

Accepted Answers:
(Type: String) 16'h88b7

0 points

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