Course outline

How does an NPTEL online course work?

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Week 7

- Lecture 30 : MODELING MEMORY
- Lecture 31 : MODELING REGISTER BANKS
- Lecture 32 : BASIC PIPELINING CONCEPTS
- Lecture 33 : PIPELINE MODELING (PART 1)
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- Lecture 35 : SWITCH LEVEL MODELING (PART 1)
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Assignments Solution

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Week 7 : Assignment 7

The due date for submitting this assignment has passed.

Due on 2021-09-15, 23:59 IST.

Assignment submitted on 2021-09-15, 22:34 IST

1) Which of the following statement(s) is/are true about memory modeling in Verilog? *1 point*

a. Memory can be defined as an array of type reg at behavioral level.
b. Memory can be modeled as a two dimensional array of type wire.
c. Both RAM and ROM can be modeled using vector of type reg.
d. Both RAM and ROM can be modeled using vector of type net.
e. All of these

HINT: (If options a, b, c and d are all correct, select option e as the answer.)

- [x] a.
- [ ] b.
- [x] c.
- [ ] d.

Yes, the answer is correct.
Score: 1
Accepted Answers:
a.
c.

2) Consider the following declaration of a 2D reg type vector in Verilog: *1 point*

```
reg [0:A] mem [0:B];
```

Which of the following statement(s) is/are true with respect to memory modeling?

a. It models a memory of size B x A bits.
b. It models a memory of size (B+1) x (A+1) bits.
c. It models a memory containing B words with word size A bits.
d. It models a memory containing (B + 1) words with word size (A + 1) bits.

- [ ] a.
- [x] b.
- [ ] c.
- [x] d.

Yes, the answer is correct.
Score: 1
Accepted Answers:
b.
d.

3) Consider the following memory write operation: *1 point*

```
memory[address] = data;
```

If memory capacity is 256 x 16, then size of address and data variable will be

a. address = 16 bit and data = 265 bit
b. address = 256 bit and data = 16 bit
c. address = 8 bit and data = 16 bit
d. None of these.

HINT: (If options a, b and c are all incorrect, select option d as the answer.)

- ○ a.
- ○ b.
- ◉ c.
- ○ d.

Yes, the answer is correct.
Score: 1
Accepted Answers:
c.

4) Which of the following statement(s) is/are true about the following Verilog module? *1 point*

```
module fun1 (rd_out, wr_in, adr, rw, clk);
      input clk, rw;
      input [2:0] adr;
      input [15:0] wr_in;
      output [15:0] rd_out;
      reg [15:0] regfile[0:7];
      assign rd_out = rw ? 16'bz : regfile[adr1];
      always @(posedge clk)
            if (rw) regfile[adr] <= wr_in;
endmodule
```

a. The module realizes a RAM with synchronous read/write operation.
b. The module realizes a RAM with asynchronous read and synchronous write.
c. The module realizes a RAM that allows simultaneous read/write operations.
d. None of these.

HINT: (If options a, b and c are all incorrect, select option d as the answer.)

- ○ a.
- ◉ b.
- ○ c.
- ○ d.

Yes, the answer is correct.

Score: 1
Accepted Answers:
b.

5) Which of the following is/are considered as standard approach for memory modeling? *1 point*

a. Variable of type inout are used to read and write data in memory.
b. Separate variable of type input and output are used to write data in memory and to read data from memory, respectively.
c. Variables of inout type or input and output type separately can be considered for modeling memory.
d. None of these.

HINT: (If options a, b and c are all incorrect, select option d as the answer.)

- a.
- (•) b.
- c.
- d.

Yes, the answer is correct.
Score: 1
Accepted Answers:
b.

6) Identify the correct statement(s) for declaring register bank using Verilog. *1 point*

a. The register bank can be declared as a reg type vector that can be accessed sequentially.
b. The register bank can be declared as independent wire type variables.
c. Two or more registers bank can be accessed concurrently for read and write operation in a clock cycle.
d. None of these.

HINT: (If options a, b and c are all incorrect, select option d as the answer.)

- a.
- b.
- (•) c.
- d.

Yes, the answer is correct.
Score: 1
Accepted Answers:
c.

7) Which of the following statement(s) is/are true about pipelined implementation? *1 point*

a. A pipelined implementation reduces the overall execution time of an individual instruction in a processor.
b. A pipelined implementation may increase the overall execution time of an individual instruction in a processor.
c. A pipelined implementation reduces the throughput of the processor.
d. A pipelined implementation increases the throughput of the processor.
e. None of these.

HINT: (If options a, b, c and d are all incorrect, select option d as the answer.)

- [x] a.
- [ ] b.
- [ ] c.
- [x] d.
- [ ] e.

No, the answer is incorrect.
Score: 0
Accepted Answers:
b.
d.

8) Assume that a computational task requires 63 ns in a non-pipelined processor for execution. 500 such tasks are assigned to a 9-stage pipelined processor with uniform stage delay. Ignoring the inter-stage memory delay, the time taken by the pipelined processor is _____ µs (in decimal).

3.556

Hint

Yes, the answer is correct.
Score: 1
Accepted Answers:
(Type: Range) 3.50,4.00

1 point

9) A pipelined processing unit has stage delays 11µs, 8µs, 13µs, 9µs, and 6µs. The latch delay in each stage of computation is 7µs. The maximum throughput observed from the processing unit is _____ (in decimal) tasks per second.

55555.56

Hint

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 50000

1 point

10) A pipelined processing unit has stage delays 6 µs, 4 µs, 5 µs, and 7 µs. The clock skew, jitter and setup times are 0.5 µs, 0.25 µs and 0.75 µs, respectively. The minimum clock period required for successful pipeline implementation is _____ µs.

7.5

Hint

No, the answer is incorrect.
Score: 0
Accepted Answers:

(Type: Numeric) 8.5

1 point

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