

Course outline

How does an NPTEL online course work?

Week 0

Week 1

Week 2

Week 3

Week 4

Week 5

Week 6

Week 7

Week 8

Lecture 37 : PIPELINE IMPLEMENTATION OF A PROCESSOR (PART 1)

Lecture 38 : PIPELINE IMPLEMENTATION OF A PROCESSOR (PART 2)

Lecture 39 : PIPELINE IMPLEMENTATION OF A PROCESSOR (PART 3)

Lecture 40 : VERILOG MODELING OF THE PROCESSOR (PART 1)

Lecture 41 : VERILOG MODELING OF THE PROCESSOR (PART 2)

Week 8 Lecture Material

Quiz: Week 8 : Assignment 8

Feedback Form of Week 8

Assignments Solution

Download Videos

Text Transcripts

Live Interactive session

Books

Week 8 : Assignment 8

The due date for submitting this assignment has passed.

Due on 2021-09-22, 23:59 IST.

Assignment submitted on 2021-09-22, 23:26 IST

1) Identify the correct statements about MIPS32 processor?

1 point

- a. MIPS32 is a complex instruction set architecture processor.
- b. MIPS32 processor contains 16 number of 32-bit general purpose registers.
- c. MIPS32 processor contains 32 number of 32-bit general purpose registers.
- d. MIPS32 processor allows arithmetic instructions with operands in register or memory.

- ☐ a.
- ☐ b.
- ☒ c.
- ☐ d.

Yes, the answer is correct.

Score: 1

Accepted Answers:

c.

2) MIPS32 instructions are classified into:

1 point

- a. Register-type, Immediate-type and J-type based on their behavior.
- b. Register-type, Immediate-type and J-type based on their encoding.

- ☐ a.
- ☒ b.

Yes, the answer is correct.

Score: 1

Accepted Answers:

b.

3) Identify all the valid R-type instructions.

1 point

- a. BEQZ R1, LOOP
- b. ADDI R4, R3, 12
- c. SUB R6, R2, R7
- d. None of the above.

- ☐ a.
- ☐ b.
- ☒ c.
- ☐ d.

Yes, the answer is correct.

Score: 1

Accepted Answers:

c.

4) Given the following MIPS32 code segment:

1 point

```
ADDI R1, R0, 40
SUBI R2, R1, 32
LW R5, 230(R0)
ADD R3, R5, R2
MUL R4, R1, R3
```

Suppose that memory locations 230, 231, 232 and 233 (in decimal) contains the data 12, 36, 110 and 26 (in decimal) respectively. The value at R4 after executing the above code segment will be _____.

- a. 195
- b. 530
- c. 486
- d. 800

- ☐ a.
- ☐ b.
- ☐ c.
- ☒ d.

Yes, the answer is correct.

Score: 1

Accepted Answers:

d.

5) Given the following MIPS32 code segment:

```
ADDI R1, R0, 230
LW R2, 0(R1)
LW R3, 2(R1)
ADD R4, R3, R2
SW R4, 4(R1)
```

Suppose that memory locations 230, 231, 232 and 233 (in decimal) contains the data 12, 36, 110 and 26 (in decimal) respectively. After executing the above code the value at memory location 234 will be _____ (in decimal).

122

Hint

Yes, the answer is correct.

Score: 1

Accepted Answers:

Accepted Answers:
(Type: Numeric) 122

1 point

- 6) Consider the execution of following MIPS32 instruction:

SLT R2, R3, R4

If registers R3 and R4 are initialized with values 34 and 42, the value of register R2 after the end of execution will be _____.

1

Hint

Yes, the answer is correct.
Score: 1

Accepted Answers:
(Type: Numeric) 1

1 point

- 7) For the instruction encoding discussed in lecture 37, the hexadecimal code of the instruction **MUL R2, R7, R4** will be

- a. 32'h14e41000
- b. 32'h1f231000
- c. 32'h34a37025
- d. 32'h2bc31000

HINT: (Provide numeric constant value as answer, e.g. 90.)

- ☒ a.
- ☐ b.
- ☐ c.
- ☐ d.

Yes, the answer is correct.
Score: 1

Accepted Answers:
a.

1 point

- 8) Consider the following code segment:

```
Loop: ADD      R2, R5, R10
      SUI      R11, R2, 25
      BNEQZ    R11, Loop
```

What will be the hexadecimal machine code for the "BNEQZ R11, Loop" instruction?

- a. 41230000
- b. 3560fffe
- c. 27e2fffe
- d. None of these

HINT: (If options a, b and c are all incorrect, select option d as the answer.)

- ☐ a.
- ☒ b.
- ☐ c.
- ☐ d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
d.

- 9) Consider the 2's complement representation of -3 using 4-bits. If the sign of the number is extended to 16 bits, the resulting value in hexadecimal will be

- a. 8010
- b. fffd
- c. fdfc
- d. None of these

HINT: (If options a, b and c are all incorrect, select option d as the answer.)

- ☐ a.
- ☒ b.
- ☐ c.
- ☐ d.

Yes, the answer is correct.
Score: 1

Accepted Answers:
b.

1 point

- 10) What is the use of HALTED signal in the Verilog implementation of the processor discussed in lecture 40?

- a. To halt the execution of instruction by interrupts from external devices.
- b. To prevent changes due the execution of instructions following the HLT instruction.
- c. To indicate the start of executions of instructions.
- d. None of these.

HINT: (If options a, b and c are all incorrect, select option d as the answer.)

- ☐ a.
- ☒ b.
- ☐ c.
- ☐ d.

Yes, the answer is correct.
Score: 1

Accepted Answers:
b.

1 point

Rate this lesson:

Not at all
useful

Not very
useful

Somewhat
useful

Very useful

Extremely
useful