Assignment 0

The due date for submitting this assignment has passed.

As per our records you have not submitted this assignment.

Due on 2021-07-26, 23:59 IST.

1) What will be the 12-bit binary sign-magnitude representation of decimal number -396? *1 point*

a. 000110001100.
b. 001110001100
c. 100110001100
d. 111110001100

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
c.

2) The smallest binary signed 2's complement 11-bit number is _____ (in decimal). *1 point*

HINT: (Specify the number in decimal, e.g. 26, -37, 98 etc.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) -1024

3) The decimal equivalent of the 2's complement number 1001 is _____. *1 point*

HINT: (Specify the number in decimal, e.g. 26, -37, 98 etc.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) -7

4) Which of the following statement(s) is/are false regarding 2's complement signed binary addition? *1 point*

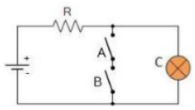
a. Adding two n-bit positive numbers causes an overflow if the result is greater than $2^{n-1} - 1$.
b. Adding two n-bit negative numbers causes an overflow if the result is less than -2^{n-1}.
c. A carry out of most significant $n - 1^{th}$ bit position during addition of two n-bit numbers indicate overflow.
d. None of these.

HINT: (If options a, b and c are all true, select option d as the answer.)

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
c.

5) A lamp (C), two switches (A and B) and a load resistance (R) are connected to a power supply in the following way: *1 point*



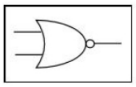
Considering the lamp-ON/ lamp-OFF as logic 1/0 output and switch-open/switch-close as logic 0/1 input, what logic gate functionality does the network realize?

a. A 2-input AND gate.
b. A 2-input NAND gate.
c. A 2-input OR gate.
d. A 2-inut NOR gate.

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
b.

6) How many 2-input NOR gate of following type are required to realize a 5-input NOR gate? *1 point*

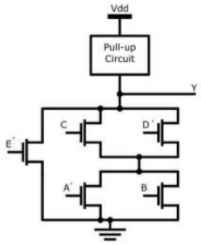


a. 5
b. 6
c. 7
d. 8

○ a.
○ b.
○ c.
○ d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
d.

7) What Boolean function is realized by the following NMOS network (Here X' is used to denote complement of X)? *1 point*



a. $Y = (A'B + CD')E'$.
b. $Y = (A' + B)(C + D') + E'$
c. $Y = (AB' + C'D)E$
d. None of these.

HINT: (If options a, b and c are all incorrect, select option d as the answer.)

○ a.
○ b.
○ c.
○ d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
c.

8) Which of the following set of modules is/are universal ? *1 point*

a. 2-input gate set {AND, OR}
b. 2-input AND gate and NOT gate
c. 2-to-1 Multiplexer
d. 2-input gate set {XOR, AND)

☐ a.
☐ b.
☐ c.
☐ d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
b.
c.
d.

9) How many 2-to-1 multiplexer will be required to realize the following logic function? *1 point*

a	b	c	y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

a. 2
b. 3
c. 4
d. 5

○ a.
○ b.
○ c.
○ d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
c.

10) Which one is the minimal equivalent expression for the following function: *1 point*

$$f = w'x + wxz + wx'yz' + xy$$

a. $f = w'x + xz + wyz' + xy$
b. $f = w'x + xy + wx'yz'$
c. $f = w'x + xz + wyz'$
d. None of these

HINT: (If options a, b and c are all incorrect, select option d as the answer.)

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
c.

11) Which of the following statement(s) is/are true regarding 1's catching problem in SR master-slave flip-flops? *1 point*

a. 1's catching occurs when slave latch is in 0 state and master latch have a static-0 hazard at S-input during the active clock state.
b. 1's catching occurs when slave latch is in 0 state and master latch have a static-0 hazard at R-input during the active high clock state.
c. 1's catching occurs when slave latch is in 1 state and master latch have a static-0 hazard at S-input during the active high clock state.
d. 1's catching occurs when slave latch is in 1 state and master latch have a static-0 hazard at R-input during the active high clock state.

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
a.

12) Which flip-flop does not suffer from 0's and 1's catching problem? *1 point*

a. JK
b. D
c. T
d. All of these

HINT: (If options a, b and c are all correct, select option d as the answer.)

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
b.

13) Which physical design is not preferable for hardware realization when higher system speed is a requirement? *1 point*

a. Gate Array
b. FPGA
c. Standard Cell
d. Full Custom

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
b.

14) Which physical implementation does not require fabrication stage and thus reduces development time and cost? *1 point*

a. Gate Array
b. FPGA
c. Standard Cell
d. Full Custom

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
b.

15) Which of the following statement(s) is/are true regarding simulation and synthesis of logic circuit? *1 point*

a. Simulation is the analysis of a designed circuit model at some higher level of abstraction in a software environment.
b. Synthesis is the analysis of a designed circuit model at some higher level of abstraction in a software environment.

c. Synthesis is the process of translating a designed circuit model at some level to the next lower level of abstraction.

d. Simulation is the process of translating a designed circuit model at some level to the next lower level of abstraction.

- [ ] a.
- [ ] b.
- [ ] c.
- [ ] d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
a.
c.

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