

Course outline

How does an NPTEL online course work?

Week 0

Week 1

Week 2

Week 3

Week 4

Week 5

Week 6

Lecture 25 : DATAPATH AND CONTROLLER DESIGN (PART 1)

Lecture 26 : DATAPATH AND CONTROLLER DESIGN (PART 2)

Lecture 27 : DATAPATH AND CONTROLLER DESIGN (PART 3)

Lecture 28 : SYNTHESIZABLE VERILOG

Lecture 29 : SOME RECOMMENDED PRACTICES

Week 6 Lecture Material

Quiz: Week 6 : Assignment 6

Week 6 : Programming Assignment 1

Feedback Form of Week 6

Week 7

Week 8

Assignments Solution

Download Videos

Text Transcripts

Live Interactive session

Books

Week 6 : Assignment 6

The due date for submitting this assignment has passed.

Due on 2021-09-08, 23:59 IST.

Assignment submitted on 2021-09-08, 13:03 IST

1) Which of the following statement(s) is/are true for designing complex digital systems? 1.25 points

- a. The system is partitioned into subparts, namely data path, control path and finite-state machine.
- b. The system is partitioned into subparts, namely data path, control path and storage registers.
- c. Complex system is partitioned into subparts, namely data path and control path.
- d. All of these.

HINT: (If options a, b and c are all correct, select option d as the answer.)

- ☐ a.
- ☐ b.
- ☒ c.
- ☐ d.

Yes, the answer is correct.
Score: 1.25

Accepted Answers:
c.

2) Which of the following types of functional units may be present in a data path? 1.25 points

- a. Counters/registers.
- b. Clock and clear/reset signals.
- c. Multiplexers/adders/other functional blocks.
- d. All of these.

HINT: (If options a, b and c are all correct, select option d as the answer.)

- ☐ a.
- ☐ b.
- ☒ c.
- ☐ d.

Partially Correct.
Score: 0.625

Accepted Answers:
a.
c.

3) Which of the following set of components are part of the data path and control path for the hardware module multiplication by repeated addition discussed in lecture 25. 1.25 points

- a. Data Path = {A, P, B, ADDER, COMP, LdA, LdP, clrP, LdB, decB, eqz, bus, data_in}
- b. Data Path = {A, P, B, ADDER, COMP, eqz, bus}
- c. Control Path = {LdA, LdP, clrP, LdB, decB, start, done, data_in, clk}
- d. Control Path = {LdA, LdP, clrP, LdB, decB, done}

- ☒ a.
- ☐ b.
- ☒ c.
- ☐ d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
b.
d.

4) The control signal generation for the multiplication by repeated addition module discussed in lecture 25 is partially shown below. 1.25 points

```
always @(state) begin
    case (state)
        S0: begin #1 LdA = 0; LdB = 0; LdP = 0; clrP = 0; decB = 0; end
        S1: begin #1 LdA = 1; end
        S2: begin #1 LdA = 0; LdB = 1; clrP = 1; end
        S3: begin #1 LdB = 0; LdP = 1; clrP = 0; decB = 1; end
        S4: begin #1 done = 1; LdB = 0; LdP = 0; decB = 0; end
        default: begin #1 LdA = 0; LdB = 0; LdP = 0; clrP = 0; decB = 0; end
    endcase
end
```

Which of the following statement(s) is/are true about the generation?

- a. All the signal functions will be realized as combinational functions.
- b. Each signal function will be realized by a 1-bit latch or flip-flop.
- c. Some of the signal function will be realized by latch or flip-flop and others as combinational functions.
- d. None of these.

HINT: (If options a, b and c are all false, select option d as the answer.)

- ☐ a.
- ☒ b.
- ☐ c.
- ☐ d.

Yes, the answer is correct.
Score: 1.25

Accepted Answers:
b.

5) Which of the following design style is/are considered as recommended approach for modeling 1.25 points

data and control path?

- a. Both state change and computation are carried out in a clock triggered procedural block.
- b. Only state change is carried out in a clock triggered procedural block.
- c. Only computation is carried out in a clock triggered procedural block.
- d. None of these.

HINT: (If options a, b and c are all incorrect, select option d as the answer.)

- ☐ a.
- ☒ b.
- ☐ c.
- ☐ d.

Yes, the answer is correct.
Score: 1.25

Accepted Answers:
b.

6) Assume the clock pulse is generated in the following way:

```
reg clk = 0;  
always #10 clk = ~clk;
```

Simulating the **multiplication by repeated addition** discussed in lecture 25 with inputs

```
#3 start = 1'b1;  
#23 data_in = 5;  
#20 data_in = 3;
```

the outcome 15 will be observed after _____ (in decimal) clock periods with **done** signal indicating the end of computation.

70

Hint

No, the answer is incorrect.
Score: 0

Accepted Answers:
(Type: Range) 6,7

1.25 points

7) Which of the following signal(s) is/are not parts of the data path in GCD computation discussed in lecture 26?

1.25 points

- a. The signal LdA for loading data in register A.
- b. The signal LT indicating value stored in register A is less than that of register B.
- c. The signal done indicating the end of GCD computation.
- d. None of these.

HINT: (If options a, b and c are all incorrect, select option d as the answer.)

- ☐ a.
- ☐ b.
- ☒ c.
- ☐ d.

Partially Correct.
Score: 0.625

Accepted Answers:
a.
c.

8) Which of the following statements is/are true about the two approaches for modeling GCD computation discussed in lecture 26?

1.25 points

- a. Both the approaches required identical hardware components when synthesized.
- b. Alternate approach requires more storage than previous one.
- c. Alternate approach requires less storage than previous one.
- d. None of these.

HINT: (If options a, b and c are all incorrect, select option d as the answer.)

- ☐ a.
- ☒ b.
- ☐ c.
- ☐ d.

Yes, the answer is correct.
Score: 1.25

Accepted Answers:
b.

Rate this lesson:

Not at all
useful

Not very
useful

Somewhat
useful

Very useful

Extremely
useful