Week 5 : Assignment 5

The due date for submitting this assignment has passed.

Due on 2021-09-01, 23:59 IST.

Assignment submitted on 2021-09-01, 19:15 IST

1) Which of the following statement(s) is/are true about Verilog test benches? *1 point*

a. Test benches may contain more than one initial block to generate input stimuli for simulating a designed module.
b. Test benches may contain both initial and always block to generate input stimuli for simulating the designed module.
c. Input and output ports of the DUT require explicit connection to the test bench.
d. All of the above.

HINT: (If options a, b and c are all true, select option d as the answer.)

a.
b.
c.
d.

Yes, the answer is correct.
Score: 1
Accepted Answers:
d.

2) Consider the following Verilog code:

```
and   #10   G1 (t1,A,B);
or    #20   G2 (t2,C,~B,D);
nor   #15   G3 (t3,E,F);
nand  #7    G4 (Y,t1,t2,t3);
```

If all the inputs A, B, C, D, E and F are fed with some logic value at the same time, after a delay of _____ time unit the correct logic value at the output port Y of nand gate will be observed.

27

Hint

Yes, the answer is correct.
Score: 1
Accepted Answers:
(Type: Numeric) 27

1 point

3) If inputs for the gates defined in **Q.2** is assigned as A = 1, B = 1, C = 0, D = 1, E = 0 and F = 0, the final output at port Y will be _____. *1 point*

0

Hint

Yes, the answer is correct.
Score: 1
Accepted Answers:
(Type: Numeric) 0

4) Consider the following Verilog statement: *1 point*

```
input [7:0] X;
input [2:0] Y;
assign out = X[Y];
```

For the following assignments

```
#2 Y = 5;
#2 X = 5 << 3;
```

what will be the logic value of **out** and after what time interval the logic value will be observed?

a. out = 0, time interval = 2
b. out = 1, time interval = 2
c. out = 0, time interval = 4
d. out = 1, time interval = 4

a.
b.
c.
d.

Yes, the answer is correct.
Score: 1
Accepted Answers:
d.

5) Which of the following is/are the design convention(s) for realizing Mealy machine? *1 point*

a. Blocking assignments are used for both state update and output generation.
b. Blocking assignments are used only for output generation.
c. State change logic is implemented separately using non-blocking assignments triggered by clock.
d. None of the above.

HINT: (If options a, b and c are all incorrect, select option d as the answer.)

b.
c.
d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
d.

6) Which of the following is/are true about Verilog simulator directive? *1 point*

a. $display directive is event-driven and print the values whenever changes in values of variable are occurred.
b. $monitor directive is event-driven and print the values whenever changes in values of variable are occurred.
c. $dumpon directive is used to write the current values of all variables whenever changes in values of variable are occurred.
d. $dumpall directive is used to write the current values of all variables regardless of changes in values of these variables.

a.
b.
c.
d.

Yes, the answer is correct.
Score: 1

Accepted Answers:
b.
d.

7) Consider the following Verilog code: *1 point*

```
module fun (clock, clear, in, out);
      input clock, clear, in;
      output reg out;
      reg X, Y, Z;
      always @(posedge clock or negedge clear) begin
            if (!clear) begin X<=0; Y<=0; Z<=0; out<=0; end
            else begin
                  out <= Z;
                  Z <= Y;
                  Y <= X;
                  X <= in;
            end
      end
endmodule
```

Which of the following statements is/are true?

a. Represent a 1-bit register with register with asynchronous reset.
b. Represent a 1-bit register with register with synchronous reset.
c. Represent a 4-bit register with asynchronous reset.
d. Represent a 4-bit shift register with asynchronous reset.
e. None of the above

HINT: (If options a, b, c and d are all false, select option e as the answer.)

a.
b.
c.
d.
e.

Yes, the answer is correct.
Score: 1

Accepted Answers:
d.

8) Consider the following Verilog code: *1 point*

```
module fun (clear, clock, X);
      parameter N = 7;
      input clear, clock;
      output reg [0:N] X;
      always @(negedge clock)
            if (clear)
                  X <= 0;
            else
                  X <= X + 1;

endmodule
```

Which of the following statements is/are true?

a. The module represents a 7-bit counter with synchronous active low reset.
b. The module represents a 8-bit counter with synchronous active high reset.
c. The module represents a 7-bit counter with asynchronous active low reset.
d. The module represents a 8-bit counter with asynchronous active high reset.
e. None of the above

HINT: (If options a, b, c and d are all false, select option e as the answer.)

a.
b.
c.
d.
e.

Yes, the answer is correct.
Score: 1

Accepted Answers:
b.

9) Which of the following statements is/are true about FSM? *1 point*

a. In Mealy machine state transition is a function of present state and present input.
b. In Moore machine state transition is a function of present state and present input.
c. In Mealy machine state transition is a function of only present state.
d. In Moore machine state transition is a function of only present state.

- [x] a.
- [ ] b.
- [ ] c.
- [x] d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
a.
b.

10) Which of the following statements is/are true about FSM? *1 point*

a. Keeping the output function in an always block triggered by FSM state (and input) minimizes number of flip-flop when synthesized.
b. Keeping the output function in an always block triggered by the clock minimizes number of flip-flop when synthesized.
c. None of the above.

HINT: (If options a, and b are all false, select option c as the answer.)

- (•) a.
- ( ) b.
- ( ) c.

Yes, the answer is correct.
Score: 1

Accepted Answers:
a.

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