Week 4 : Assignment 4

The due date for submitting this assignment has passed.

Due on 2021-09-01, 23:59 IST.

Assignment submitted on 2021-09-01, 19:03 IST

1) Consider the procedural assignment expression of the form

target = expression
or
target <= expression

Which of the following(s) is/are valid target of such assignment expression?

a. A scalar or vector net type variable.
b. A scalar net type or register type variable.
c. A scalar or vector register type variable.
d. All of the above.

HINT: (If options a, b, and c are all valid, select option d as the answer.)

1 point

- (○) a.
- (○) b.
- (◉) c.
- (○) d.

Yes, the answer is correct.
Score: 1

Accepted Answers:
c.

2) Which of the following(s) is/are true about blocking assignments?

a. The targets of all blocking assignments in a procedural block of a module are updated in sequence.
b. The targets of all blocking assignments in all the procedural blocks of a module are updated in sequence.
c. The targets of blocking assignments appearing in two different procedural blocks of a module are updated in parallel.
d. None of the above.

HINT: (If options a, b, and c are all valid, select option d as the answer.)

1 point

- (☑) a.
- (☐) b.
- (☑) c.
- (☐) d.

Yes, the answer is correct.
Score: 1

Accepted Answers:
a.
c.

3) Consider the following Verilog code segment

```
reg [3:0] w, x, y, z;
initial begin
    w = #2 7;  x = #2 9;  y = #2 4;  z = #2 13;
    w = #2 x | y;
    x = #2 y & z;
    y = #2 y ^ z;
end
```

What will be the value of variables w, x, y, and z after time interval of 10 units?

a. w = 7, x = 9, y = 4, z = 13
b. w = 13, x = 9, y = 4, z = 13.
c. w = 7, x = 9, y = 4, z = x.
d. w = 13, x = 4, y = 4, z = 13.
e. None of the above.

HINT: (If options a, b, c and d are all incorrect, select option e as the answer.)

1 point

- (○) a.
- (◉) b.
- (○) c.
- (○) d.
- (○) e.

Yes, the answer is correct.
Score: 1

Accepted Answers:
b.

4) Consider the following Verilog code segment

```
reg [3:0] w, x, y, z;
initial begin
    w = 7;  x = 9;  y = 4;  z = 13;
end
initial begin
    w <= #2 x | y;
    x <= #2 y & z;
    y <= #2 y ^ z;
end
```

What will be the value of variables w, x, y, and z after time interval of 4 units?

1 point

a. w = 7, x = 9, y = 4, z = 13
b. w = 13, x = 9, y = 4, z = 13.
c. w = 13, x = 4, y = 9, z = 13.
d. w = 13, x = 4, y = 4, z = 13.
e. None of the above.

HINT: (If options a, b, c and d are all incorrect, select option e as the answer.)

- ○ a.
- ○ b.
- ◉ c.
- ○ d.
- ○ e.

Yes, the answer is correct.
Score: 1
Accepted Answers:
c.

5) Which of the following(s) is/are considered recommended styles for modeling circuits? *1 point*

a. Blocking assignments are used to generate combinational circuits.
b. Non-blocking assignments are used to generate combinational circuits.
c. Blocking assignments are used to generate sequential circuits.
d. Non-blocking assignments are used to generate sequential circuits.
e. None of the above.

HINT: (If options a, b, c and d are all incorrect, select option e as the answer.)

- ☑ a.
- ☐ b.
- ☐ c.
- ☑ d.
- ☐ e.

Yes, the answer is correct.
Score: 1
Accepted Answers:
a.
d.

6) Which of the following(s) represent(s) a Verilog race condition? *1 point*

a. The RHS variable of a blocking assignment in one procedural block is also the LHS variable of another blocking assignment in another procedural block and both assignments are scheduled to execute in the same simulation time step.
b. The RHS variable of a non-blocking assignment in one procedural block is also the LHS variable of another non-blocking assignment in another procedural block and both assignments are scheduled to execute in the same simulation time step.
c. None of the above.

HINT: (If options a, and b are incorrect, select option c as the answer.)

- ◉ a.
- ○ b.
- ○ c.

Yes, the answer is correct.
Score: 1
Accepted Answers:
a.

7) Consider the following Verilog code segment:

```
initial begin
      clk = 0;
      forever #5 clk = ~clk;
end
always @(posedge clk) begin
      x <= #2 a & ~b;
      y <= #2 b | ~c;
end
always @(posedge clk)
      f <= #2 t1 ^ t2;
```

In simulating the code segment initializing input variables a, b, and c after a delay of time 4 units, an output in port f will be observed at time _____ unit.

18

Hint

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 7

1 point

8) Which of the following statement(s) is/are true regarding user defined primitives? *1 point*

a. A functional block with more than one output cannot be modeled using UDP.
b. UDP functional block must be specified completely, i.e. output is defined for all possible inputs.
c. Symbol x denotes a “don’t care” value that can only appear at the output field of an UDP.
d. None of the above.

HINT: (If options a, b and c are all false, select option d as the answer.)

- ◉ a.
- ○ b.
- ○ c.
- ○ d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
d.

9) Consider the following UDP

```
primitive fun(f, x, y, z);
     input x, y, z;
     output f;
     table
          // x y z   f
             0 0 0 : 1;
             0 0 1 : 0;
             0 1 ? : 0;
             1 0 0 : 1;
             1 0 1 : 0;
             1 1 0 : 0;
             1 1 1 : 1;
     endtable
endprimitive
```

Simulating the UDP initializing the inputs x, y, and z in the following way

```
reg [3:0] out;
integer i;
for (i = 0; i <= 7; i = i + 1) begin
     if ( i % 2 == 0) begin
          #2 {x, y, z } = i;
          #2 out = {out[2:0], f};
     end
end
```

the value of variable `out` after the end of for loop will be _____ (in binary).

4'b1001

Hint

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: String) 4'b1010

1 point

10) Which of the following Boolean function is realized by the UDP defined in Q.9?

1 point

a. x'y'z' + xy'z + xyz.
b. y'z' + xyz.
c. x'y'z + x'y + xy'z + xyz'.
d. None of the above.

HINT: (If options a, b and c are all incorrect, select option d as the answer.)

- a.
- b.
- c.
- d.

Yes, the answer is correct.
Score: 1
Accepted Answers:
b.

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