

THỰC HÀNH KIẾN TRÚC MÁY TÍNH

WEEK 12

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Assignment 1:

- Thực hiện từ bước 1 đến bước 7 với chương trình row-major:

The screenshot displays the Mars MIPS simulator interface. The main window shows assembly code for a program named 'week12.mips.asm'. The code includes instructions for moving values between registers, multiplying, and storing data. A 'Data Cache Simulation Tool, Version 1.2' dialog box is open, showing cache organization settings (Direct Mapping, 8 blocks, 4 words, 128 bytes) and performance metrics (Memory Access Count: 32, Cache Hit Count: 24, Cache Miss Count: 8, Cache Hit Rate: 75%). The registers window on the right shows the state of various registers, including \$zero, \$at, \$v0, \$v1, \$a0, \$a1, \$a2, \$a3, \$t0, \$t1, \$t2, \$t3, \$t4, \$t5, \$t6, \$t7, \$t8, \$t9, \$k0, \$k1, \$gp, \$sp, \$ra, \$pc, \$hi, and \$lo.

- Kết quả cuối cùng

This screenshot shows the final state of the Mars MIPS simulator. The assembly code window displays the complete program, including the 'syscall' instruction. The registers window on the right shows the final values of the registers, with \$v0 and \$v1 highlighted in green. The 'Data Cache Simulation Tool' dialog box is also visible, showing the final performance metrics (Memory Access Count: 256, Cache Hit Count: 192, Cache Miss Count: 64, Cache Hit Rate: 75%).

- Tỷ lệ cache hit rate cuối cùng là 75%. Vì với mỗi lần bỏ lỡ, một khối 4- word được ghi vào bộ đệm. Trong một đường truyền chính theo hàng, các phần tử của ma trận là được truy cập theo cùng thứ tự chúng được lưu trữ trong bộ nhớ. Do đó, mỗi lần bỏ lỡ bộ đệm là theo sau là 3 lần truy cập vì 3 phần tử tiếp theo được tìm thấy trong cùng một khối bộ đệm. Tiếp theo là một lỗi khác khi ma trận trực tiếp ánh xạ tới khối bộ đệm tiếp theo và sau đó lặp đi lặp lại chính nó. Vì vậy, 3 trong số 4 lần truy cập bộ nhớ sẽ được giải quyết trong bộ đệm.

- Dự đoán, khi tăng blocksize từ 4 lên 8 thì tỉ lệ Cache hit rate là 87,5%, còn khi giảm blocksize từ 4 xuống 2 thì tỉ lệ Cache hit rate còn 50% .

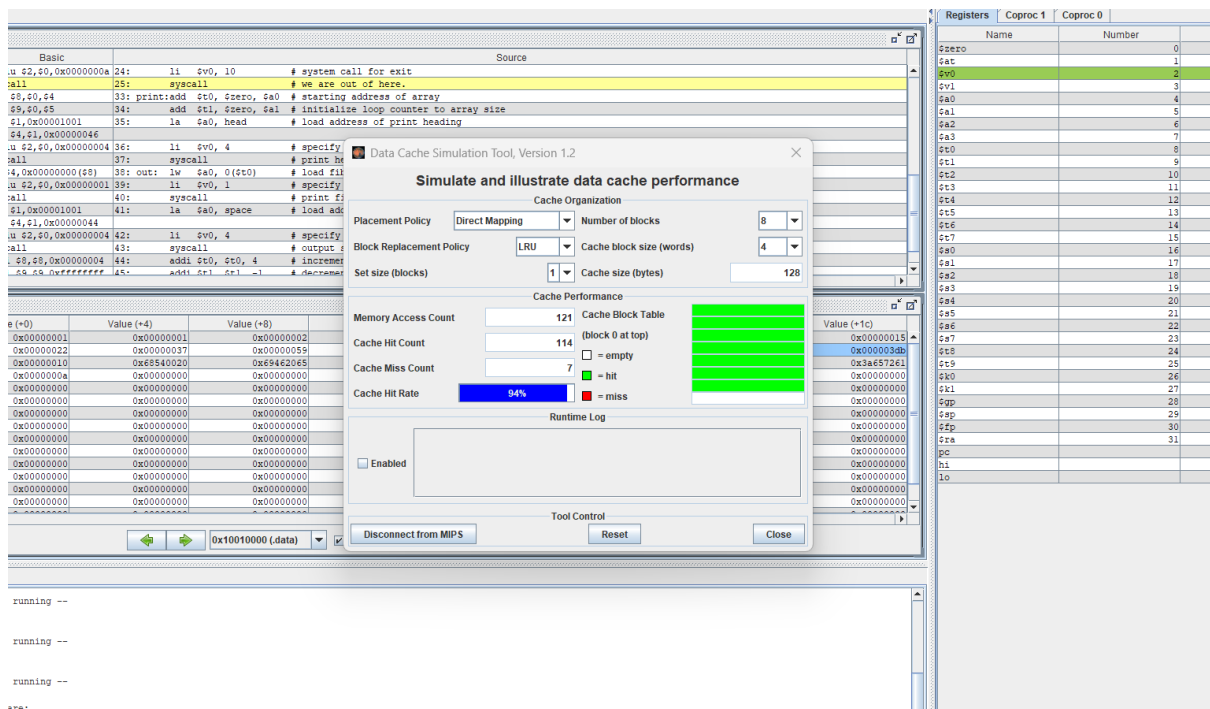
- Hiệu suất bộ đệm cũng bằng tỉ lệ Cache hit rate và bằng 75%.

- Trường hợp chạy chương trình column:

The screenshot shows the 'Data Cache Simulation Tool' interface. The main window displays assembly code for a column-major traversal of a 16x16 matrix. A 'Data Cache Simulation Tool' dialog box is open, showing 'Simulate and illustrate data cache performance' settings. The 'Cache Organization' section shows 'Direct Mapping' placement policy, 'LRU' block replacement policy, 8 blocks, and 4 words per block. The 'Cache Performance' section shows a 'Memory Access Count' of 256, 'Cache Hit Count' of 0, 'Cache Miss Count' of 256, and a 'Cache Hit Rate' of 0%. The 'Runtime Log' is empty. The 'Tool Control' section has 'Disconnect from MIPS', 'Reset', and 'Close' buttons. The background shows the MIPS assembly code and a register window on the right.

- Khi chạy chương trình column, tỉ lệ Cache hit rate là 0%, suy ra hiệu suất bộ nhớ đệm cũng là 0%

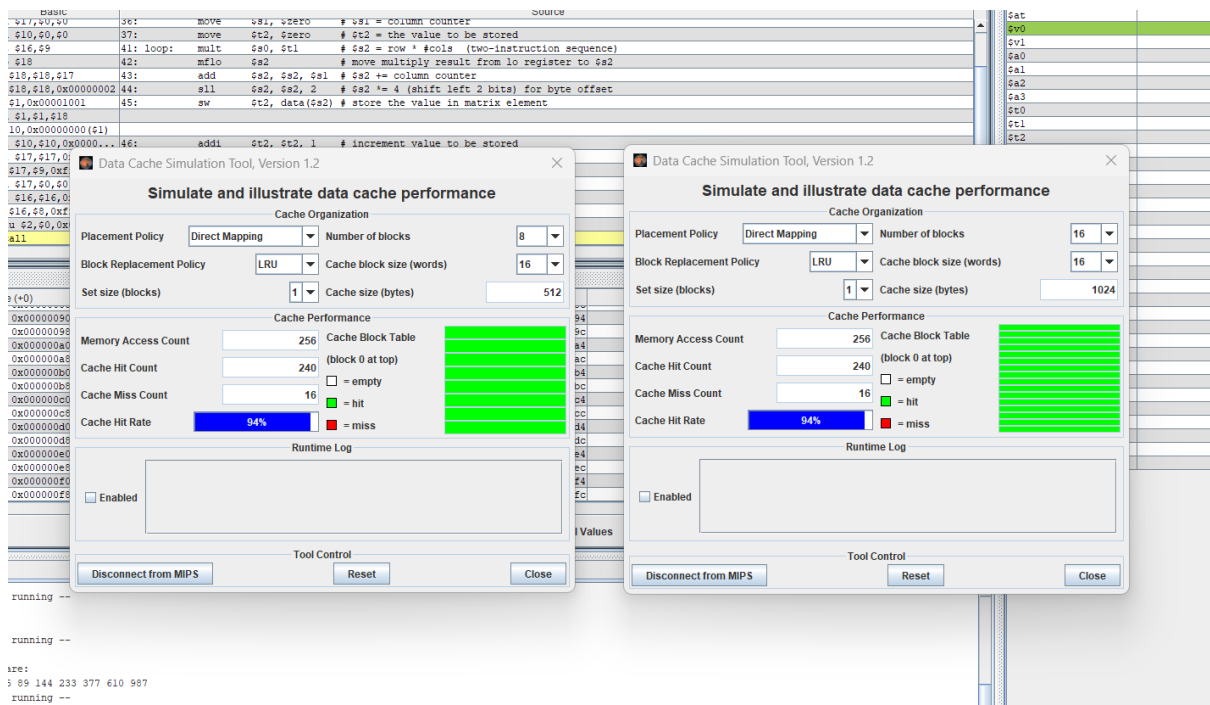
- Trường hợp chạy chương trình Fibonacci:



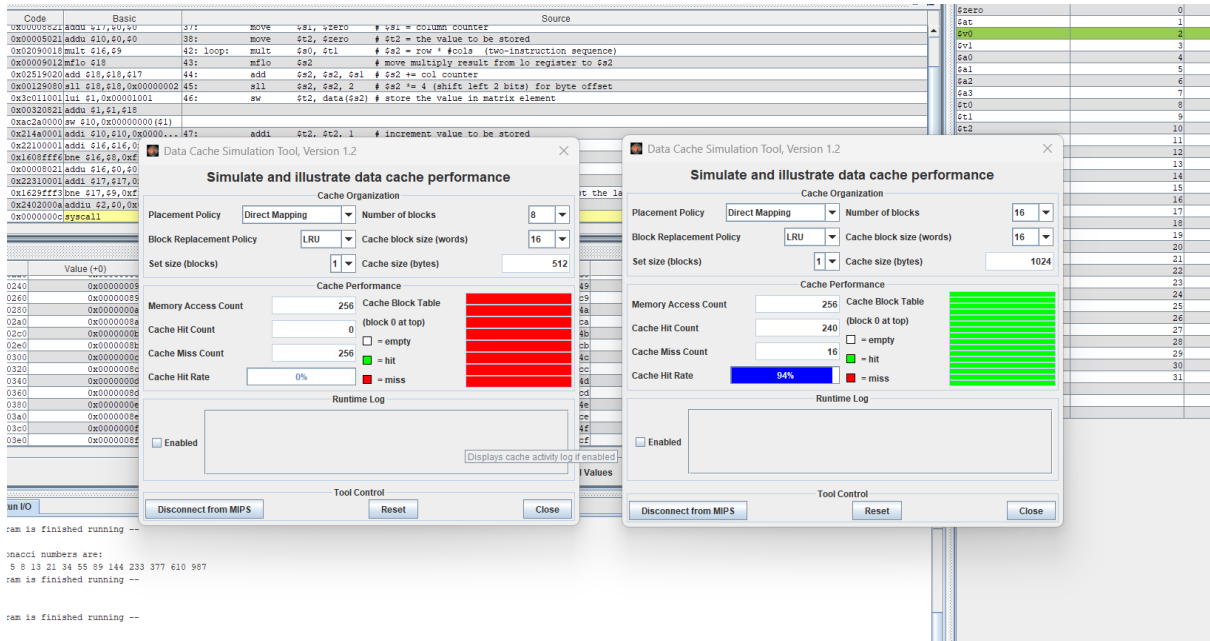
- Khi chạy chương trình Fibonacci, hiệu suất bộ nhớ đệm là 94%.

- Thực hiện từ bước 13 đến bước 15 (Trong các ảnh kết quả, cửa sổ dữ liệu cache bên trái là bản gốc, cửa sổ data cache bên phải là bản mới):

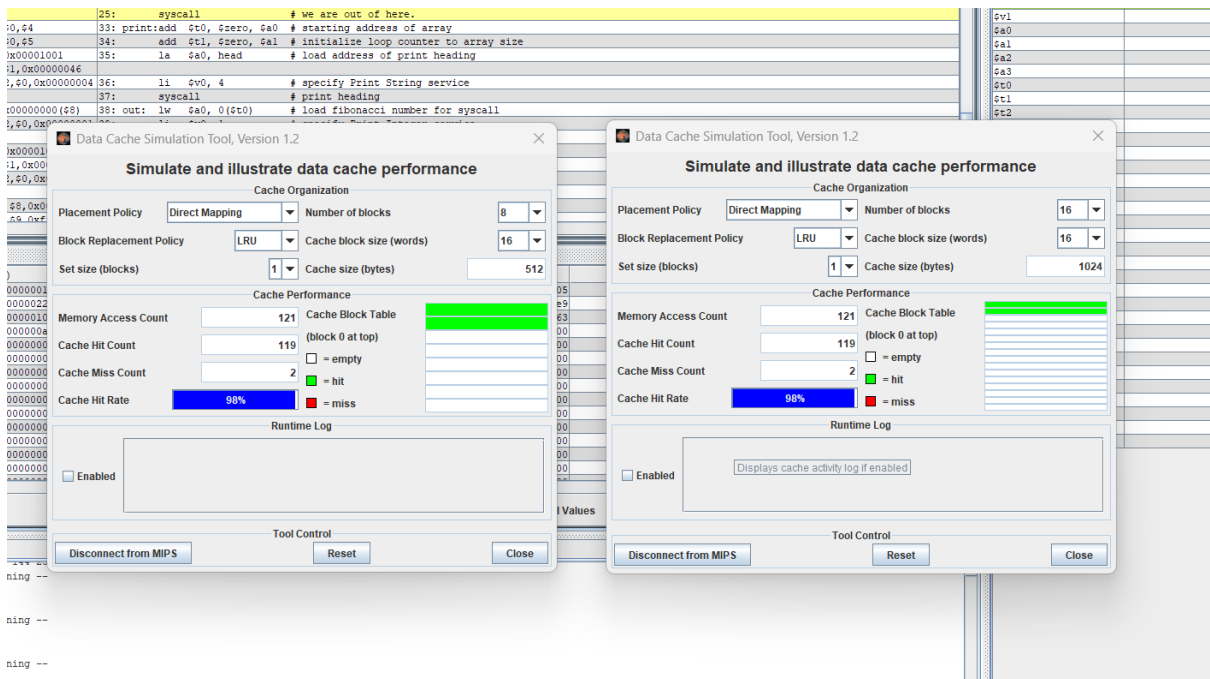
+ Khi chạy chương trình row-major:



+ Khi chạy chương trình column-major:



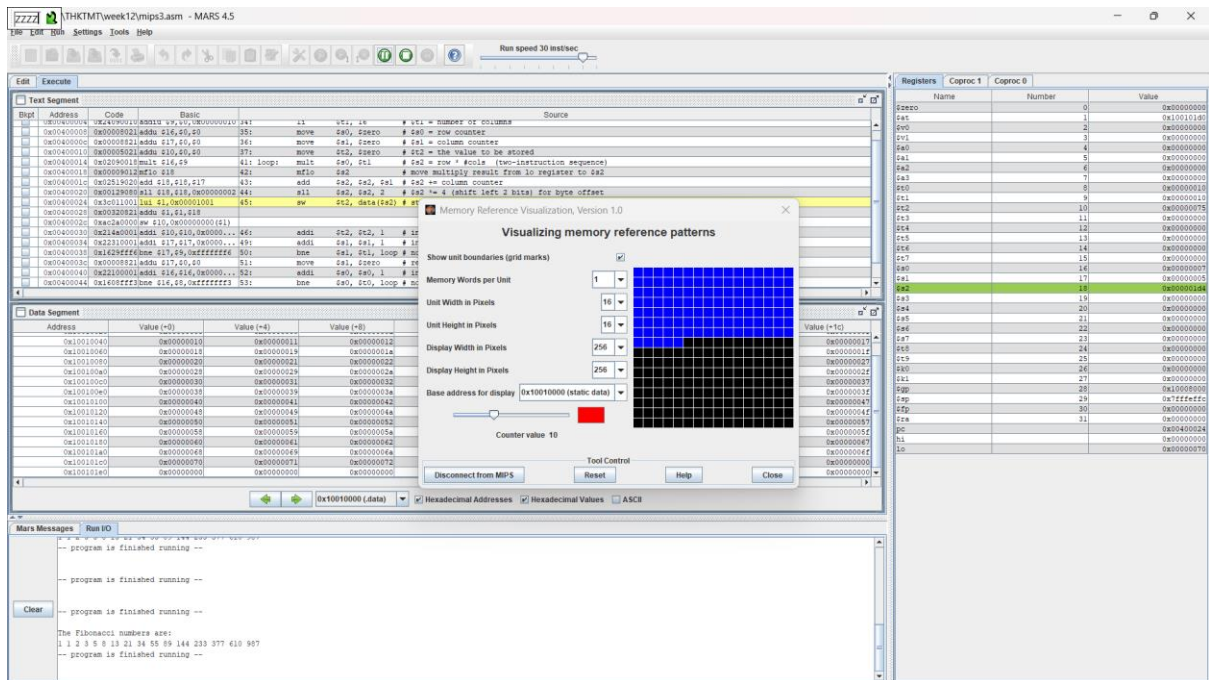
- Khi chạy chương trình Fibonacci:



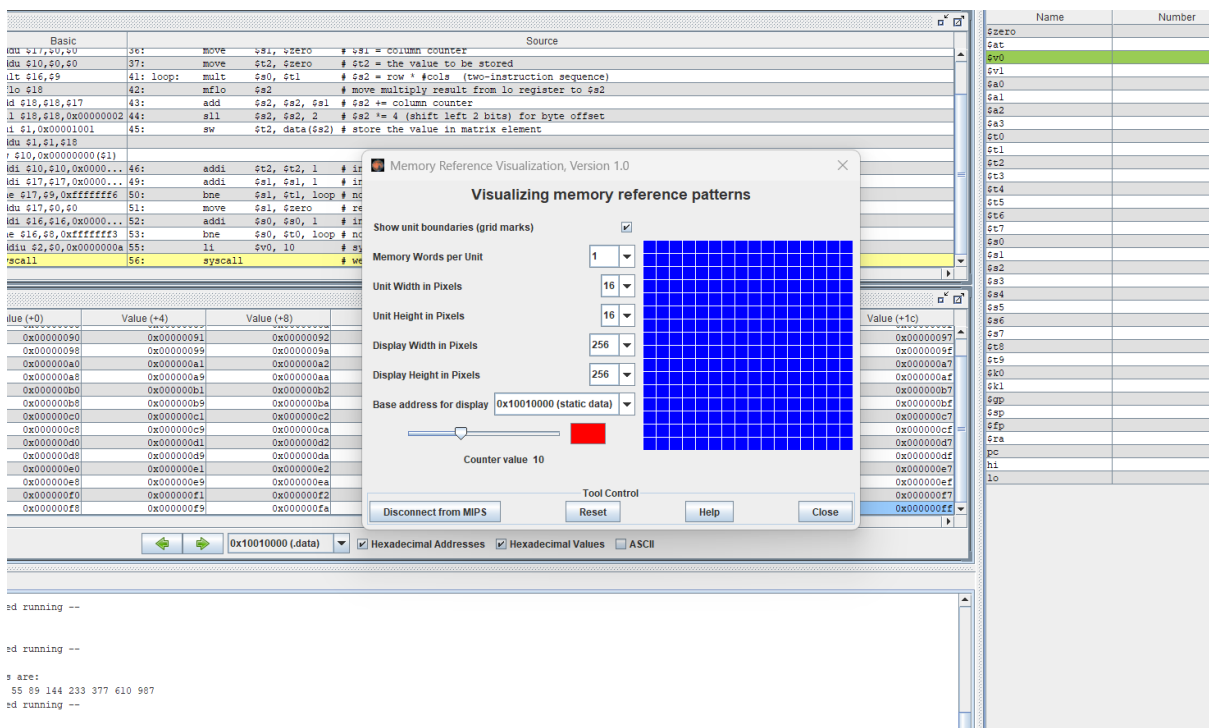
Assignment 2:

- Với chương trình row-major:

+ Khi đang chạy chương trình:

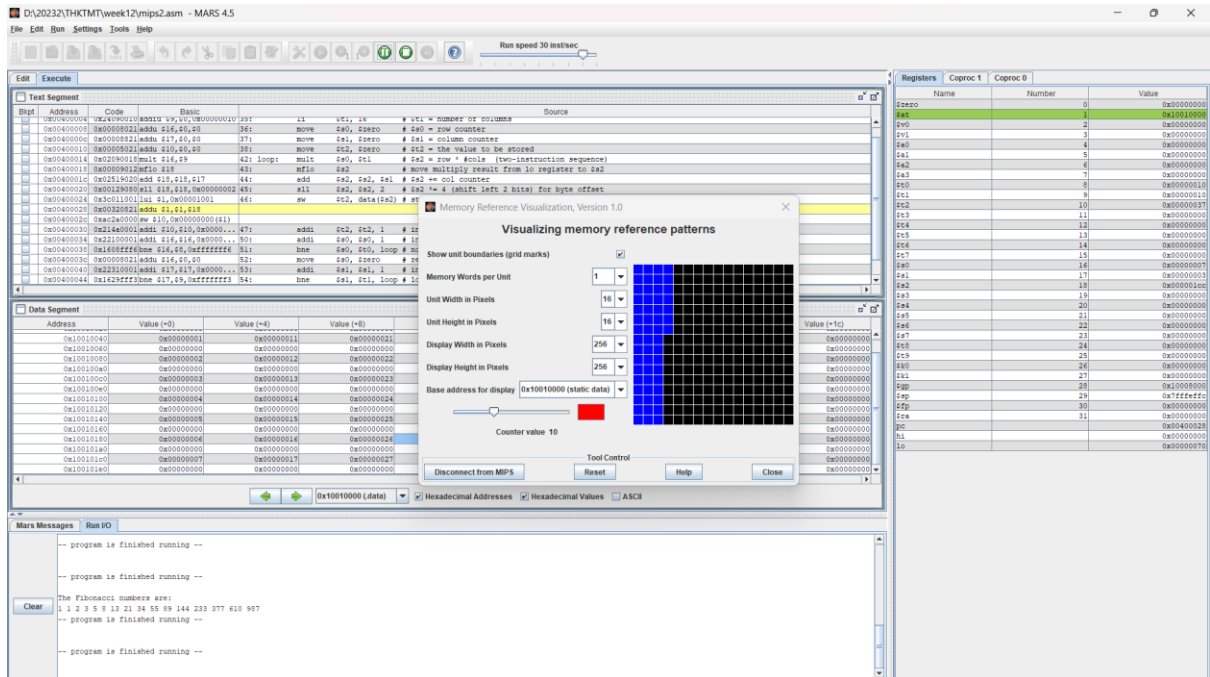


+ Khi đã chạy xong chương trình:

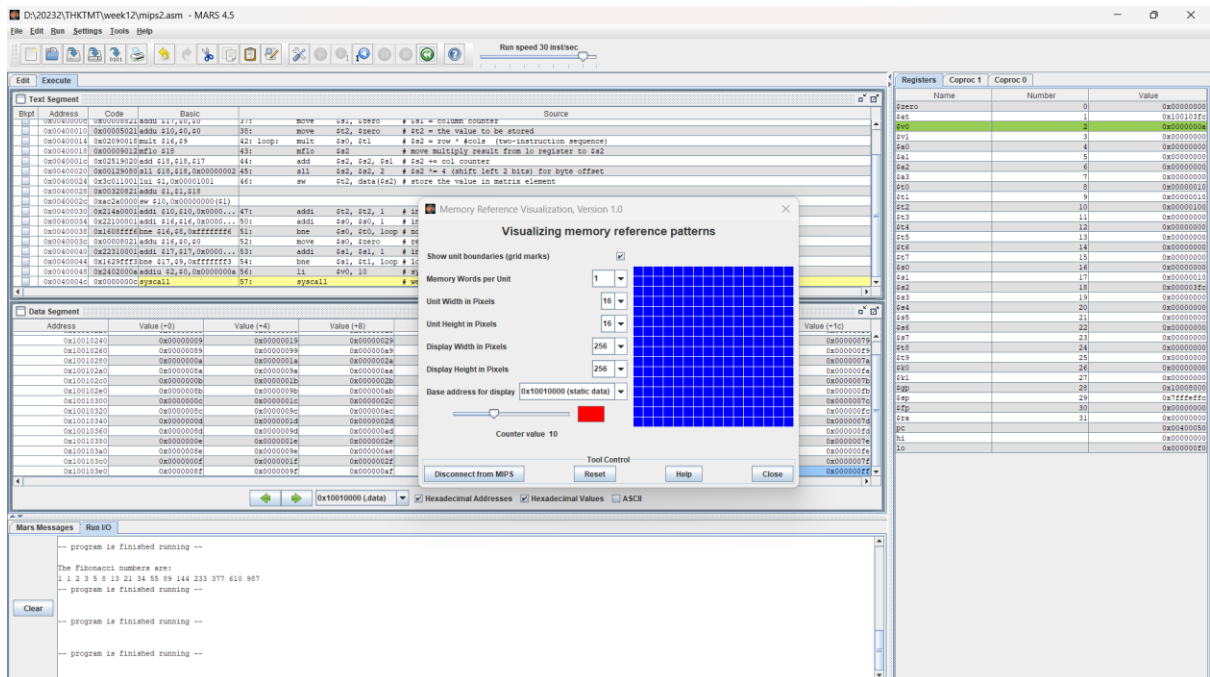


- Với chương trình column-major:

+ Khi chương trình đang chạy:



+ Khi đã chạy xong chương trình



- Với chương trình Fabonacci:

+ Khi chương trình đang chạy:

D:\2023\THKMT\week12\mpis1.asm - MARS 4.5

File Edit Run Settings Tools Help

Run speed 30 inst/sec

Test Segment

Inst	Address	Code	Basic	Source
0x00000000	0x40000000	li \$t0, \$zero	li \$t0, \$zero	# load address of array
0x00000001	0x40000001	li \$t1, 1	li \$t1, 1	# load address of size variable
0x00000002	0x40000002	li \$t2, 0	li \$t2, 0	# load array size
0x00000003	0x40000003	li \$t3, 1	li \$t3, 1	# 1 is first and second Fib. number
0x00000004	0x40000004	li \$t4, 0	li \$t4, 0	# \$t4 = 1
0x00000005	0x40000005	li \$t5, 0	li \$t5, 0	# \$t5 = 1
0x00000006	0x40000006	li \$t6, 0	li \$t6, 0	# \$t6 = 1
0x00000007	0x40000007	li \$t7, 0	li \$t7, 0	# \$t7 = 1
0x00000008	0x40000008	li \$t8, 0	li \$t8, 0	# \$t8 = 1
0x00000009	0x40000009	li \$t9, 0	li \$t9, 0	# \$t9 = 1
0x0000000A	0x4000000A	li \$tA, 0	li \$tA, 0	# \$tA = 1
0x0000000B	0x4000000B	li \$tB, 0	li \$tB, 0	# \$tB = 1
0x0000000C	0x4000000C	li \$tC, 0	li \$tC, 0	# \$tC = 1
0x0000000D	0x4000000D	li \$tD, 0	li \$tD, 0	# \$tD = 1
0x0000000E	0x4000000E	li \$tE, 0	li \$tE, 0	# \$tE = 1
0x0000000F	0x4000000F	li \$tF, 0	li \$tF, 0	# \$tF = 1
0x00000010	0x40000010	li \$t10, 0	li \$t10, 0	# \$t10 = 1
0x00000011	0x40000011	li \$t11, 0	li \$t11, 0	# \$t11 = 1
0x00000012	0x40000012	li \$t12, 0	li \$t12, 0	# \$t12 = 1
0x00000013	0x40000013	li \$t13, 0	li \$t13, 0	# \$t13 = 1
0x00000014	0x40000014	li \$t14, 0	li \$t14, 0	# \$t14 = 1
0x00000015	0x40000015	li \$t15, 0	li \$t15, 0	# \$t15 = 1
0x00000016	0x40000016	li \$t16, 0	li \$t16, 0	# \$t16 = 1
0x00000017	0x40000017	li \$t17, 0	li \$t17, 0	# \$t17 = 1
0x00000018	0x40000018	li \$t18, 0	li \$t18, 0	# \$t18 = 1
0x00000019	0x40000019	li \$t19, 0	li \$t19, 0	# \$t19 = 1
0x0000001A	0x4000001A	li \$t1A, 0	li \$t1A, 0	# \$t1A = 1
0x0000001B	0x4000001B	li \$t1B, 0	li \$t1B, 0	# \$t1B = 1
0x0000001C	0x4000001C	li \$t1C, 0	li \$t1C, 0	# \$t1C = 1
0x0000001D	0x4000001D	li \$t1D, 0	li \$t1D, 0	# \$t1D = 1
0x0000001E	0x4000001E	li \$t1E, 0	li \$t1E, 0	# \$t1E = 1
0x0000001F	0x4000001F	li \$t1F, 0	li \$t1F, 0	# \$t1F = 1
0x00000020	0x40000020	li \$t20, 0	li \$t20, 0	# \$t20 = 1
0x00000021	0x40000021	li \$t21, 0	li \$t21, 0	# \$t21 = 1
0x00000022	0x40000022	li \$t22, 0	li \$t22, 0	# \$t22 = 1
0x00000023	0x40000023	li \$t23, 0	li \$t23, 0	# \$t23 = 1
0x00000024	0x40000024	li \$t24, 0	li \$t24, 0	# \$t24 = 1
0x00000025	0x40000025	li \$t25, 0	li \$t25, 0	# \$t25 = 1
0x00000026	0x40000026	li \$t26, 0	li \$t26, 0	# \$t26 = 1
0x00000027	0x40000027	li \$t27, 0	li \$t27, 0	# \$t27 = 1
0x00000028	0x40000028	li \$t28, 0	li \$t28, 0	# \$t28 = 1
0x00000029	0x40000029	li \$t29, 0	li \$t29, 0	# \$t29 = 1
0x0000002A	0x4000002A	li \$t2A, 0	li \$t2A, 0	# \$t2A = 1
0x0000002B	0x4000002B	li \$t2B, 0	li \$t2B, 0	# \$t2B = 1
0x0000002C	0x4000002C	li \$t2C, 0	li \$t2C, 0	# \$t2C = 1
0x0000002D	0x4000002D	li \$t2D, 0	li \$t2D, 0	# \$t2D = 1
0x0000002E	0x4000002E	li \$t2E, 0	li \$t2E, 0	# \$t2E = 1
0x0000002F	0x4000002F	li \$t2F, 0	li \$t2F, 0	# \$t2F = 1
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0x00000032	0x40000032	li \$t32, 0	li \$t32, 0	# \$t32 = 1
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0x00000039	0x40000039	li \$t39, 0	li \$t39, 0	# \$t39 = 1
0x0000003A	0x4000003A	li \$t3A, 0	li \$t3A, 0	# \$t3A = 1
0x0000003B	0x4000003B	li \$t3B, 0	li \$t3B, 0	# \$t3B = 1
0x0000003C	0x4000003C	li \$t3C, 0	li \$t3C, 0	# \$t3C = 1
0x0000003D	0x4000003D	li \$t3D, 0	li \$t3D, 0	# \$t3D = 1
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0x00000089	0x40000089	li \$t89, 0	li \$t89, 0	# \$t89 = 1
0x0000008A	0x4000008A	li \$t8A, 0	li \$t8A, 0	# \$t8A = 1
0x0000008B	0x4000008B	li \$t8B, 0	li \$t8B, 0	# \$t8B = 1
0x0000008C	0x4000008C	li \$t8C, 0	li \$t8C, 0	# \$t8C = 1
0x0000008D	0x4000008D	li \$t8D, 0	li \$t8D, 0	# \$t8D = 1
0x0000008E	0x4000008E	li \$t8E, 0	li \$t8E, 0	# \$t8E = 1
0x0000008F	0x4000008F	li \$t8F, 0	li \$t8F, 0	# \$t8F = 1
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0x00000097	0x40000097	li \$t97, 0	li \$t97, 0	# \$t97 = 1
0x00000098	0x40000098	li \$t98, 0	li \$t98, 0	# \$t98 = 1
0x00000099	0x40000099	li \$t99, 0		